Audio Accessory IC Series

## OP Amp.



# with 3 Inputs Selector

### BA3131FS

#### Description

The BA3131FS incorporates two built-in circuits with Audio amplifiers, configured of three differential input circuits, an output circuit, and a switch circuit. The three differential input circuits are separate, enabling independent settings to be entered for the gain and frequency characteristics.

#### Features

- 1) High gain and low distortion. (Gv = 110dB, THD = 0.0015% typ.)
- 2) Low noise. (Vn =  $2\mu$ Vrms typ.)
- 3) Switching circuit can be directly coupled to microcomputer port.
- 4) Small switching noise.
- 5) Equipped with 1/2 Vcc output circuit for single power supply.

#### Applications

Car stereos, audio amplifiers, and other electronic circuits

#### •Absolute maximum ratings (Ta=25°C)

| Parameter                  | Symbol | Limits   | Unit |
|----------------------------|--------|----------|------|
| Power supply voltage       | Vcc    | 18.0     | V    |
| Power dissipation          | Pd     | 750*     | mW   |
| Operating temperature      | Topr   | -40-+85  | S    |
| Storage temperature        | Tastg  | -55-+125 | S    |
| Common-mode input voltage  | Vi     | 3-Vcc    | V    |
| Differential input voltage | Vid    | Vcc      | V    |
| Load current               | IOMax. | ±50.0    | mA   |

\*Reduced by 7.5 mW/°C over 25°C, when mounted on a glass epoxy board (90mm ×50mm × 1.6t)

#### Recommended operating conditions (Ta=25°C)

| Parameter                         | Symbol | Min. | Тур. | Max. | Unit | Conditions             |
|-----------------------------------|--------|------|------|------|------|------------------------|
| Operating power<br>supply voltage | Vcc    | 6.0  | 8.0  | 16.0 | V    | single power<br>source |

#### •Electrical characteristics (unless otherwise noted, Ta=25°C, Vcc=8V)

| Parameter                            | Symbol                           | Min. | Тур. | Max. | Unit  | Conditions                          | Test Circuit |  |
|--------------------------------------|----------------------------------|------|------|------|-------|-------------------------------------|--------------|--|
| Quiescent current                    | lq                               | 2.0  | 4.9  | 7.8  | mA    | V <sub>IN</sub> =0,RL=∞,SW pin open | Fig.7        |  |
| Input offset voltage                 | Vio                              | -    | 0.5  | 5.0  | mV    | RS≤10kΩ                             | Fig.6        |  |
| Input offset current                 | lio                              | _    | 5    | 200  | nA    |                                     | Fig.6        |  |
| Input bias current                   | lb                               | _    | 50   | 500  | nA    | *1                                  | Fig.6        |  |
| High-amplitude voltage gain          | Avol                             | 86   | 110  | -    | dB    | RL≥2kΩ, VO=±1.5V                    | Fig.6        |  |
| Common-mode input voltage            | Vicm                             | 3    | 6    | I    | V     |                                     | Fig.6        |  |
| In-phase signal rejection ratio      | CMRR                             | 60   | 72   | I    | dB    | RS≤10kΩ                             | Fig.6        |  |
| Power supply voltage rejection ratio | PSRR                             | 76   | 90   | _    | dB    | RS≤10kΩ                             | Fig.6        |  |
|                                      |                                  | 3    | 6    | I    | V     | RL≥10kΩ                             |              |  |
| Maximum output voltage               | V <sub>OH</sub> /V <sub>OL</sub> | 3    | 6    | I    | V     | RL≥2kΩ                              | Fig.8/Fig.9  |  |
| Input conversion noise voltage       | Vn                               | _    | 2.0  | 4.0  | μVrms | *2                                  | Fig.12       |  |
| Reference voltage change             | $\Delta V_{\text{REF}}$          | _    | _    | ±10  | mV    | loref=±1mA                          | —            |  |

\*1 Since the first stage is configured with PNP transistors, input bias current is from the IC.

<sup>\*</sup>2 Tested under the following conditions: Gv = 40dB,  $RS = 2k\Omega$ , Matsushita Tsuko VP-9690A (using DIN audio filter)

•Design guaranteed values (unless otherwise noted, Ta=25°C, Vcc=8V)

| Parameter                    | Symbol | Min. | Тур.       | Max. | Unit | Conditions                  | Test Circuit |
|------------------------------|--------|------|------------|------|------|-----------------------------|--------------|
| Slew rate                    | SR     | 0.5  | 1.2        | -    | V/µS | Gv=0dB,RL=2kΩ               | Fig.10       |
| Gainbandwidth product        | GBW    | 1.5  | 2.6        | -    | MHz  | f=10kHz                     | Fig.11       |
| Crosstalk between A, B and C | CTABC  | 60   | 73         | _    | dB   | f=1kHz                      | Fig.13       |
| Total harmonic distortion    | THD    | _    | 0.00<br>25 | 0.01 | %    | Gv=0dB, f=1kHz,<br>Vo=1Vrms | Fig.14       |
| Channel separation           | CS     | 90   | 115        | -    | dB   | f=1kHz, input conversion    | Fig.15       |

\*This item is not guaranteed during processes.

#### •Electrical characteristic curves

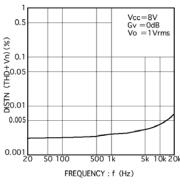
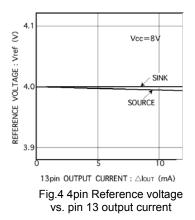


Fig.1 Distortion vs. frequency



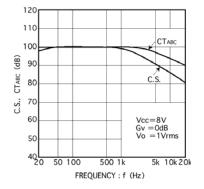


Fig.2 Channel separation and crosstalk vs. frequency

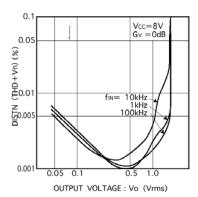
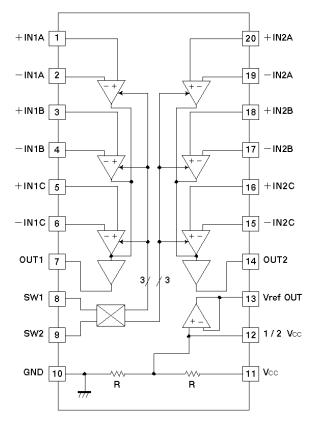
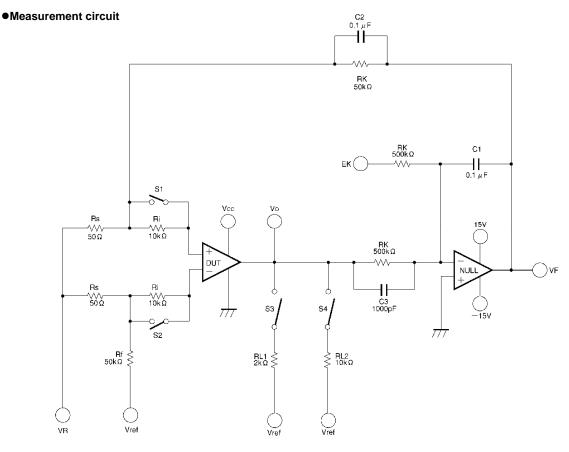


Fig.3 Distortion vs. output voltage

Block diagram







\*C2 and C3 are used to prevent oscillation (adjustment required)

Fig.6

#### Measurement conditions (Figure 6)

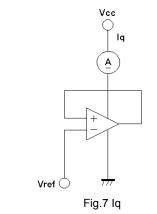
| Measurement Item                                  | Vcc | VR           | EK           | VF   | S1  | S2  | S3  | S4  | Equation |
|---|-----|--------------|--------------|------|-----|-----|-----|-----|----------|
| Input offset voltage                              | 8   | Vref         | -            | VF1  | ON  | ON  | OFF | OFF | 1        |
| Input offset current                              | 8   | Vref         | -            | VF2  | OFF | OFF | OFF | OFF | 2        |
| Innut bing gurrant                                | 0   | Vref         |              | VF3  | OFF | ON  |     | OFF | •        |
| Input bias current                                | 8   | viei         | _            | VF4  | ON  | OFF | OFF | OFF | 3        |
|   | 0   | \ / <b>f</b> | 5.5          | VF5  |     | ON  |     |     | 4        |
| High-amplitude voltage gain                       | 8   | viei         | Vref 2.5 VF6 | ON   | ON  | ON  | OFF | 4   |          |
| Common-mode signal                                | 8   | 6            | 8            | VF7  |     |     |     |     |          |
| rejection ratio<br>(Common-mode input<br>voltage) | 8   | 2            | 0            | VF8  | ON  | ON  | OFF | OFF | 5        |
| Power supply voltage                              | 6   | Vref         |              | VF9  | ON  | ON  | OFF | OFF | 6        |
| rejection ratio                                   | 18  | Vref         | _            | VF10 | ON  | ON  | UFF | UFF | 0        |

#### Equations

(1) Input offset voltage (Vio) Vio = |VF1|/(1 + Rf/Rs)(2) Input offset current (Iio) Iio = |VF2 - VF1|/(Ri(1 + Rf/Rs))(3) Input bias current (Ib) Ib = |VF4 - VF3|/(2 Ri(1 + Rf/Rs))(4) High-amplitude voltage gain (Avol) Avol = 20log (3 (1 + Rf/Rs)/|VF6 - VF5|) (dB) (5) In-phase signal rejection ratio (CMRR) CMRR = 20log (4 (1 + Rf/Rs)/|VF8 - VF7|) (dB) (6) In-phase input voltage range (PSRR)

PSRR = 20log (12 (1 + Rf / Rs) / | VF10 - VF9 | ) (dB)

#### Measurement circuits



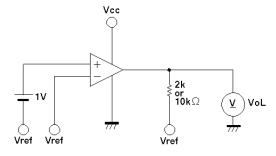


Fig.9 Maximum output voltage: Low

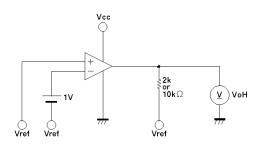
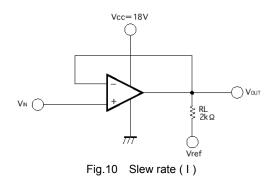
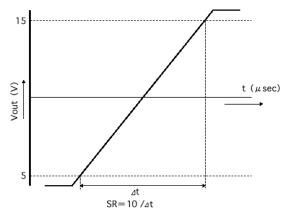
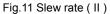


Fig.8 Maximum output voltage: High







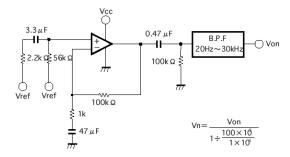
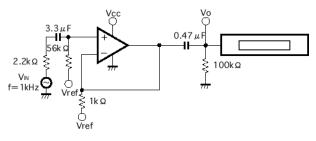


Fig.13 Input conversion noise voltage



Vo=1Vrms

Fig.15 Total harmonic distortion

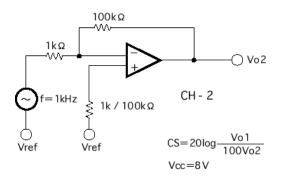


Fig.17 Channel separation (II)

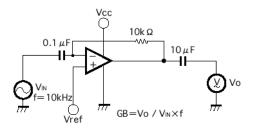


Fig.12 Band width frequency gain

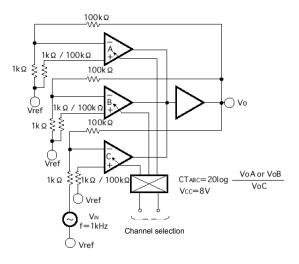


Fig.14 Crosstalk between A and B

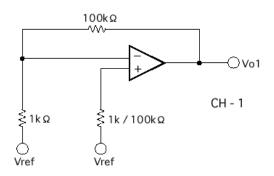


Fig.16 Channel separation (I)

#### •Application example

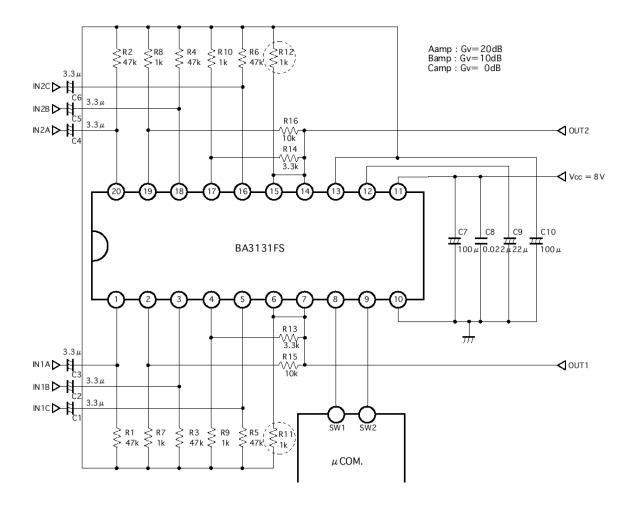


Fig.18

#### •Truth value table

|            | ch1 | ch2 | ch3 | OFF | Conditions                 |
|------------|-----|-----|-----|-----|----------------------------|
| SW1 (8pin) | Н   | Н   | L   | L   |                            |
| SW2 (9pin) | Н   | L   | Н   | L   | Corresponds to µCOM output |

 $\ast$  "H" when the applied voltage at pins 8 and 9 is 2.0V or more, and "L" when it is 1.0V or less.

#### •Cautions on use

#### (1) Numbers and data in entries

Numbers and data in entries are representative design values and are not guaranteed values of the items.

#### (2) Example application circuit

Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.

#### (3) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

#### (4) GND potential

Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

#### (5) Thermal design

Perform thermal design, in which there are adequate margins, by taking into account the power dissipation (Pd) in actual states of use.

#### (6) Short circuit between terminals and erroneous mounting

Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.

#### (7) Operation in strong electromagnetic field

Using the ICs in a strong electromagnetic field can cause operation malfunction.

#### (8) Pin13 (reference output terminal)

Pin 13 is the reference output terminal, which outputs 1/2 Vcc. Determine the bypass condenser value in accordance with the desired characteristics. In addition, as the value may oscillate within the 500pF- 1 $\mu$ F, make sure to set the bypass condenser value to more than 10 $\mu$ F for alternate grounding. Furthermore, as pin 12 is located in the reference circuit, make sure to use bypass condenser for ac grounding for the reference output. (Recommended value22 $\mu$ F)

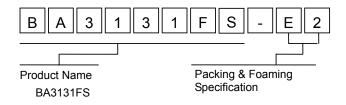
•Reference data (these values are intended only as a reference, and performance is not guaranteed)

| 12 pin bypass capacitor (µF) | Ripple Rejection (fin=100Hz) (dB) | Output Startup Time |
|------------------------------|-----------------------------------|---------------------|
| 10                           | -35                               | 150                 |
| 22                           | -42                               | 300                 |
| 47                           | -48                               | 550                 |

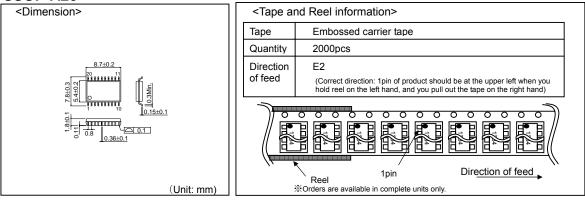
\* Measuring condition: With Power Voltage ON (Vcc=8V), Vcc path control, pin 13 path control100μF, the time which is 90% of equilibrium output voltage

#### (9) Capacity load

This IC can be used in the low grain range (0-2dB). It may oscillate at a capacity load of more than 200pF. The phase margin 10° Typ. (Ta=85°C, 0dB point) for capacity 200pF. Therefore, take precaution when using capacity load. In addition, for using 0db buffer, as shown in the application example (Fig. 18), inserting bias resister of k $\Omega$  to minus input [R11, R12 (within  $\bigcirc$  mark of Fig 18) ] will enable stable use against the capacity load.



#### SSOP-A20



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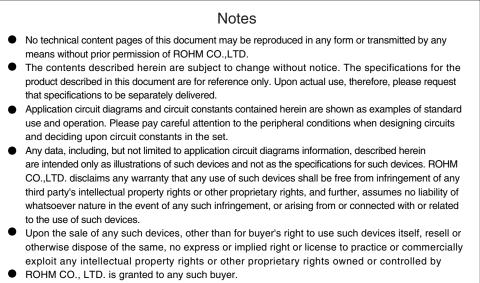
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