AN5290S

Antenna diversity IC for on-vehicle TV

■ Overview

The AN5290S is an on-vehicle television antenna-diversity IC in which the noise detection circuit and antenna changeover circuit are integrated on a single chip. It is destined for NTSC/PAL system.

■ Features

- Built-in vertical and horizontal synchronizing circuit
- It outputs changeover pulse for noise canceler.
- Built-in antenna changeover stop function

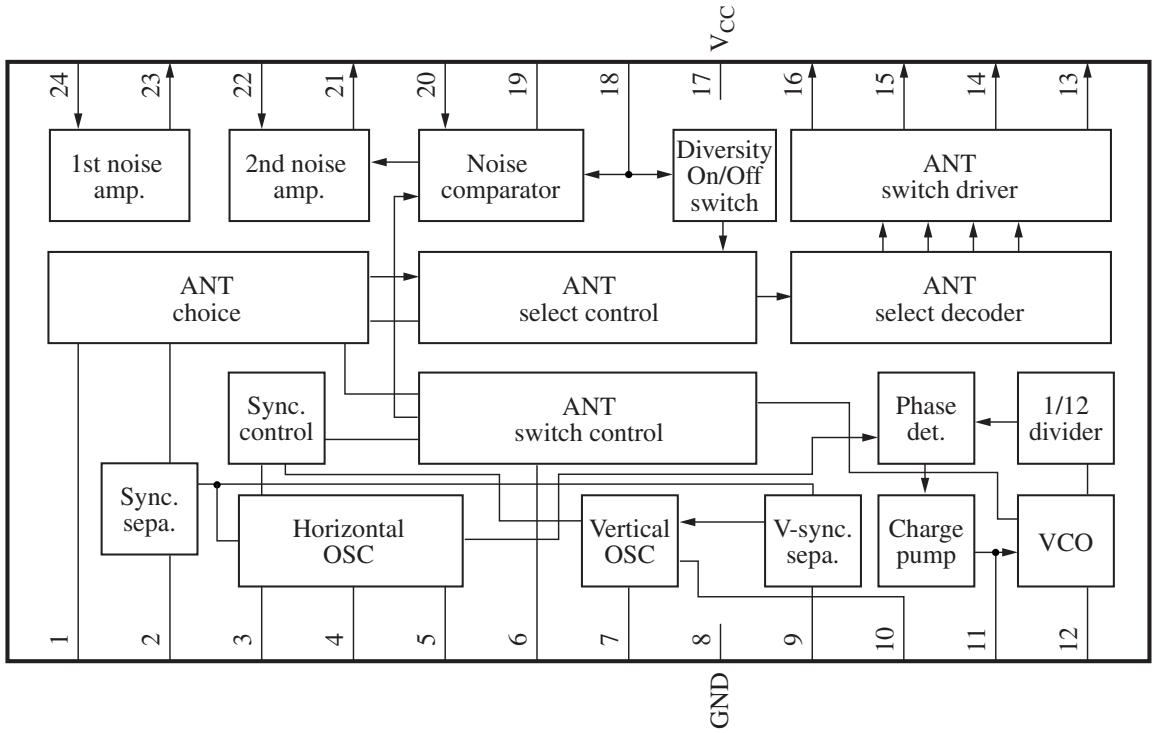
■ Applications

- On-vehicle televisions

■ Package

- SOP024-P-0375C

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Antenna selection level holding capacitance	12	VCO oscillation time-constant setting
2	Sync. separation video signal input	13	Antenna selection output 4
3	Horizontal sync. signal AFC output	14	Antenna selection output 3
4	Horizontal sync. signal oscillation time-constant setting	15	Antenna selection output 2
		16	Antenna selection output 1
5	Horizontal sync. signal output	17	Power supply
6	Output for noise canceler	18	Noise comparator level setting/diversity off
7	Vertical sync. signal output	19	Noise level hold capacitor
8	GND	20	Noise comparator input
9	Vertical sync. signal separation time constant setting	21	2nd noise amplifier output
		22	Video clamp input
10	Vertical sync. signal oscillation time constant setting	23	1st noise amplifier output
		24	Video signal input
11	Charge pump integral time-constant setting		

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.6	V
Supply current	I_{CC}	30.0	mA
Power dissipation *	P_D	168	mW
Operating ambient temperature	T_{opr}	−30 to +80	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note) 1. Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

2. In order to protect the IC, do not use the IC by rotating it 180 degrees.

3. To protect the IC, do not connect the open collector pins (pin 5, pin 6, pin 7, pin 13, pin 14, pin 15 and pin 16) directly to the power supply. Use the protection resistors (1 kΩ or larger for pin 5, pin 6 and pin 7, and 200 Ω or larger for pin 13, pin 14, pin 15 and pin 16). Use the IC within the range of its power dissipation.

4. * : T_a = 80 °C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V

■ Electrical Characteristics at V_{CC} = 5 V, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent current without load	I_{CC}	Without input	12.0	20.0	28.0	mA
Horizontal sync. oscillation frequency *	f_H	Without input, pin 5 frequency	15.58	15.68	15.78	kHz
PLL sync. oscillation frequency	$12f_H$	Without input, pin 12 frequency	186	188.2	190	kHz
Vertical sync. oscillation frequency	f_V	Without input, pin 7 frequency	36.0	42.0	48.0	Hz
Electric field judgment period	f_{FJ}	Without input, pin 21 frequency	36.0	42.0	48.0	Hz
Output frequency for N.C.	f_{NC}	Asynchronous, at changing over antenna, pin 6 frequency	36.0	42.0	48.0	Hz
Antenna selection 1 on voltage	V_{AS1ON}	Voltage, when pin 16 is on	—	0.2	0.5	V
Antenna selection 1 off voltage	V_{AS1OFF}	Voltage, when pin 16 is off	4.9	5.0	—	V
Antenna selection 2 on voltage	V_{AS2ON}	Voltage, when pin 15 is on	—	0.2	0.5	V
Antenna selection 2 off voltage	V_{AS2OFF}	Voltage, when pin 15 is off	4.9	5.0	—	V
Antenna selection 3 on voltage	V_{AS3ON}	Voltage, when pin 14 is on	—	0.2	0.5	V
Antenna selection 3 off voltage	V_{AS3OFF}	Voltage, when pin 14 is off	4.9	5.0	—	V
Antenna selection 4 on voltage	V_{AS4ON}	Voltage, when pin 13 is on	—	0.2	0.5	V
Antenna selection 4 off voltage	V_{AS4OFF}	Voltage, when pin 13 is off	4.9	5.0	—	V

Note) * : The Horizontal oscillation frequency is a frequency after adjustment.

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
1st amplifier voltage gain	A_{N1}	V_{IN} = 10 mV[p-p], f_{IN} = 10 kHz, at 1st amp. active	—	17.0	—	dB
2nd amplifier voltage gain	A_{N2}	V_{IN} = 10 mV[p-p], f_{IN} = 10 kHz, at 2st amp. active	—	17.5	—	dB
Output voltage, when 2nd amplifier is on	V_{NON2}	At 2st amp. active, pin 21 DC voltage	—	1.51	—	V
Output voltage, when 2nd amplifier is off	V_{NOF2}	At 2nd amp. inactive, pin 21 DC voltage	—	4.20	—	V
Antenna input amplifier voltage gain	A_C	V_{IN} = 50 mV[p-p], f_{IN} = 10 kHz, at input amp. active	—	5.5	—	dB
Level hold output bias voltage	V_{NOB2}	At input amp. active, pin 1 DC voltage	—	1.43	—	V
Antenna switch output sink current 1	I_{AS1}	Antenna selection output pin, max. current, when pin 16 is on	10.0	—	—	mA
Antenna switch output sink current 2	I_{AS2}	Antenna selection output pin, max. current, when pin 15 is on	10.0	—	—	mA
Antenna switch output sink current 3	I_{AS3}	Antenna selection output pin, max. current, when pin 14 is on	10.0	—	—	mA
Antenna switch output sink current 4	I_{AS4}	Antenna selection output pin, max. current, when pin 13 is on	10.0	—	—	mA

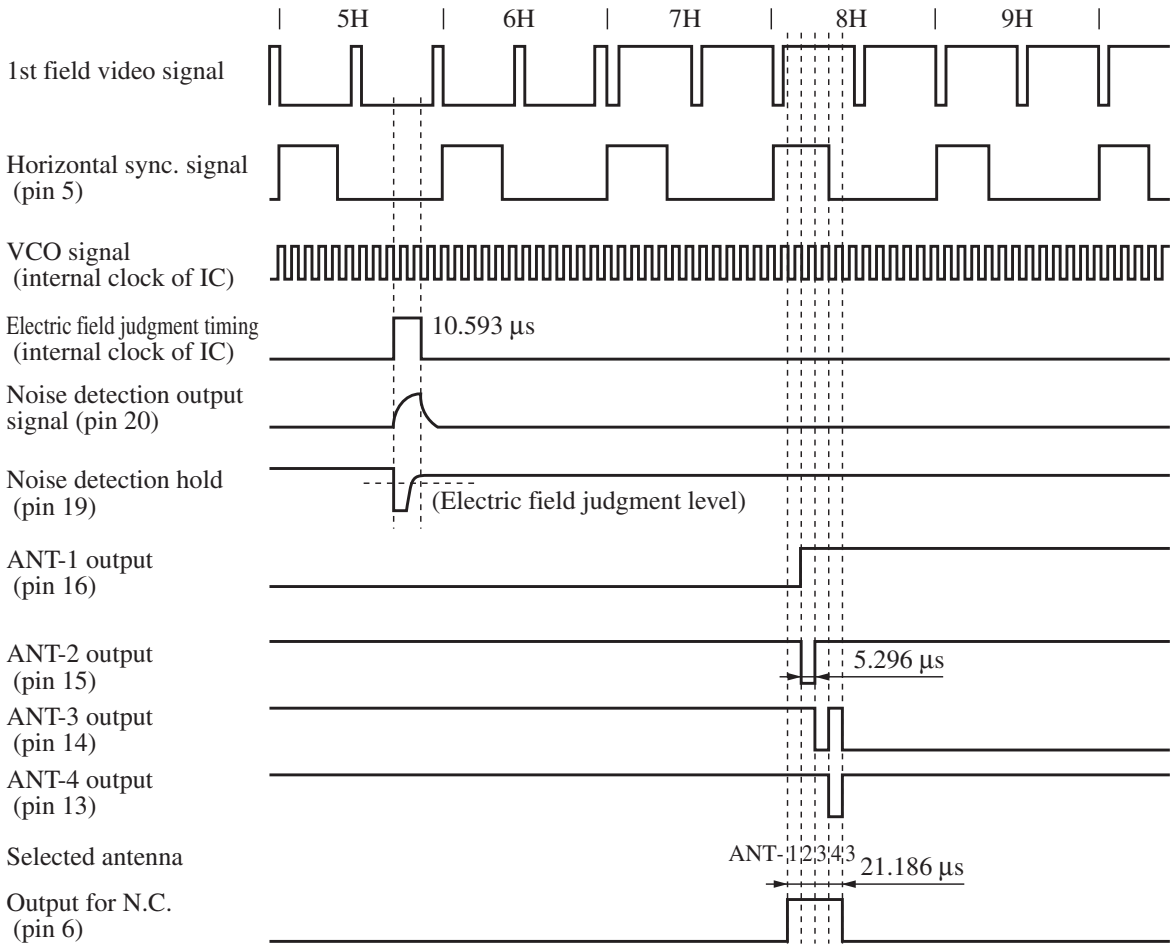
■ Technical Information

Note) The following characteristics are the reference value for design and not guaranteed value. The timing chart is for explaining the IC operation plainly. Those vary depending on input condition.

1. Timing chart 1

- When NTSC reception (in horizontal and vertical synchronization) antenna is selected.

  Electric field judgment and antenna selection timing when the change over from ANT-1 to ANT-3 by the antenna selection is done.



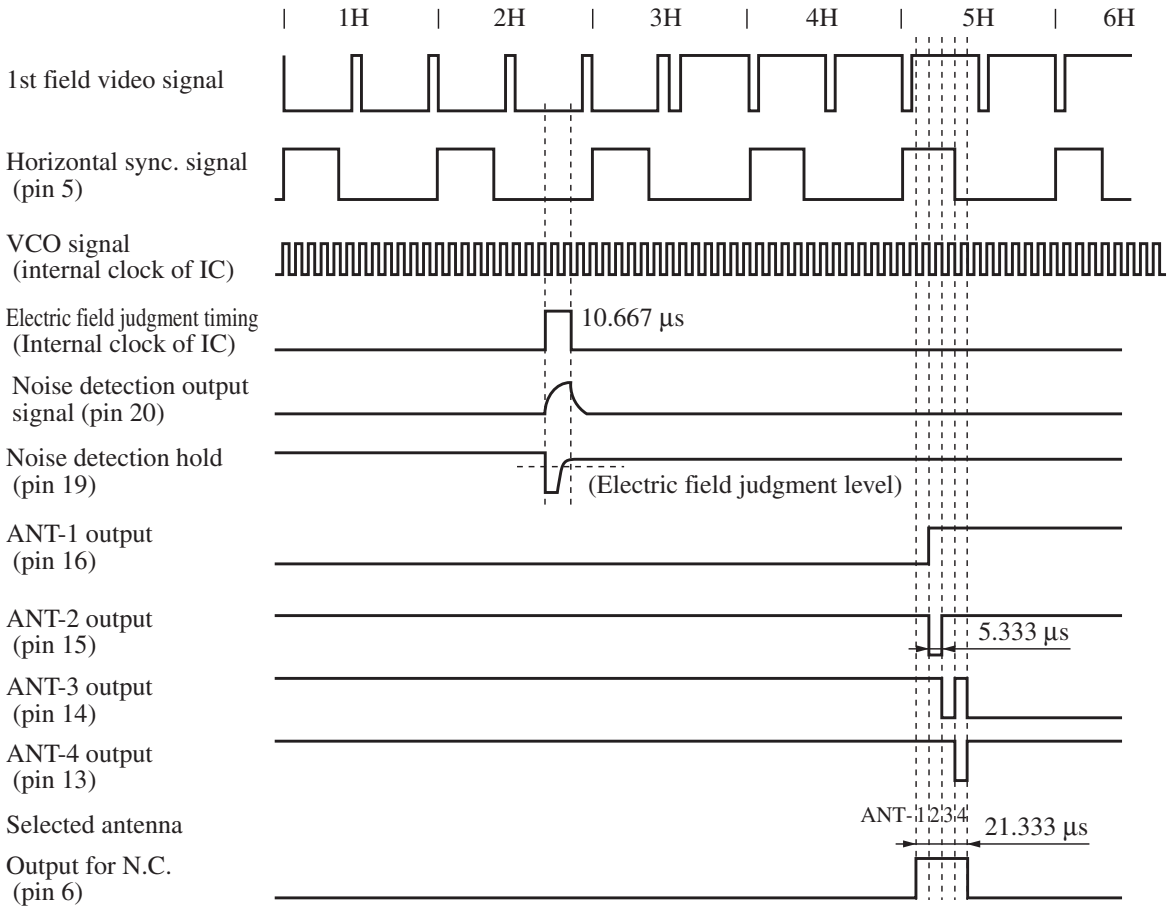
(In the above timing chart, the 1st field video signal is not an internal signal but an input signal, and some signals which do not outputted to pins, as VCO signal, are included.)

■ Technical Information (continued)

2. Timing chart 2

- When PAL reception (in horizontal and vertical synchronization) antenna is selected.

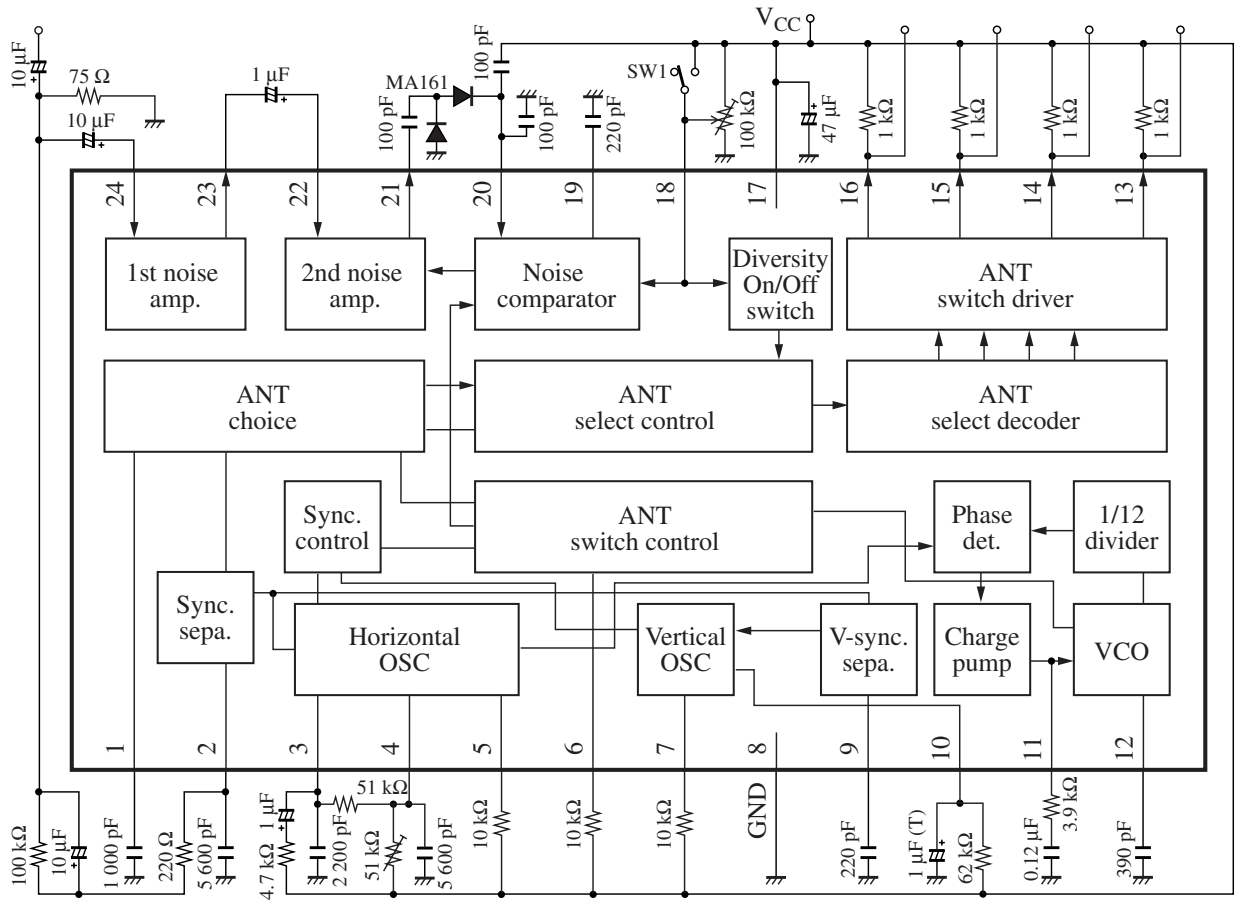
  Electric field judgment and antenna selection timing when the change over from ANT-1 to ANT-3 by the antenna selection is done.



The antenna selection sequence is as follows:

→ ANT-1 → ANT-2 → ANT-3 → ANT-4 →

■ Application Circuit Example



The circuit shows an example of application circuit and circuit constant but does not guarantee the design of mass-production set.

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