ISD2100

Digital ChipCorder

with

Multi Time Programming and Digital Audio Interface

TABLE OF CONTENTS

1 GENERAL DESCRIPTION

The ISD2100 is a digital ChipCorder® featuring digital de-compression, comprehensive memory management, flash storage, and integrated digital audio signal paths. This family utilizes flash memory to provide non-volatile audio playback with duration up to 30 seconds (based on 8kHz/4bit ADPCM) for a single-chip solution.

Unlike the MLS ChipCorder series, this device provides higher sampling frequency and a signal path with SNR equivalent to 12-bit resolution.

The ISD2100 can take digital audio data via SPI interface. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD2100 supported sample rates.

The ISD2100 has built-in speaker driver output.

2 FEATURES

- Duration
  - 30 seconds based on 8kHz/4bit ADPCM (**ISD2130)**
- Audio Management
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences.
- Sample Rate
  - 7 sampling frequencies such as 4, 5.3, 6.4, 8, 12.8, 16 and 32 kHz are available.
- Compression Algorithms
  - µ-Law: 6, 7 or 8 bits per sample
  - Differential µ-Law: 6, 7 or 8 bits per sample
  - PCM: 8, 10 or 12 bits per sample
  - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
  - Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
  - Internal oscillator with internal reference: with ±1% deviation at room temperature.
- Output
  - PWM: Class D speaker driver to direct drive an 8Ω speaker or buzzer
- I/Os
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - 6 general purpose I/O pins that share SPI interface.
- One 8-bit Volume Controls set by SPI command.
- Operating Voltage: 2.7-3.6V
- Package: green, 20L-QFN
- Temperature Options:
  - Industrial: -40°C to 85°C

3 BLOCK DIAGRAM

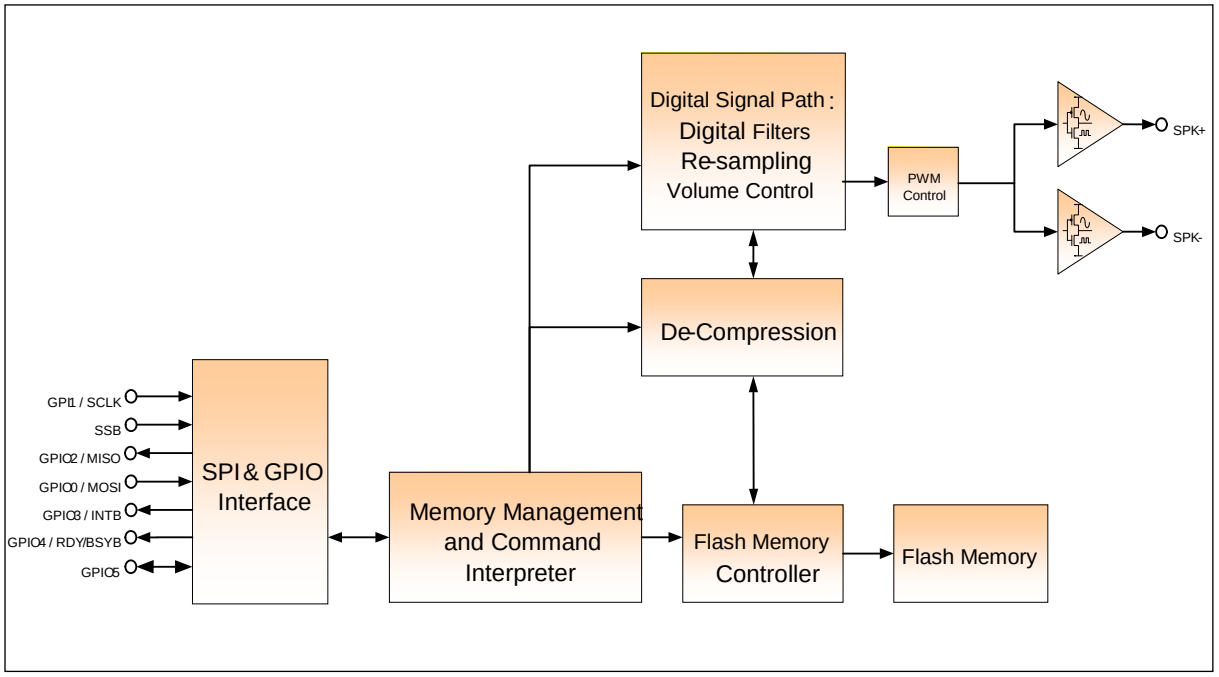


Figure 3-1 ISD2100 Block Diagram

4 PINOUT CONFIGURATION

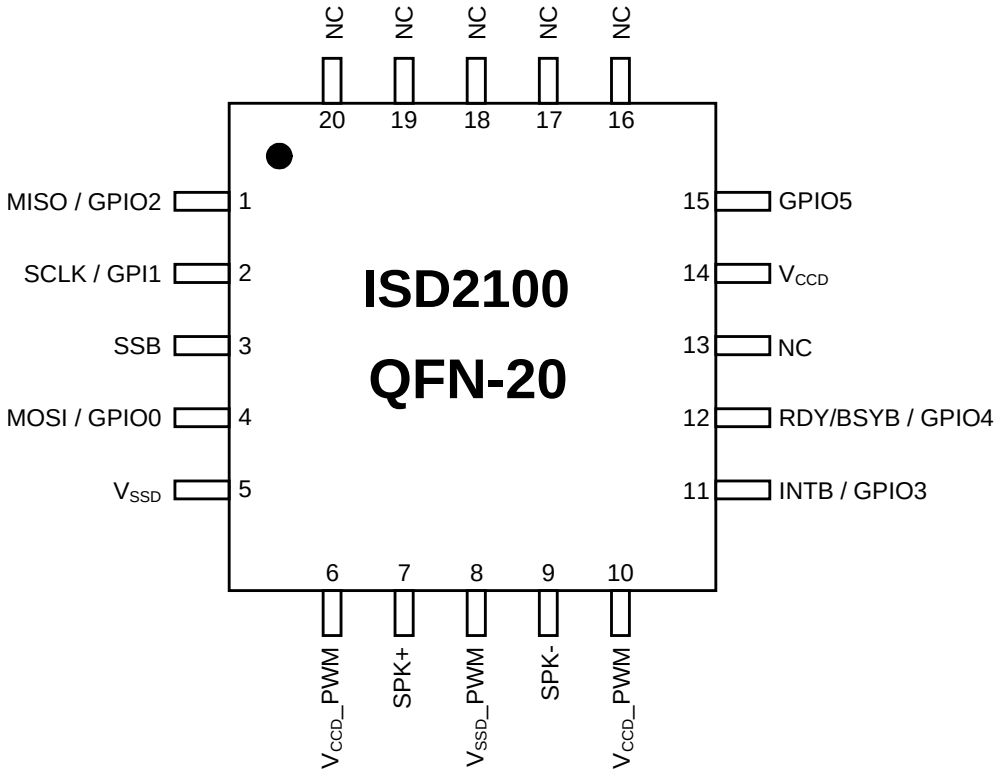


Figure 4-1 ISD2100 20-Lead QFN Pin Configuration.

5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	MISO / GPIO2	O	Master-In-Slave-Out. Serial output from the ISD2100 to the host. This pin is in tri-state when SSB=1. Can be configured as a general purpose I/O pin.
2	SCLK / GPI1	I	Serial Clock input to the ISD2100 from the host. Can be configured as a general purpose input pin.
3	SSB	I	Slave Select input to the ISD2100 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
4	MOSI / GPIO0	I	Master-Out-Slave-In. Serial input to the ISD2100 from the host. Can be configured as a general purpose I/O pin.
5	V_{SSD}	I	Digital Ground.
6	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
7	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state.
8	V_{SSD}_PWM	I	Digital Ground for the PWM Driver.
9	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state.
10	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
11	INTB / GPIO3	O	Active low interrupt request pin. This pin is an open-drain output. Can be configured as a general purpose I/O pin.
12	RDY/BSYB / GPIO4	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD2100 is ready to accept new SPI commands or data. Can be configured as a general purpose I/O pin.
13	NC		This pin should be left unconnected.
14	V_{CCD}	I	Digital Power.
15	GPIO5	I/O	General purpose I/O pin.
16	NC		This pin should be left unconnected.
17	NC		This pin should be left unconnected.
18	NC		This pin should be left unconnected.
19	NC		This pin should be left unconnected.
20	NC		This pin should be left unconnected.

6 SPI INTERFACE

This is a standard four-wire interface used for communication between ISD2100 and the host. It consists of an active low slave-select (SSB), a serial clock (SCLK), a data input (Master Out Slave In - MOSI), and a data output (Master In Slave Out - MISO). In addition, for some transactions requiring data flow control, a RDY/BSYB signal (pin) is available.

The ISD2100 supports **SPI mode 3:** (1) SCLK must be high when SPI bus is inactive, and (2) data is sampled at SCLK rising edge. A SPI transaction begins on the falling edge of SSB and its waveform is illustrated below:

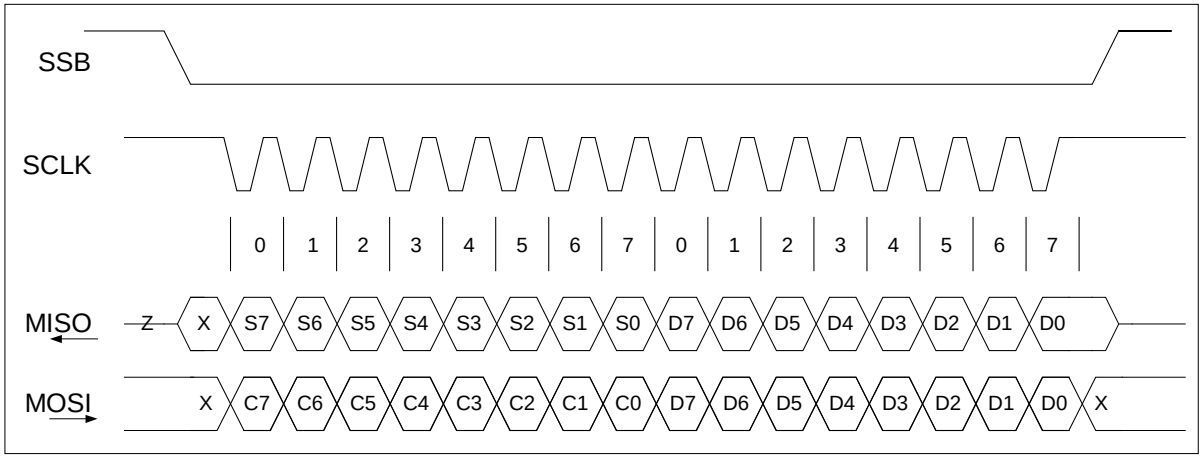


Figure 6-1 SPI Data Transaction.

A transaction begins with sending a command byte (C7-C0) with the most significant bit (MSB – C7) sent in first. During the byte transmission, the status (S7-S0) of the device is sent out via the MISO pin. After the byte transmission, depending upon the command sent, one or more bytes of data will be sent via the MISO pin.

RDY/BSYB pin is used to handshake data into or out of the device. Upon completion of a byte transmission, RDY/BSYB pin could change its state after the rising edge of the SCLK if the built-in 32-byte data buffer is either full or empty. At this point, SCLK must remain high until RDY/BSYB pin returns to high, indicating that the ISD2100 is ready for the next data transmission. See below for timing diagram.

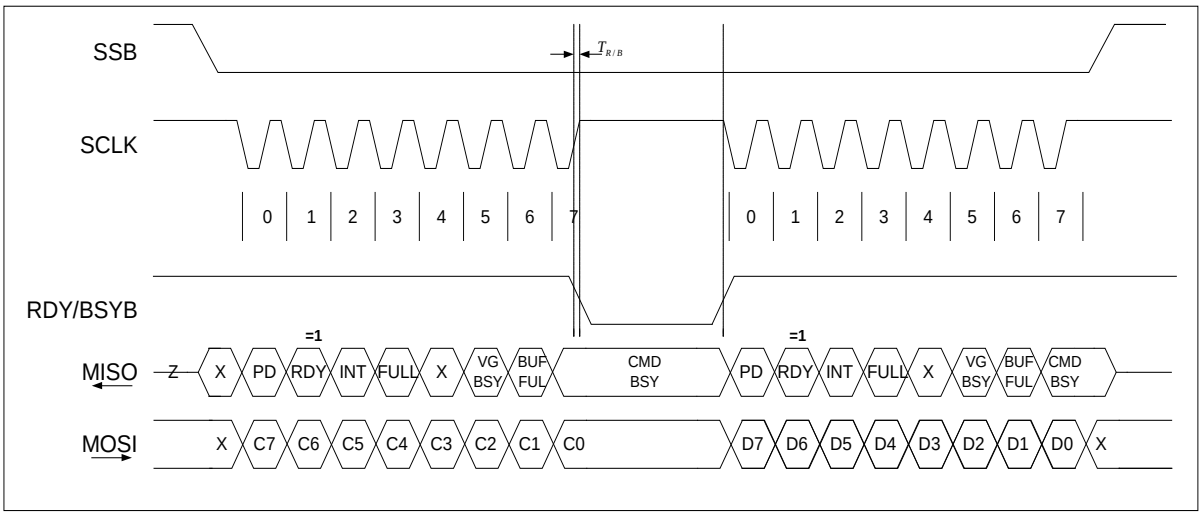


Figure 6-2 RDY/BSYB Timing for SPI Writing Transactions.

If the SCLK does not remain high, RDY bit of the status register will be set to zero and be reported via the MISO pin so the host can take the necessary actions (i.e., terminate SPI transmission and re-transmit the data when the RDY/BSYB pin returns to high).

For commands (i.e., DIG_READ, SPI_PCM_READ) that read data from ISD2100, MISO is used to read the data; therefore, the host must monitor the status via the RDY/BSYB pin and take the necessary actions.

The INT pin will go low to indicate (1) data overrun/overflow when sending data to the ISD2100; or (2) invalid data from ISD2100. See Figure 6-3 for the timing diagram.

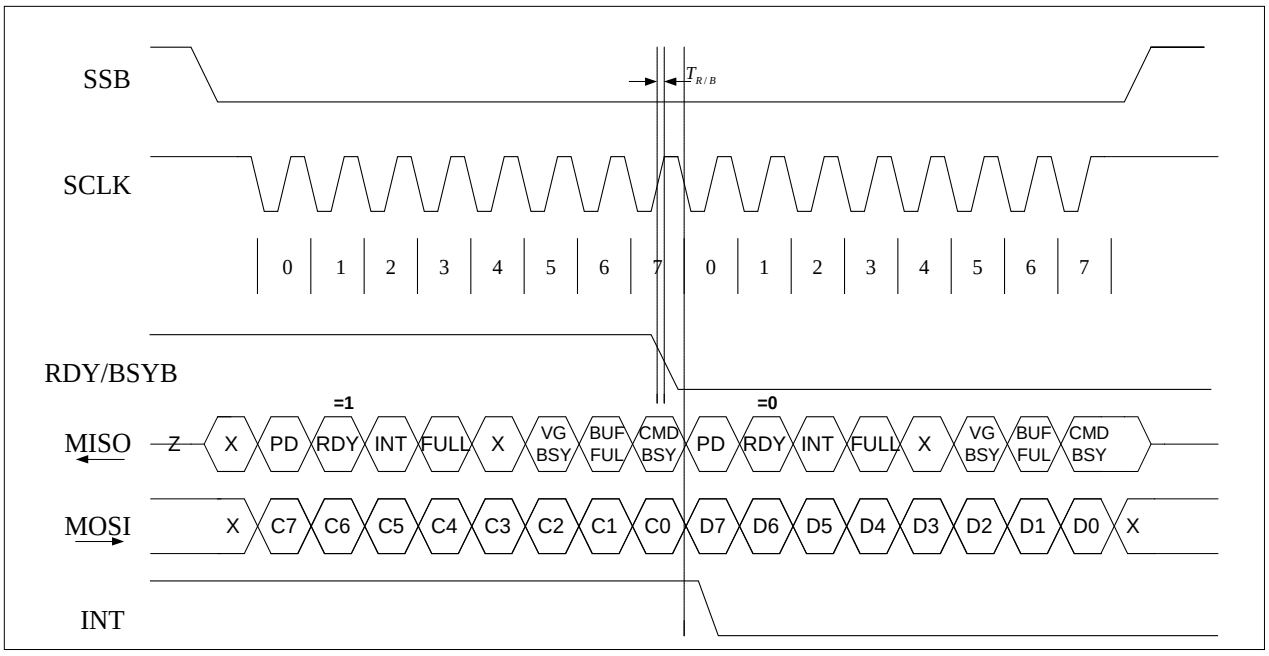


Figure 6-3 SPI Transaction Ignoring RDY/BSYB

7 ANALOG AND DIGITAL SIGNAL PATH

7.1.1 PWM Speaker Driver

PWM driver output pins SPK-, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down these pins are in tri-state.

7.1.2 Internal Oscillator

The ISD2100 device has an internal oscillator that requires no external resistor to operate, however the ISD2100 also provide an internal oscillator with external reference resistor (Rosc) that has an accuracy of ±5% with selectable master sample rate 4Khz, 5.33Khz, 6.4khz, 8Khz, 12.8Khz, 16Khz, and 32Khz.

8 ISD2100 MEMORY MANAGEMENT

The ISD2100 employs several memory management techniques to make audio playback transparent to the host controller. The address space of the ISD2100 starts at address zero of the internal memory.

8.1 MESSAGE MANAGEMENT

The message management schemes implemented on the ISD2100 are:

1. Voice Prompts: A collection of pre-recorded audio that can be played back using the PLAY_VP SPI command or Voice Macros.
2. Voice Macros: A powerful voice script allowing users to create custom macros to play Voice Prompts, insert silence and configure the device. Voice Macros are executed with a single SPI command.
3. User Data: Memory sectors defined and allocated by the users for use in other applications

8.1.1 Voice Prompts

Voice prompts are pre-recorded audio of any length, from short words, phrases or sound effects to long passages of music. These Voice Prompts can be played back in any order as determined by the users and applications. A Voice Prompt consists of two components:

1. An index pointing to the pre-recorded audio
2. Pre-recorded audio

8.1.2 Voice Macros

Voice Macros are a powerful voice script that allows users to customize their own play patterns such as play Voice Prompts, insert silence, change the master sample clock, power-down the device and configure the signal path, including gain and volume control.

8.1.3 GPIO Voice Trigger Macros:

The ISD2100 GPIO flexibility allows the user to configure the device to triggers a voice macro in many different combinations for a push button application. Below is some possible configuration of the GPIO pins using Voice trigger macros?

1. **Single Hi-Low trigger sequence through messages**

A high to low trigger on any GPIO 0~ 5 will start to play Voice Macro 3, 4, 5, 6 and back to Voice Macro 3. Each Voice Macro points directly or indirectly to voice prompt One, Two, Three, Four.

2. **Single Hi-Low trigger Loop unless interrupted by another Trigger**

A single trigger on any GPIO 0~ 5 will loop through several messages until it is interrupted by another trigger to stop playback, the device goes to power down after.

3. **Single Hi-Low trigger through messages uninterruptable by another Trigger**

A single trigger on any GPIO 0~ 5 will sequence through several messages until all messages are played. The playback cannot be interrupted by another trigger on any GPIO 0~ 5 to stop playback.

4. **Single Hi-Low trigger sequences through messages with silence (pause) in between each message.**

A single trigger on any GPIO 0~ 5 will sequence through several messages with pause in between each message. A 256ms play silence added in between each message to create a short pause for natural sound. All messages are played in a loop indefinitely until another trigger on any GPIO 0~ 5 to stop playback.

5. **Level Hold trigger sequence through messages interruptible**

A Level Hold on any GPIO 0~ 5 will sequence through several messages with pause in between each message. A 32ms play silence added in between each message to create a very short pause for natural sound. Playback stops when GPOI is released or all messages are played.

6. **Level Hold trigger Loop through messages interruptible**

A Level Hold on any GPIO 0~ 5 will loop through several messages with pause in between each message. A 32ms play silence added in between each message to create a very short pause for natural sound. Playback stops when GPOI is released or interrupted or by another GPIO trigger.

9 ELECTRICAL CHARACTERISTICS

9.1 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85°C
Supply voltage (V_{DD}) [1]	+2.7V to +3.6V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 3.6V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] $V_{DD} = V_{CCA} = V_{CCD} = V_{CCPWM}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSPWM}$

9.2 AC PARAMETERS

9.2.1 Internal Oscillator

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Internal Oscillator with internal reference	F_{INT}	-1%	65.536 MHz	+1%	MHz	Vdd = 3V. At room temperature

9.2.2 Speaker Outputs

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SNR, Memory to SPK+/SPK-	SNR_{MEM_SPK}		60		dB	Load 150Ω [2][3]
Output Power	P_{OUT_SPK} VCC=3.0			0.4	W	Load 8Ω [2]
THD, Memory to SPK+/SPK-	THD %		<1%			Load 8Ω [2]
Minimum Load Impedance	$R_{L(SPK)}$	4	8		Ω	

Notes: [1] Conditions V_{cc}=3V, T_A=25°C unless otherwise stated.

[2] Based on 12-bit PCM.

[3] All measurements are C-message weighted.

9.3 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.7		3.6	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	

Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1mA
INTB Output Low Voltage	V_{OH1}			0.4	V	
Playback Current	$I_{DD\_Playback}$		5		mA	No Load
Standby Current	I_{SB}		1	10	µA	V_{DD}= 3.6V
Input Leakage Current	I_{IL}			±1	µA	Force V_{DD}

Notes: [1] Conditions V_{DD}=3V, T_A=25°C unless otherwise stated

9.3.2 SPI Timing

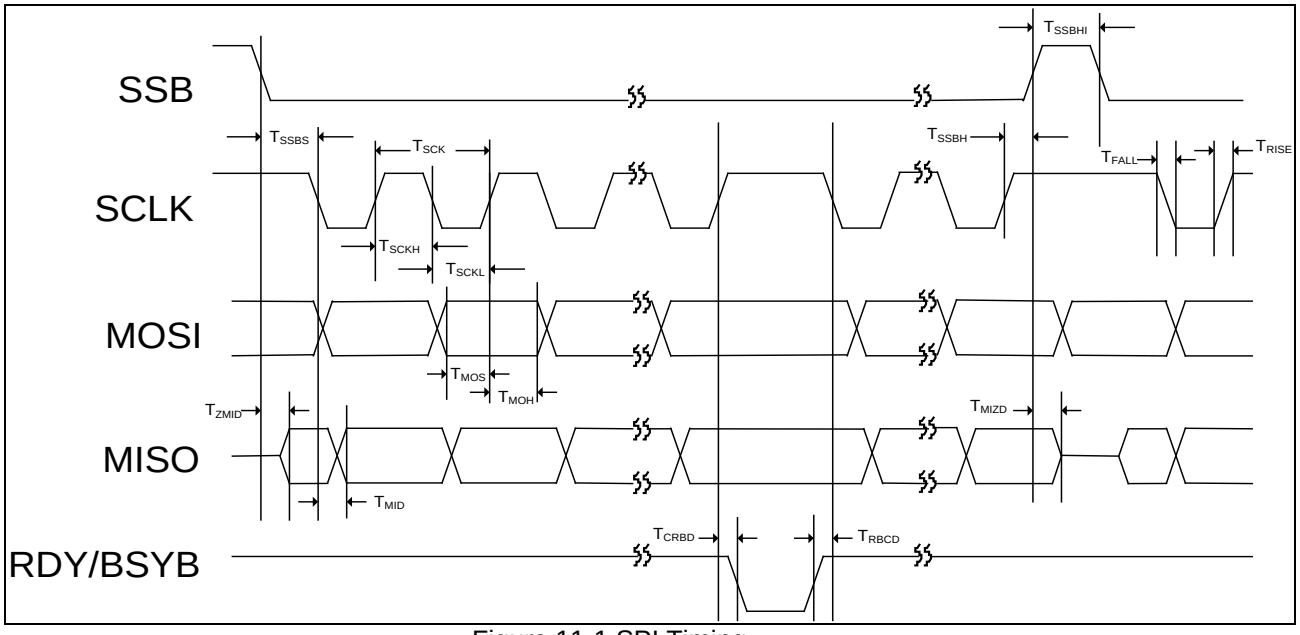


Figure 11-1 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

10 APPLICATION DIAGRAM

The following applications example is for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

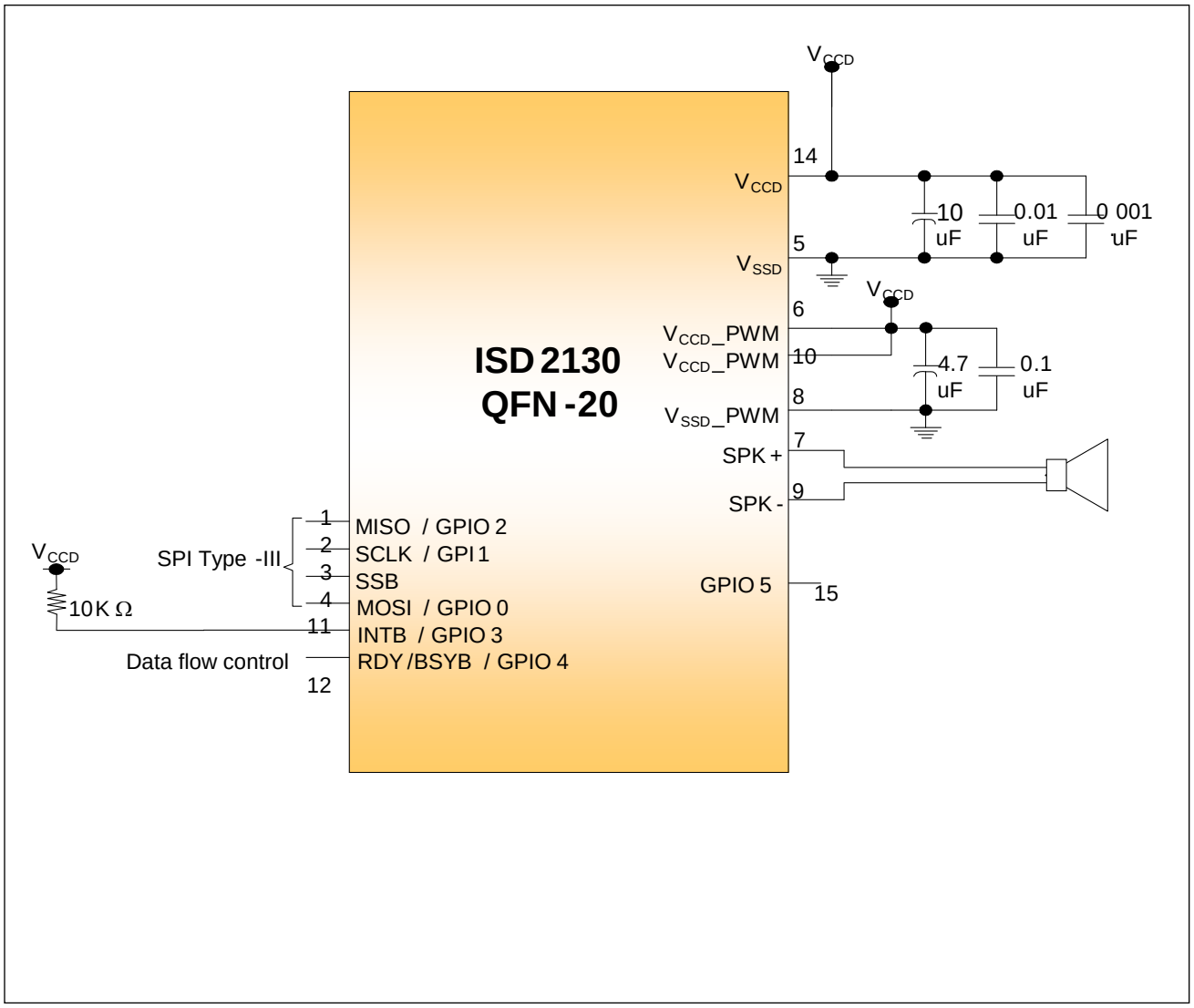
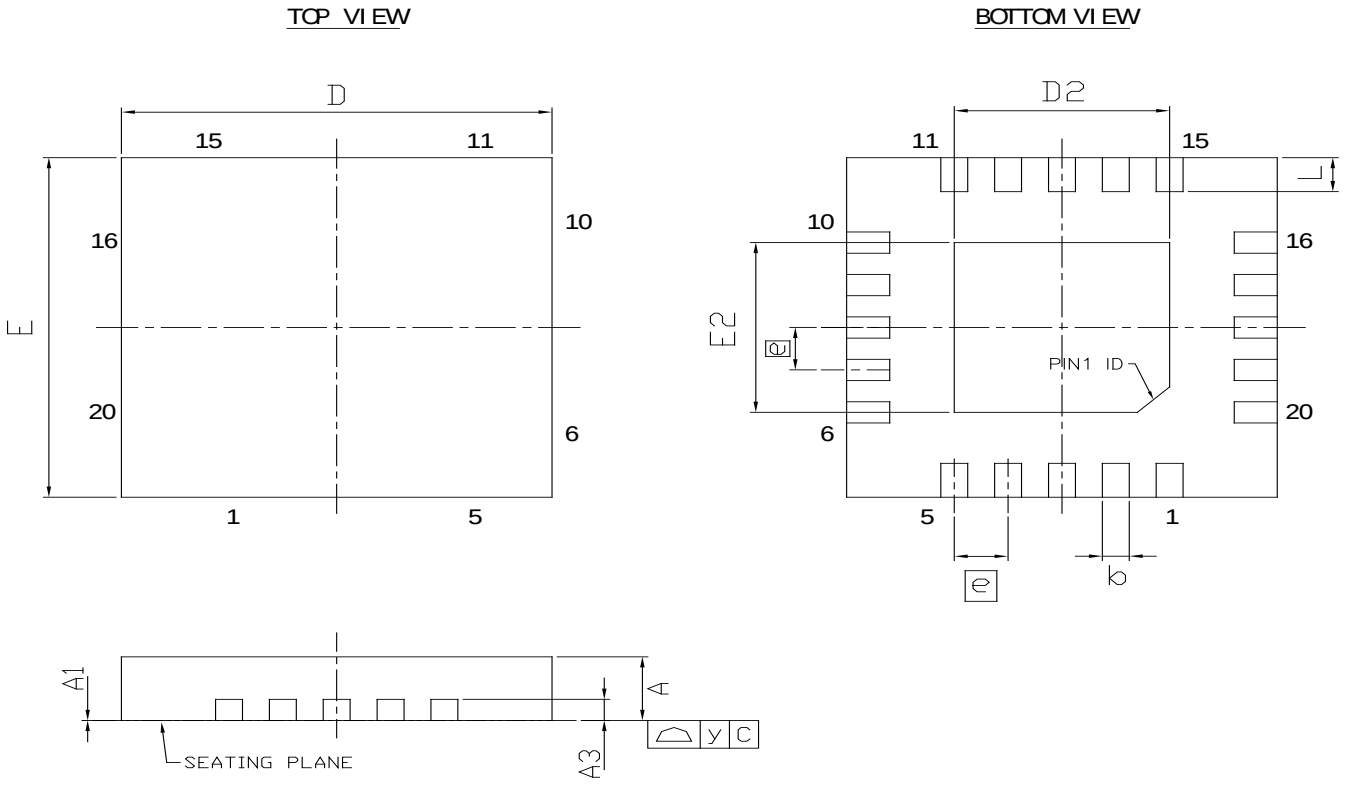


Figure 12-1 ISD2100 Application Diagram

The above application examples are for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

11 PACKAGE SPECIFICATION

11.1 20 LEAD QFN

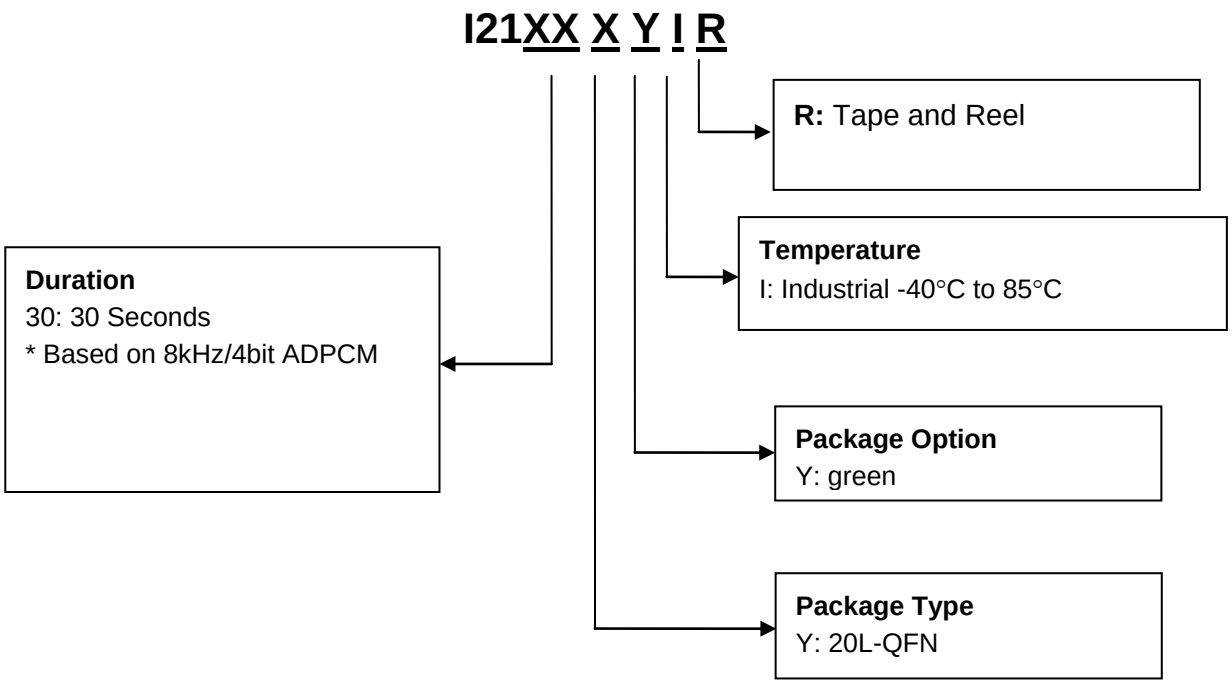


Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

12 ORDERING INFORMATION



13 REVISION HISTORY

Version	Date	Description
0.2	Jan 29, 2009	Initial draft.
0.45	August 5, 2009	Add Wake-Up VM description
0.46	November 11, 2009	Add Checksum Description
0.48	January 9, 2010	Simplify all Block diagrams
0.51	Feb 4, 2010	Update description

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Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.nuvoton.com.tw/

Nuvoton Technology Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
http://www.nuvoton-usa.com/

Nuvoton Technology (Shanghai) Ltd.
27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356998

Taipei Office
9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Nuvoton Technology Corporation Japan
7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokuku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Nuvoton Technology (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064