ISD15C00

Multi-Message Record/Playback Devices

with Digital Audio Interface

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1 GENERAL DESCRIPTION

The ISD15C00 is a multi-message ChipCorder® featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The message management feature is designed to make message recording simple and address-free as well as make code development easier for playback-only applications. The ISD15C00 utilizes winbond 25X/25Q series flash memory to provide non-volatile audio record/playback for a two-chip solution. Unlike other ChipCorder series, the ISD15C00 provides an I^2S digital audio interface, faster digital recording, higher sampling frequency, and a signal path with SNR equivalent to 12bit resolution.

The ISD15C00 can take digital audio data via I^2S or SPI interface. When I^2S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD15C00 supported sample rates.

The ISD15C00 has built-in analog audio inputs, analog audio line driver, and speaker driver output. The two analog audio inputs to the device are: (1) AUXIN has a fixed gain configured by SPI command, and (2) ANAIN/ANAOUT has a fixed gain amplifier with the gain set by two external resistors. ANAIN/ANAOUT can also be used as a microphone differential input (ANAIN/ANAOUT becomes MIC+/MIC-) in conjunction with an automatic gain control (AGC) circuit configured by SPI command. Analog outputs are available in three forms: (1) AUXOUT is a single-ended voltage output; (2) AUDOUT can be configured as either a single-ended voltage output or a single-ended current output; (3) BTL (bridge-tied-load) is a differential voltage output.

2 FEATURES

- External Memory: support winbond 25X/25Q SpiFlash.
  - The addressing ability of ISD15C00 is up to 128Mbit, which is 64-minute recording time based on 8kHz/4bit ADPCM.
- Fast Digital Programming
  - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Message Management
  - Perform address-free recording: The ISD15C00 allocates memory for new recording requests and upon completion, returns a start address to the host via SPI interface
  - Store pre-recorded audio (Voice Prompts) using high quality digital compression
  - Use a simple index based command for playback
  - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences and message recordings.
- Sample Rate
  - Seven record and playback sampling frequencies are available for a given master sample rate. For example, the record and playback sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate.
  - For I^2S operation, 32, 44.1 and 48kHz master sample rates are available with record and playback sampling frequencies scaling accordingly.
- Compression Algorithms
  - For recording
    - ADPCM: 2, 3, 4 or 5 bits per sample
    - µ-Law: 6, 7 or 8 bits per sample
    - Differential µ-Law: 6, 7 or 8 bits per sample
    - PCM: 8, 10 or 12 bits per sample. Each sampled value is stored as a code, offering no compression but preserving maximum resolution

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- For Pre-Recorded Voice Prompts
  - µ-Law: 6, 7 or 8 bits per sample
  - Differential µ-Law: 6, 7 or 8 bits per sample
  - PCM: 8, 10 or 12 bits per sample
  - Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
  - Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
  - Internal oscillator with internal reference: 2.048 MHz with ±10% deviation
  - Internal oscillator with external resistor: 2.048 MHz with ±5% deviation when Rosc is 80k-ohm
  - External crystal or clock input
  - I^2S bit clock input
  - Crystals and resonators support standard audio sampling rates of 2.048, 4.096, 8.192, 12.288 and11.2896MHz
- Inputs
  - AUXIN: Analog input with 2-bit gain control configured by SPI command
  - ANAIN/ANAOUT:
    - Analog input with the gain set by two external resistors from ANAOUT to ANAIN, or
    - Microphone differential input (ANAIN/ANAOUT becomes MIC+/MIC-)
  - Digital AGC:
    - Automatic gain control of digitized data from the analog input
- Outputs
  - PWM: Class D speaker driver to direct drive an 8Ω speaker or buzzer
  - AUDOUT: configurable as a current or voltage single-ended line driver
  - AUXOUT: a single-ended voltage output
  - BTL: a differential voltage output
- I/Os
  - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
  - I^2S interface: I^2S_CLK, I^2S_WS, I^2S_SDI, I^2S_SDO for digital audio data
  - 8 GPIO pins (4 of the 8 GPIO pins share with I^2S).
- Three 8-bit Volume Control set by SPI command for flexible mixing
  - VOLA: volume control for the digital audio data from I^2S or analog inputs
  - VOLB: volume control for the digital audio data from decompression block or SPI
  - VOLC: master volume control for PWM, AUDOUT, AUXOUT and I^2S outputs
- Operating Voltage: 2.7-3.6V
- Standby Current: 1uA typical
- Package: Green 48L-LQFP
- Temperature Options:
  - Industrial: -40°C to 85°C

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3 BLOCK DIAGRAM

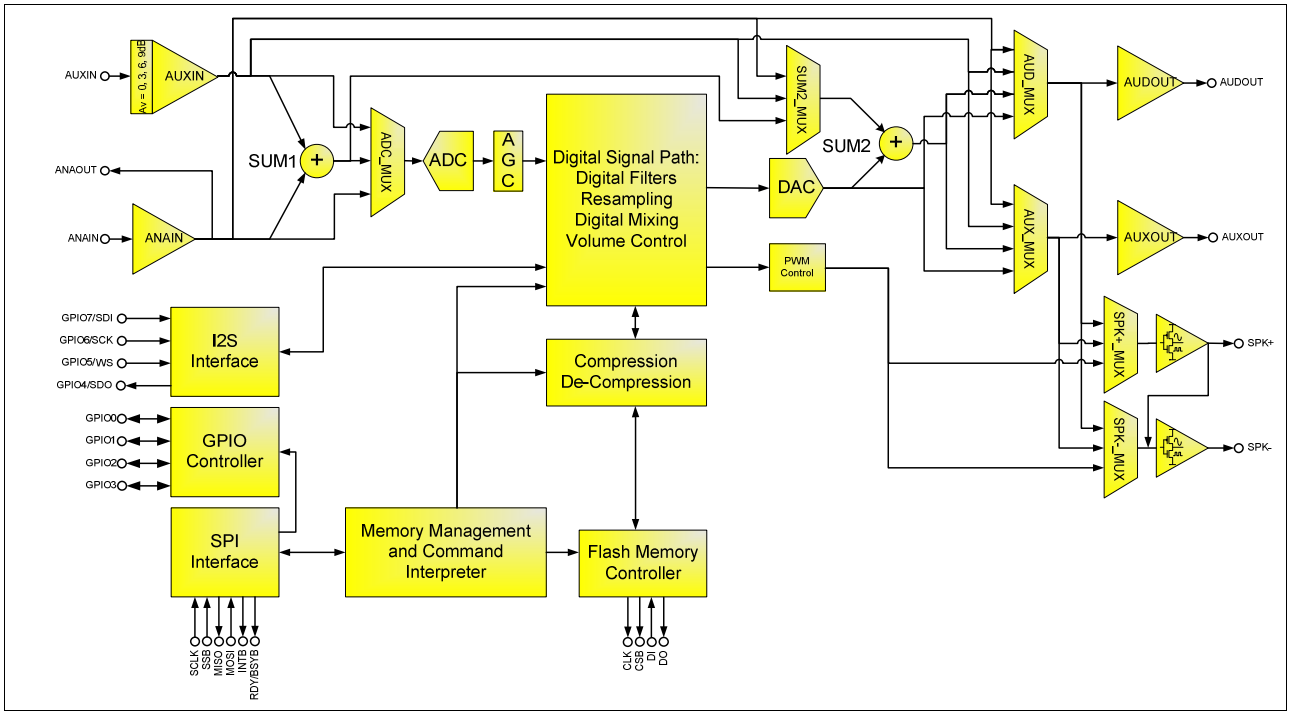

Figure 3-1 ISD15C00 Block Diagram, ANAIN Selected

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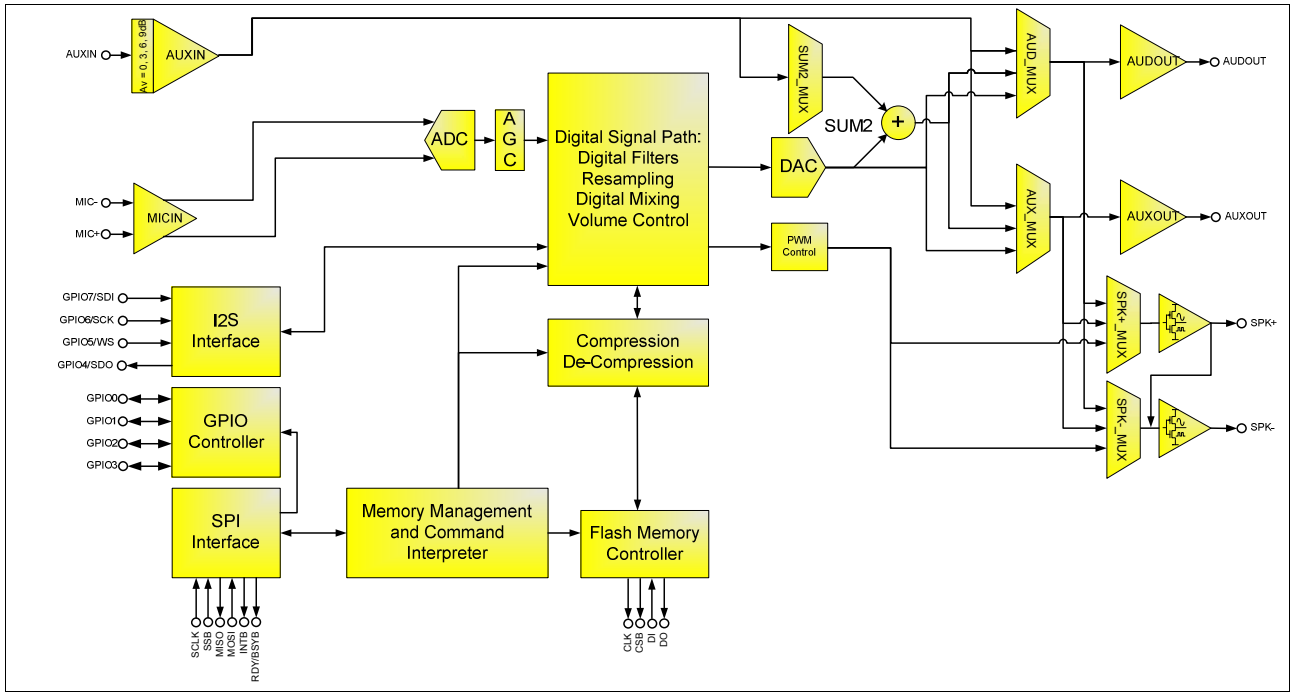

Figure 3-2 ISD15C00 Block Diagram, MICIN Selected

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4 PINOUT CONFIGURATION

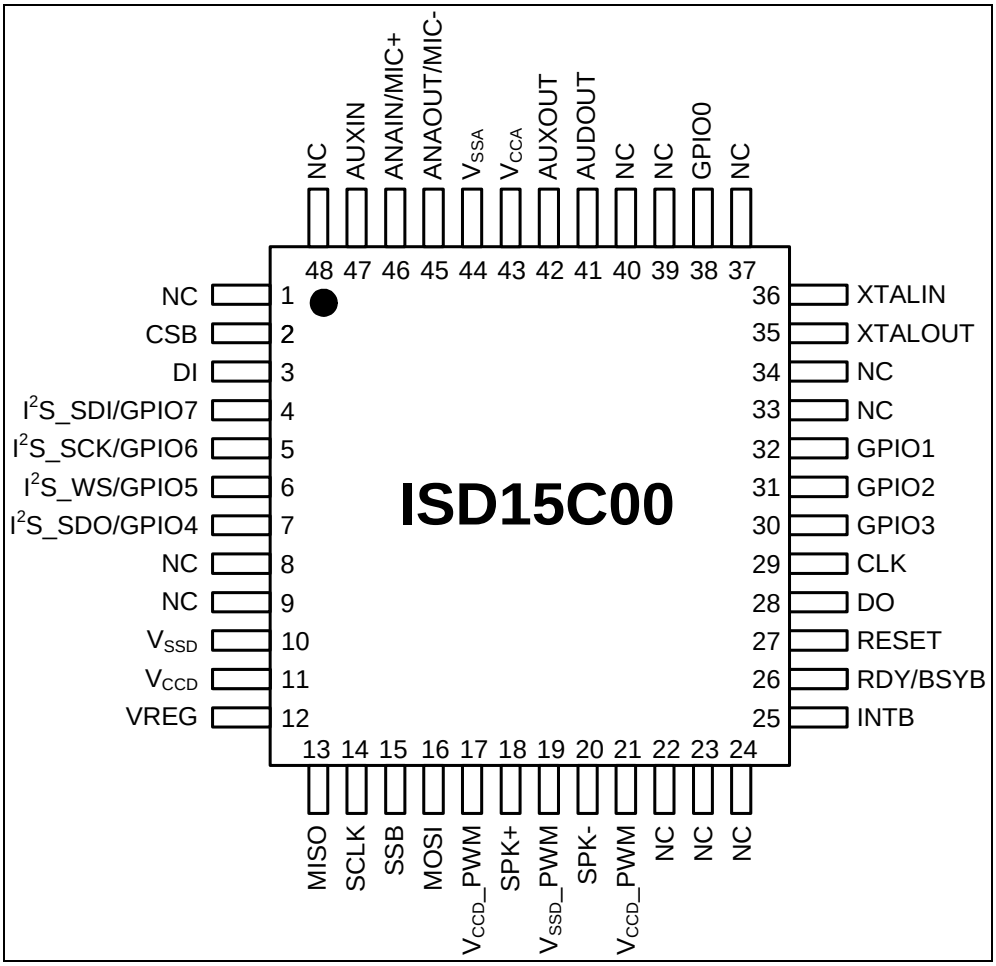

Figure 4-1 ISD15C00 48-Lead LQFP Pin Configuration.

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5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	NC		This pin should be left unconnected.
2	CSB	O	Chip Select Bar of the external serial flash interface.
3	DI	I	Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory.
4	I^2S_SDI/ GPIO7	I	Serial Data Input of the I^2S interface (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
5	I^2S_SCK/ GPIO6	I/O	Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I^2S is not used (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
6	I^2S_WS/ GPIO5	I/O	Word Select (WS) input in slave mode or WS output in master mode (If I2S is not used, this pin should be grounded). Or, can be configured as a GPIO pin.
7	I^2S_SDO/ GPIO4	O	Serial Data Output of the I^2S Interface (If I2S is not used, this pin should be left unconnected). Or, can be configured as a GPIO pin.
8	NC		This pin should be left unconnected.
9	NC		This pin should be left unconnected.
10	V_{SSD}	I	Digital Ground.
11	V_{CCD}	I	Digital power supply.
12	VREG	O	A 1.8V regulator to supply the internal logic. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability.
13	MISO	O	Master-In-Slave-Out. Serial output from the ISD15C00 to the host. This pin is in tri-state when SSB=1.
14	SCLK	I	Serial Clock input to the ISD15C00 from the host.
15	SSB	I	Slave Select input to the ISD15C00 from the host. When SSB is low device is selected and responds to commands on the SPI interface.
16	MOSI	I	Master-Out-Slave-In. Serial input to the ISD15C00 from the host.
17	V_{CCD}_PWM	I	Digital Power for the PWM Driver.

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Pin Number	Pin Name	I/O	Function
18	SPK+	O	PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state. Or, can be configured as BTL which, together with SPK- pin, provide a differential voltage output. Or, can independently switch to AUDOUT or AUXOUT.
19	V_{SSD}_PWM	I	Digital Ground for the PWM Driver.
20	SPK-	O	PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state. Or, can be configured as BTL which, together with SPK+ pin, provide a differential voltage output. Or, can independently switch to AUDOUT or AUXOUT.
21	V_{CCD}_PWM	I	Digital Power for the PWM Driver.
22	NC		This pin should be left unconnected.
23	NC		This pin should be left unconnected.
24	NC		This pin should be left unconnected.
25	INTB	O	Active low interrupt request pin. This pin is an open-drain output.
26	RDY/BSYB	O	An output pin to report the status of data transfer on the SPI interface. “High” indicates that ISD15C00 is ready to accept new SPI commands or data.
27	RESET	I	Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.)
28	DO	O	Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash.
29	CLK	O	Serial data CLK of the external serial flash interface.
30	GPIO3	I/O	GPIO
31	GPIO2	I/O	GPIO
32	GPIO1	I/O	GPIO
33	NC		This pin should be left unconnected.
34	NC		This pin should be left unconnected.
35	XTALOUT	O	Crystal interface output pin.

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Pin Number	Pin Name	I/O	Function
36	XTALIN	I	The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected.
37	NC		This pin should be left unconnected.
38	GPIO0	I/O	GPIO
39	NC		This pin should be left unconnected.
40	NC		This pin should be left unconnected.
41	AUDOUT	O	Audio Out. This pin can be either a voltage output or a current output configured by the internal registers via SPI command. If AUDOUT is not used, this pin should be left unconnected.
42	AUXOUT	O	Aux Out. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected.
43	V_{CCA}	I	Analog power supply pin.
44	V_{SSA}	I	Analog ground pin.
45	ANAOUT/ MIC-	O	Variable gain analog output with the gain set by feedback resistance to ANAIN. Or, can be configured as MIC- which, together with MIC+, provides a microphone differential input. If ANAIN/ANAOUT is not used, this pin should be left unconnected.
46	ANAIN/ MIC+	I	Variable gain analog input. Or, can be configured as MIC+ which, together with MIC-, provides a microphone differential input. If ANAIN/ANAOUT is not used, this pin should be left unconnected.
47	AUXIN	I	Auxiliary input with the gain set by SPI command If AUXIN is not used, this pin should be left unconnected.
48	NC		This pin should be left unconnected.

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6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature)	-40°C to +85℃
Supply voltage (V_{DD}) [1]	+2.7V to +3.6V
Ground voltage (V_{SS}) [2]	0V
Input voltage (V_{DD}) [1]	0V to 3.6V
Voltage applied to any pins	(V_{SS} –0.3V) to (V_{DD} +0.3V)

NOTES: [1] $V_{DD} = V_{CCA} = V_{CCD} = V_{CCPWM}$

[2] $V_{SS} = V_{SSA} = V_{SSD} = V_{SSPWM}$

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.7		3.6	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3		0.3xV_{DD}	V	
Input High Voltage	V_{IH}	0.7xV_{DD}		V_{DD}	V	
Output Low Voltage	V_{OL}	V_{SS}-0.3		0.3xV_{DD}	V	I_{OL} = 1mA
Output High Voltage	V_{OH}	0.7xV_{DD}		V_{DD}	V	I_{OH} = -1mA
INTB Output Low Voltage	V_{OH1}			0.4	V	
Record Current	I_{DD_Record}			40	mA	V_{DD}= 3.6V, No load, Sampling freq = 16 kHz
Playback Current	$I_{DD_Playback}$			30	mA	
Standby Current	I_{SB}		1	10	µA	V_{DD}= 3.6V
Input Leakage Current	I_{IL}			±1	µA	Force V_{DD}

Notes: [1] Conditions V_{DD}=3V, T_A=25℃ unless otherwise stated

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6.3 AC PARAMETERS

6.3.1 Internal Oscillator

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Internal Oscillator with internal reference	F_{INT}	-10%	2.048 MHz	+10 %	MHz	Vdd = 3V. At room temperature
Internal Oscillator with external resistor [1]	F_{Ext}	-5%	2.048 MHz	+5%	MHz	With 1% precision resistor, 80k-ohm. Vdd = 3V. At room temperature

Notes:
[1] Characterization data shows that frequency deviation is +/- 5% across temperature and voltage ranges.

6.3.2 Inputs

ANAIN & MICIN

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
ANAIN Input Voltage	V_{ANAIN}		10-1000		mV	Peak-to-Peak[2]
ANAIN Feed Back Resistance	$R_{ANA(FB)}$	40		100	KΩ	
MICIN Input Voltage	V_{MICIN}		5-500		mV	Peak-to-Peak[2]

Notes: [1] Conditions V_{DD}=3V, T_{AB}=25℃ unless otherwise stated
[2] Depends on Gain Setting

AUXIN

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
AUXIN Input Voltage	V_{AUXIN}		1000		mV	Peak-to-Peak[2]
Gain from AUXIN to AUXOUT/ANAOUT	$A_{AUXIN\ GAIN}$		0 to 9		dB	4 Gain Steps of 3db each
AUXIN Gain Accuracy	$A_{AUXIN\ (GA)}$	-0.5		+0.5	dB	
AUXIN Input Resistance	R_{AUXIN}		20-40		KΩ	Depending on AUXIN Gain Setting

Notes: [1] Conditions V_{DD}=3V, T_A=25℃ unless otherwise stated.
[2] With 0db Gain setting.

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6.3.3 Outputs

AUXOUT

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SINAD, AUXIN to AUXOUT	$SINAD_{AUXIN_AUXOUT}$		80		dB	Load 5K[2][3]
SINAD, ANAIN to AUXOUT	$SINAD_{ANAIN_AUXOUT}$		80		dB	Load 5K[2][3]
PSRR	$PSRR_{AUXOUT}$		-40		dB	[4]
DC Bias	V_{BIAS_AUXOUT}			1.2	V	
Minimum Load Impedance	$R_{L(AUXOUT)}$	5			KΩ	
Maximum Load Capacitance	$C_{L(AUXOUT)}$			0.1	nF	

Notes:
[1] Conditions V_{DD}=3V, T_A=25℃ unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
[3] All measurements are C-message weighted.
[4] Measured with 1KHz, 100 mVpp sine wave applied to V_{CCA} pins.

AUDOUT

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SINAD, AUXIN to AUDOUT[5]	$SINAD_{AUXIN_AUDOUT}$		80		dB	Load 5K[2][3]
SINAD, ANAIN to AUDOUT[5]	$SINAD_{ANAIN_AUDOUT}$		80		dB	Load 5K[2][3]
PSRR[5]	$PSRR_{AUDOUT}$		-40		dB	[4]
DC Bias[5]	V_{BIAS_AUDOUT}			1.2	V	
Minimum Load Impedance[5]	$R_{L(AUDOUT)}$	5			KΩ	
Maximum Load Capacitance[5]	$C_{L(AUDOUT)}$			0.1	nF	
Output Current [6]	I_{AUDOUT}	0	3	6	mA	[2][6]

Notes:
[1] Conditions V_{cc}=3V, T_A=25℃ unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
[3] All measurements are C-message weighted.
[4] Measured with 1Khz, 100 mVpp sine wave applied to V_{CCA} pins.
[5] Configured as AUDOUT(Voltage Output).
[6] Configured as AUDOUT(Current Output).

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SPEAKER OUTPUTS

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
SNR, AUXIN to SPK+/SPK-	SNR_{AUXIN_SPK}		60		dB	Load 150Ω [2][3]
SNR, ANAIN to SPK+/SPK-	SNR_{ANAIN_SPK}		60		dB	Load 150Ω [2][3]
Output Power	P_{OUT_SPK} VCC=3.0			360	mW	Load 8Ω [2]
THD, AUXIN to SPK+/SPK-	THD %		<1%			Load 8Ω [2]
Minimum Load Impedance	$R_{L(SPK)}$	4	8		Ω	

Notes: [1] Conditions V_{CC}=3V, T_A=25℃ unless otherwise stated.
[2] 1 Vpp 1KHz signal applied at AUXIN/ANAIN with 0db Gain setting.
[3] All measurements are C-message weighted.

6.3.4 SPI Timing

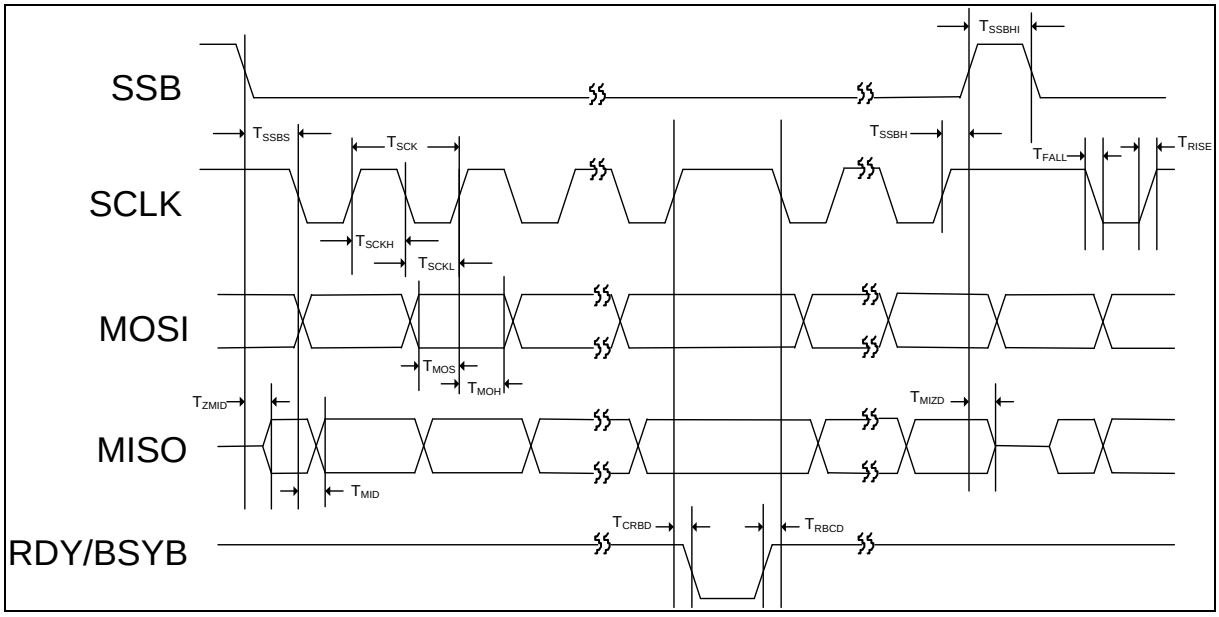

Figure 6-1 SPI Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	60	---	---	ns
T_{SCKH}	SCLK High Pulse Width	25	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns

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SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{SSBS}	SSB Falling Edge to 1st SCLK Falling Edge Setup Time	30	---	---	ns
T_{SSBH}	Last SCLK Rising Edge to SSB Rising Edge Hold Time	30ns	---	50us	---
T_{SSBHI}	SSB High Time between SSB Lows	20	---	---	ns
T_{MOS}	MOSI to SCLK Rising Edge Setup Time	15	---	---	ns
T_{MOH}	SCLK Rising Edge to MOSI Hold Time	15	---	---	ns
T_{ZMID}	Delay Time from SSB Falling Edge to MISO Active	--	--	12	ns
T_{MIZD}	Delay Time from SSB Rising Edge to MISO Tri-state	--	--	12	ns
T_{MID}	Delay Time from SCLK Falling Edge to MISO	---	---	12	ns
T_{CRBD}	Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge	--	--	12	ns
T_{RBCD}	Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge	0	--	--	ns

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6.3.5 I²S Timing

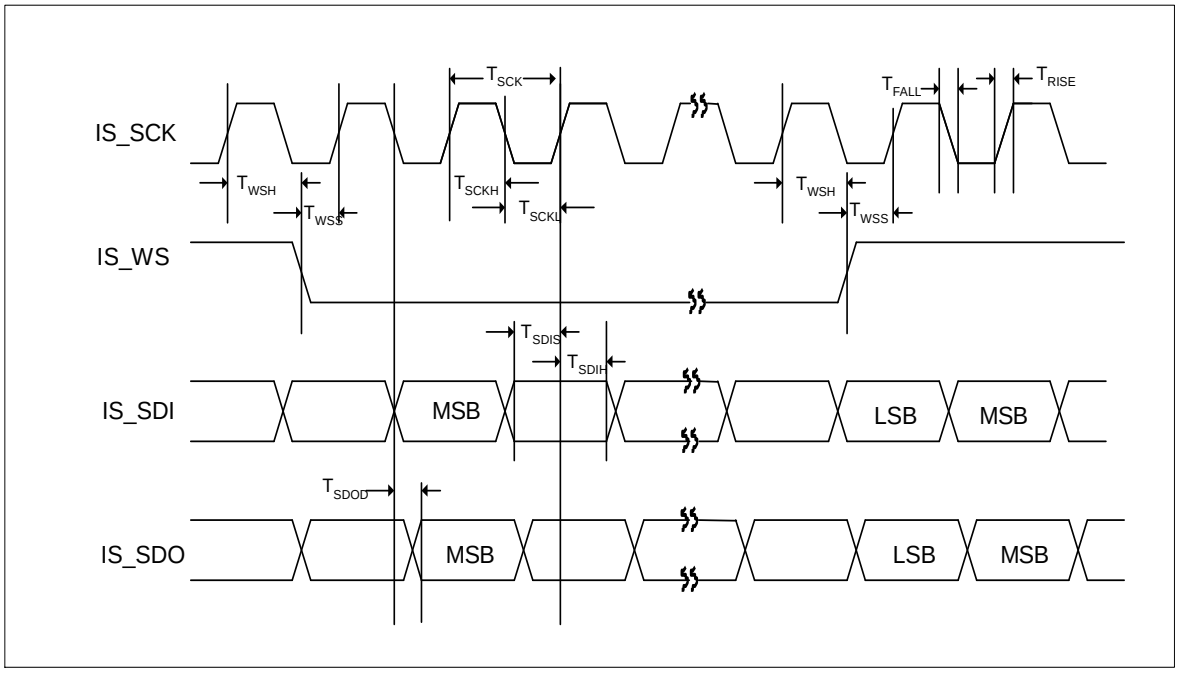

Figure 6-2 I²S Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	IS_SCK Cycle Time	60	---	---	ns
T_{SCKH}	IS_SCK High Pulse Width	25	---	---	ns
T_{SCKL}	IS_SCK Low Pulse Width	25	---	---	ns
T_{RISE}	Rise Time for All Digital Signals	---	---	10	ns
T_{FALL}	Fall Time for All Digital Signals	---	---	10	ns
T_{WSS}	WS to IS_SCK Rising Edge Setup Time	20	---	---	ns
T_{WSH}	IS_SCK Rising Edge to IS_WS Hold Time	20	---	---	ns
T_{SDIS}	IS_SDI to IS_SCK Rising Edge Setup Time	15	---	---	ns
T_{SDIH}	IS_SCK Rising Edge to IS_SDI Hold Time	15	---	---	ns
T_{SDOD}	Delay Time from IS_SCLK Falling Edge to IS_SDO	---	---	12	ns

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7 APPLICATION DIAGRAM

The following applications example is for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

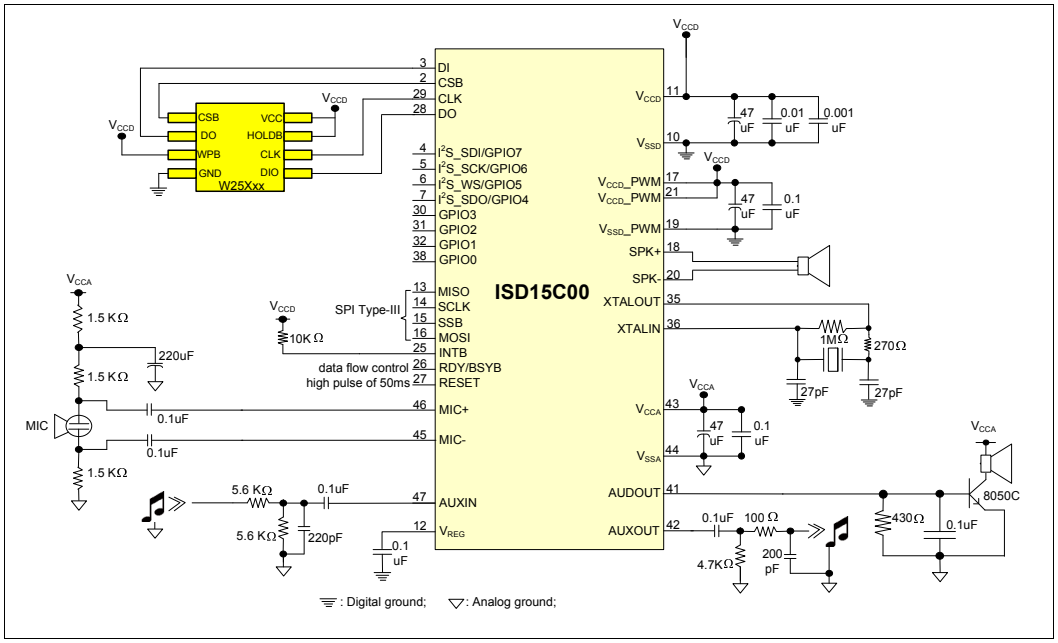

Figure 7-1 ISD15C00 Application Diagram

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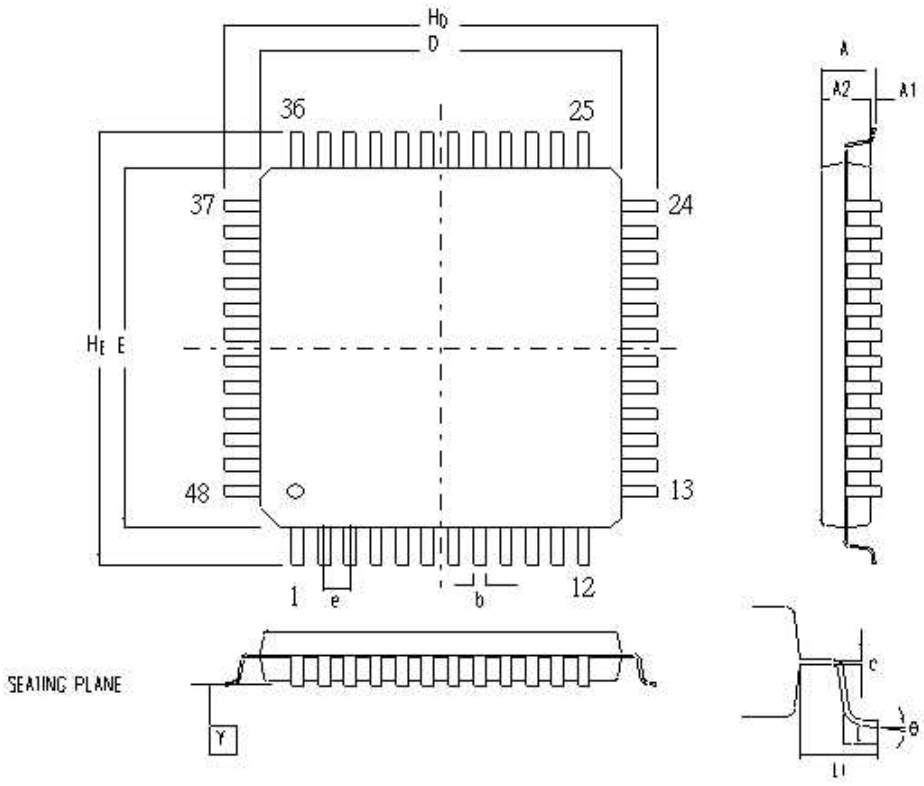
8 PACKAGE SPECIFICATION

8.1 48 LEAD LQFP(7X7X1.4MM FOOTPRINT 2.0MM)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
HD	0.350	0.354	0.358	8.90	9.00	9.10
HE	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

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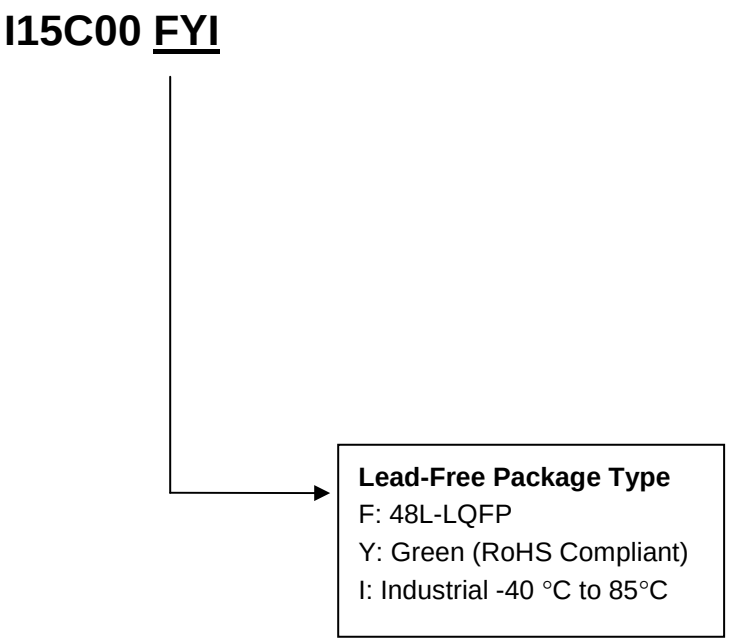
9 ORDERING INFORMATION



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10 REVISION HISTORY

Version	Date	Description
0.71	May 28, 2008	Initial release. • Reset pulse: 50ms. • Add a 270-ohm resistor between XTALOUT and crystal. • Update spec of internal oscillator. • Industrial temp.
0.75	Sep 10, 2008	Update: • SPI timing: T_{SSBH} maximum 50us. • MICIN input signal: 500mV • Revise Block Diagram; add BTL block. • Revise Application Diagram.
0.80	Feb 10, 2009	Update: • Remove the Preliminary watermark. • Output low/high voltage.
0.82	Nov 20, 2009	Update Block Diagram.
1.0	July 1, 2010	Update crystal configuration.

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