October 2006

SLIC-P

Subscriber Line Interface Circuit Enhanced Power Management

SLIC-P (PEB 4266), Version 1.2

Preliminary

Data Sheet

Revision 5.0

Communication Solutions

Never stop thinking

Edition 2006-10-09

Published by
Infineon Technologies AG
81726 München, Germany

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SLIC-P Subscriber Line Interface Circuit Enhanced Power Management

Revision History: 2006-10-09, Revision 5.0

Previous Version: Revision 4.0	
Page	**Subjects (major changes since last revision)**
all	Package P-/PG-VQFN-48-4 changed to PG-VQFN-48-15
all	Package P-/PG-DSO-20-24 changed to PG-DSO-20-24
Page 35	**"Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package" on Page 35** modified.

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1 General Description

The High Voltage Subscriber Line Interface Circuit SLIC-P (PEB 4266) is a reliable interface between the telephone line and the codec devices of the DuSLIC® or VINETIC® chip sets. It is fabricated using Infineon Technologies´ well-proven Smart Power Technology SPT 170.

Due to the integrated triple battery switch, the PEB 4266 enables highly flexible solutions, e.g.

- 2 battery voltages (V_{BATH}, V_{BATL}) for power saving DC line feed and the third one (V_{BATR}) for internal ring signal generation. With V_{BATR} = –150 V, the amplitude of a balanced ringing signal may reach 85 V_{rms}. Besides, unbalanced ringing up to 50 V_{rms} can be chosen on either TIP (ROT) or RING (ROR).
- When using an external ring generator, the three battery voltages allow further reduction of power dissipation due to a still better adaptation of battery voltage to loop length.

The PEB 4266 is designed for a voltage-feeding/current-sensing line interface concept and senses the transversal and longitudinal line current.

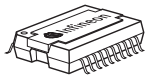
To minimize system power dissipation, a power-down mode can be used; the PEB 4266 is switched off and the line outputs go to a high-impedance mode. Off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

The PEB 4266 is compatible with both 3.3 V and 5 V V_{DD} supplies.

Version 1.2

1.1 Features

- High-voltage line feeding
- 3 Battery voltages (V_{BATL}, V_{BATH}, V_{BATR}) –15 V … –150 V
- Extended V_{DD} voltage range (3.1 V to 5.5 V) supports pure 3.3 V designs
- Long loop driving capability
- Integrated balanced ringing up to 85 Vrms
- Integrated unbalanced ringing up to 50 Vrms
- Support for external ringing
- Sensing of transversal and longitudinal line currents
- Selectable current limitation (60 mA or 90 mA)
- Package options:
  - PG-DSO-20-24
  - PG-VQFN-48-15
- Reliable Smart Power Technology (SPT170)
- Enables high packing densities on board



PG-DSO-20-24

PG-VQFN-48-15

Product Name	Product Type	Package
SLIC-P	PEB 4266 T	PG-DSO-20-24
	PEB 4266 V	PG-VQFN-48-15

1.2 Logic Symbol

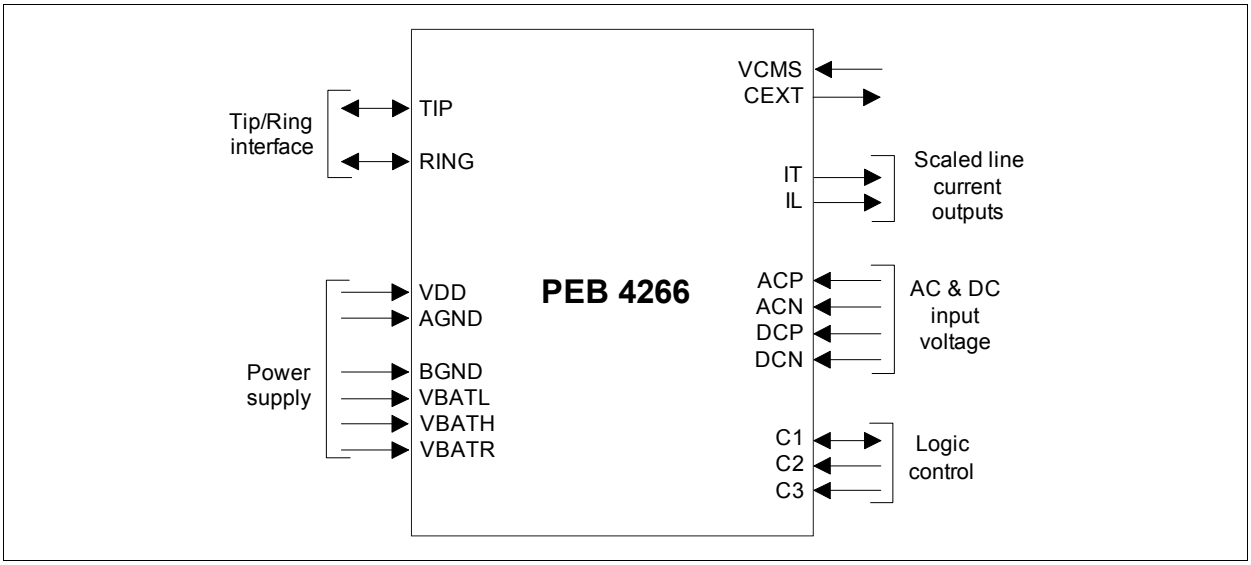


Figure 1 Logic Symbol

1.3 Pin Configuration

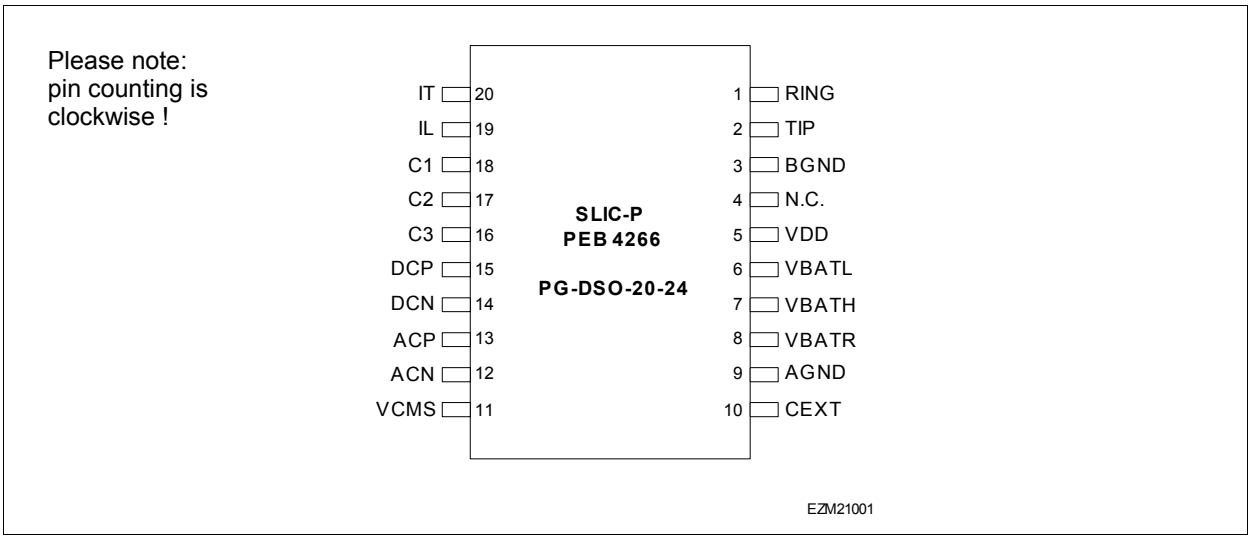


Figure 2 Pin Configuration PG-DSO-20-24 Package (top view)

Note: The PG-DSO-20-24 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).

Attention: The heatsink (see Figure 21) is connected to VBATR via the chip substrate. Due to the high voltage of up to 150 V between VBATR and BGND, touching of the heatsink or any attached conducting part can be hazardous.

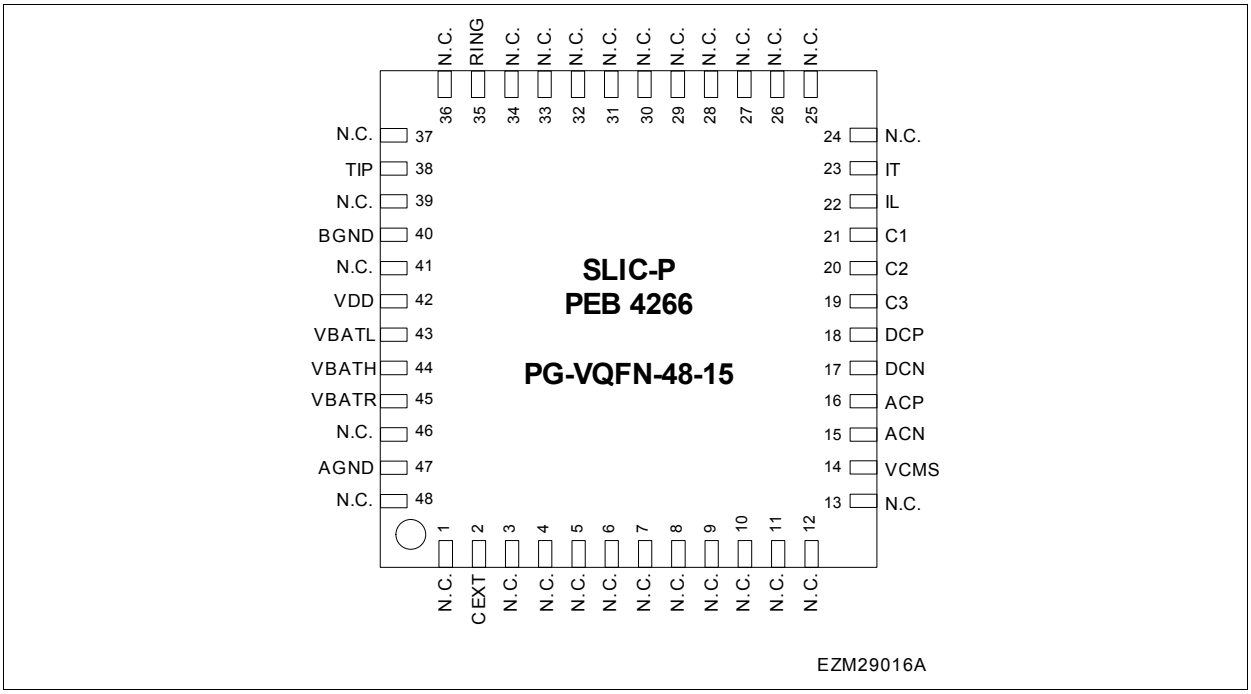


Figure 3 **Pin Configuration PG-VQFN-48-15 Package** (top view)

Attention: The exposed die pad and die pad edges are connected to VBATR via the chip substrate. Due to the high voltage of up to 150 V between VBATR and BGND, touching of the die pad or any attached conducting part can be hazardous.

1.4 Pin Definitions and Functions

1.5 Functional Block Diagram

Table 1 **Pin Definitions and Functions PEB 4266**

Pin No. PG-DSO-20-24	Pin No. PG-VQFN-48-15	Name	Pin Type	Function
1	35	RING	I/O	Subscriber loop connection RING
2	38	TIP	I/O	Subscriber loop connection TIP
3	40	BGND	Power	Battery ground: reference for TIP, RING, V_{BATH}, V_{BATL} and V_{BATR}
5	42	V_{DD}	Power	Positive supply voltage (3.1 V ≤ V_{DD} ≤ 5.5 V), referred to AGND
6	43	V_{BATL}	Power	Negative battery supply voltage (–15 V ≥ V_{BATL} ≥ –140 V)
7	44	V_{BATH}	Power	Negative battery supply voltage (–20 V ≥ V_{BATH} ≥ –145 V, V_{BATL} ≥ V_{BATH})

Table 1 Pin Definitions and Functions PEB 4266 (cont'd)

Pin No. PG-DSO-20-24	Pin No. PG-VQFN-48-15	Name	Pin Type	Function
8	45	V_{BATR}	Power	Negative battery supply voltage used for ringing or on-hook (–25 V ≥ V_{BATR} ≥ –150 V; V_{BATL} ≥ V_{BATH} ≥ V_{BATR})
9	47	AGND	Power	Analog ground: V_{DD} and all signal and control pins with the exception of TIP and RING refer to AGND
10	2	CEXT	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance 60 kΩ)
11	14	VCMS	I	Reference voltage (1.5 V) for differential two wire interface
12, 13	15, 16	ACN, ACP	I	Differential two-wire AC input voltage; at TIP/RING outputs multiplied by –6 and related to $V_{BI}/2$[1)]
14, 15	17, 18	DCN, DCP	I	Differential two-wire DC input voltage; at TIP/RING outputs multiplied by –30 (ACTH and ACTL mode) or –60 (ACTR mode) and related to $V_{BI}/2$[1)]
16	19	C3	I	Binary logic input, controlling the operation mode. Must be connected to – IO2A/B of SLICOFI®-2 or IO0A/B of VINETIC®, when two supply voltages for voice transmission and internal ringing are used. – GND, when three supply voltages for voice transmission and external ringing are used.
17	20	C2	I	Ternary logic input, controlling the operation mode
18	21	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C), this pin sinks a current of typically 150 µA.
19	22	IL	O	Current output: longitudinal line current scaled down by a factor of 100.
20	23	IT	O	Current output: transversal line current scaled down by a factor of 50.
4	[2)]	N.C.		Not connected

1) V_{BI} is the output voltage of the battery switch (see **Figure 4**)

2) For the PG-VQFN-48-15 package the following pins are not connected: 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 36, 37, 39, 41, 46, 48

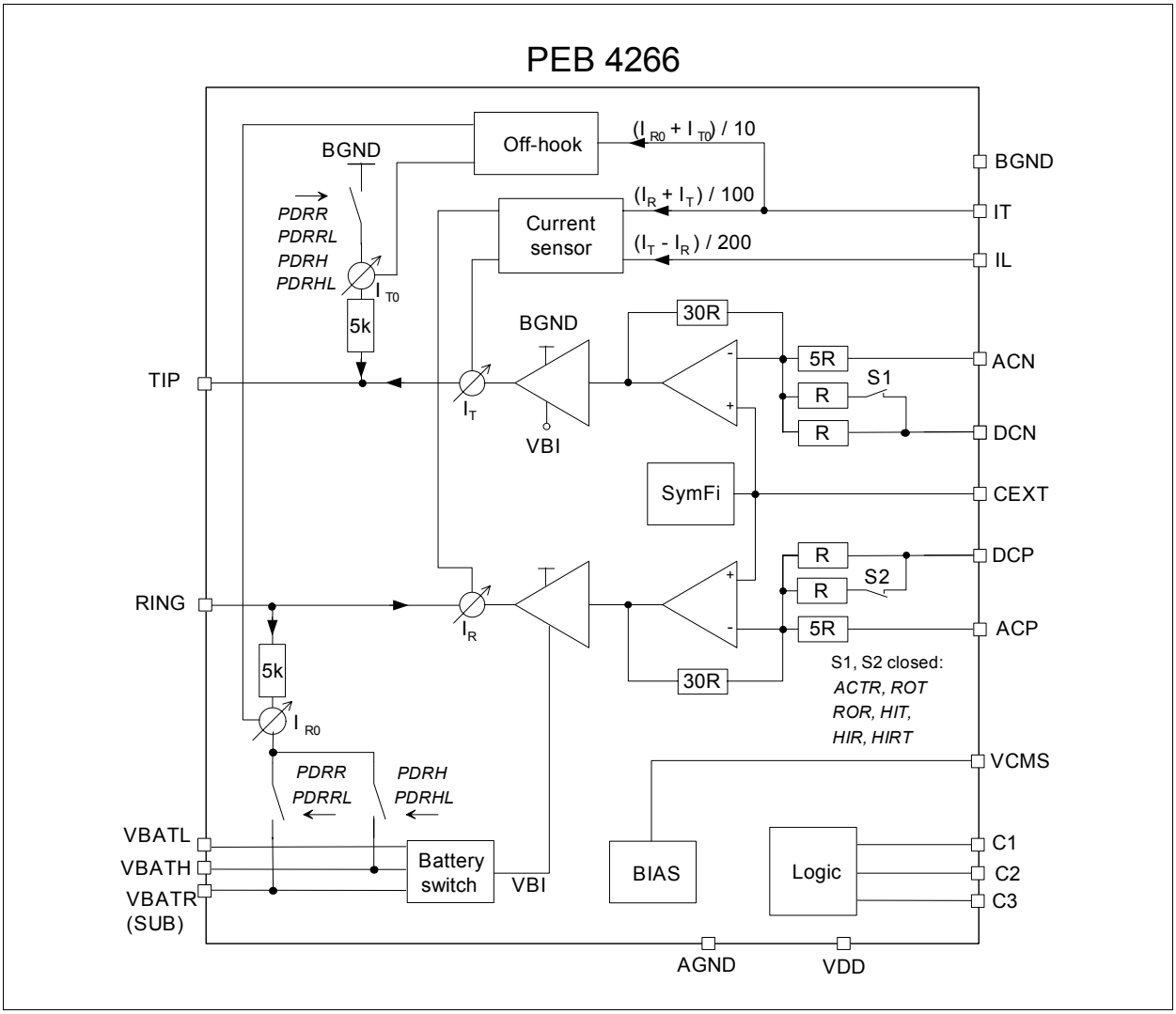


Figure 4 Block Diagram

2 Functional Description

The SLIC-P supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} and the longitudinal current I_{Long} (**Figure 5**).

In receive direction DC and AC voltages are handled separately with different gains on the PEB 4266. Both are applied differentially via pins DCP and DCN or ACP and ACN, respectively.

The line voltages V_R and V_T are the amplified input voltages, related to the mean supply voltage $V_M = V_{BI}/2$. In the active modes ACTH with $V_M = V_{BATH}/2$ and ACTL with $V_M = V_{BATL}/2$, the line voltages are given by

$$V_T = V_{TIP} = V_M - 30 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 30 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS}),$$

and in ringing mode ACTR with $V_M = V_{BATR}/2$,

$$V_T = V_{TIP} = V_M - 60 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 60 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

The transversal line voltage $V_{TR} = V_T - V_R$ thus is simply related to the input voltages:

$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$

$= 30 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ for modes ACTL, ACTH

$= 60 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ for mode ACTR

A reversed polarity of V_{TR} is easily obtained by changing the sign of $(V_{DCP} - V_{DCN})$.

In transmit direction the transversal and longitudinal currents are measured and scaled images are provided at the IT and IL pin, respectively.

$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$	$I_{IL} = (I_T - I_R)/200 = I_{Long}/100$
$I_{Trans} = (I_T + I_R)/2$	$I_{Long} = (I_T - I_R)/2$

For off-hook detection, in PDRH or PDRR mode 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH or VBATR, respectively.

The currents through these resistors, I_{T0} and I_{R0}, are sensed, scaled and provided at the IT pin (see **Figure 4**):

$I_{IT0} = (I_{T0} + I_{R0})/10 = I_{TRANS0}/5$

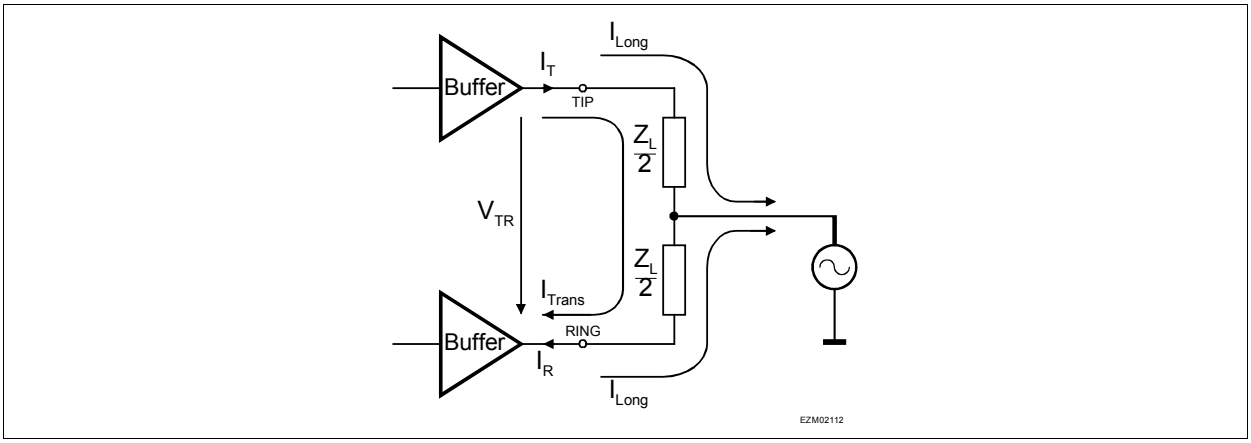


Figure 5 Definition of Output Current Directions

2.1 Operating Modes

The SLIC-P (PEB 4266) operates in the following modes controlled by ternary logic signals at C1, C2 and a binary signal at C3:

Table 2 SLIC-P Interface Code

		C2				
		L	**M**	**H**		
C1	**L**[1]	PDH	PDRR	PDRRL	**L**	**C3**[2]
			PDRHL	PDRH	**H**	
	M	$ACTL_{90}$[3]	$ACTH_{90}$	$ACTR_{90}$	**L**	
		$ACTL_{60}$	$ACTH_{60}$	$ACTR_{60}$	**H**	
	H	HIRT	HIT	HIR	**L**	
			ROT	ROR	**H**	

1) No 'Overtemp' signaling possible via pin C1 if C1 is low.
2) When used with the DuSLIC® chip set, the C3 pin of SLIC-P is typically connected to IO2 pin of SLICOFI®-2. When used with the VINETIC® chip set, the C3 pin of SLIC-P is typically connected to IO0 pin of VINETIC®.
3) SLIC-P Version 1.2 features selectable current limitation (60 mA or 90 mA) in the Active and Ringing operating modes. In this document ACTL, ACTH and ACTR refers to both current limitation values.

Table 3 SLIC-P Modes

SLIC-P Mode	Mode Description	Internal Battery Supply Voltage
PDH	Power Down High Impedance	V_{BATH}
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Resistive High Load	V_{BATH}
PDRR	Power Down Resistive Ring	V_{BATR}
PDRRL	Power Down Resistive Ring Load	V_{BATR}
$ACTL_{90}$, $ACTL_{60}$	Active Low with Current Limitation 90 mA or 60 mA	V_{BATL}
$ACTH_{90}$, $ACTH_{60}$	Active High with Current Limitation 90 mA or 60 mA	V_{BATH}
$ACTR_{90}$, $ACTR_{60}$	Active Ring with Current Limitation 90 mA or 60 mA	V_{BATR}

Table 3 SLIC-P Modes (cont'd)

SLIC-P Mode	Mode Description	Internal Battery Supply Voltage
HIRT	High Impedance on RING and TIP	V_{BATR}
HIT	High Impedance on TIP (RING current limitation of 90 mA)	V_{BATR}
HIR	High Impedance on RING (TIP current limitation of 90 mA)	V_{BATR}
ROR	Ring on RING (current limitation 60 mA)	V_{BATR}
ROT	Ring on TIP (current limitation 60 mA)	V_{BATR}

Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

Power Down Resistive (PDRH, PDRR)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, Power Down Resistive provides a connection of 5 kΩ resistors from TIP to BGND and RING to either VBATH (PDRH) or VBATR (PDRR), while the output buffers show high impedance (see Figure 4). The current through these resistors is sensed and transferred to the IT pin for off-hook supervision.

Power Down Resistive Load (PDRHL, PDRRL)

PDRHL (PDRRL) is used as a transition state when the operating mode is changed from PDRH (PDRR) to ACTH (automatically initiated by the codec). It causes fast preloading of C_{EXT} in order to suppress line voltage transients.

Active Low ($ACTL_{90}$, $ACTL_{60}$), Active High ($ACTH_{90}$, $ACTH_{60}$)

These are the regular transmission modes for voiceband. The line-driving section is operated between V_{BATL} or V_{BATH} and BGND. By means of pin C3, current limitations can be chosen to be either 90 mA or 60 mA.

Active Ring ($ACTR_{90}$, $ACTR_{60}$)

This mode can be used for balanced ringing up to 85 V_{rms} or as a third voice transmission mode (in applications with external ringing).

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer can still be measured by IT or IL. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

Ring on Tip (ROT)

An unbalanced ring signal up to 50 V_{rms} can be fed to the Tip line. The Ring line is fixed to a potential near BGND.

Ring on Ring (ROR)

An unbalanced ring signal up to 50 V_{rms} can be fed to the Ring line. The Tip line is fixed to a potential near BGND.

2.2 Current Limitation / Overtemperature

According to the application requirements the output current limit for SLIC-P can be selected by C3 (see **Table 2**). With C3 = L, the total current delivered by the output drivers is limited to typically 90 mA in operating modes ACTL, ACTH, ACTR, HIT and HIR. C3 = H sets this limitation to typically 60 mA in operating modes ACTL, ACTH, ACTR, ROT and ROR.

If, however, the junction temperature exceeds 165 °C, the current limit is further reduced to keep the junction temperature constant.

Simultaneously, pin C1 sinks a signalling current I_{therm}.

3 Typical Application Circuit for DuSLIC® and VINETIC®

Figure 6 (**Figure 7**) shows one channel of an application including SLIC-P and SLICOFI®-2/-2S or VINETIC®-4VIP/-4M (please refer to the latest DuSLIC® and VINETIC® Data Sheets). In **Table 4** the external passive components for a dual-channel solution according to **Figure 6** and **Figure 7** are listed.

Table 4 External Components DuSLIC® / VINETIC® for 2 Channels

Qu.	Symbol	Value	Unit	Relat.Tol.	Rating	DuSLIC®	VINETIC®
2	R_{IT1}	470	Ω	1 %		x	
2	R_{IT1}	510	Ω	1 %			x
2	R_{IT2}	680	Ω	1 %		x	x
2	R_{IL}	1.6	kΩ	1 %		x	x
4	R_{STAB}	30 (typ.)	Ω	1 %[1)]		x	x
4	R_{PROT}[2)]	20 ... 50	Ω	1 %[1)]		x	x
4	C_{STAB}	15 (typ.)	nF	10 %	150 V	x	x
2	C_N[3)]	100	pF	10 %	150 V		
2	C_{DC}	120	nF	10 %	10 V	x	
2	C_{DC}	220	nF	10 %	10 V		x
2	C_{ITAC}	680	nF	10 %	10 V	x	
2	C_{ITAC}	1	µF	10 %	10 V		x
1	C_{PRE}[4)]	18	nF	5 %	10 V		x
2	C_{VCMIT}	680	nF	10 %	10 V	x	
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	470	nF	20 %	10 V	x	x
7	C_1	typ. 100	nF	10 %	10 V	x	
13	C_1	typ. 100	nF	10 %	10 V		x
6	C_2	typ. 100	nF	10 %	150 V	x	x
1	C_3	4.7	µF	20 %	10 V, Tantal	x	
2	D_1	BAS 21	–	–	–	x	x
4	D_2	BAS 21	–	–	–	x	x
2	U_1[2)]	Overvoltage Protection	–	–	–	x	x

1) Dependent on longitudinal balance requirements (for details see **[2]**).
2) See **[1]**.
3) Optional EMC filter, recommended in noisy environment (WLAN)
4) C_{PRE} is only necessary when TTX (12 or 16 kHz metering) is used.

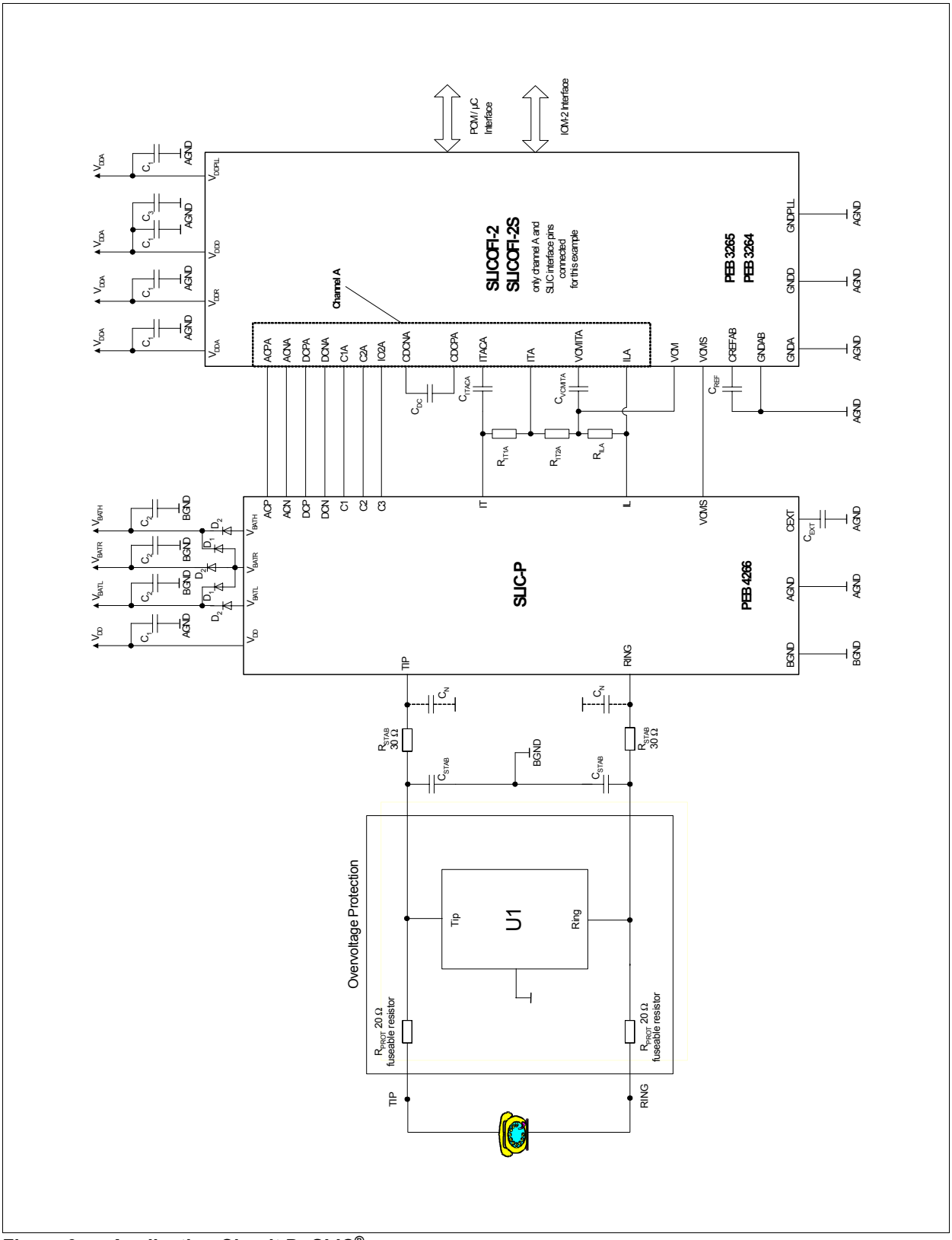


Figure 6 Application Circuit DuSLIC®

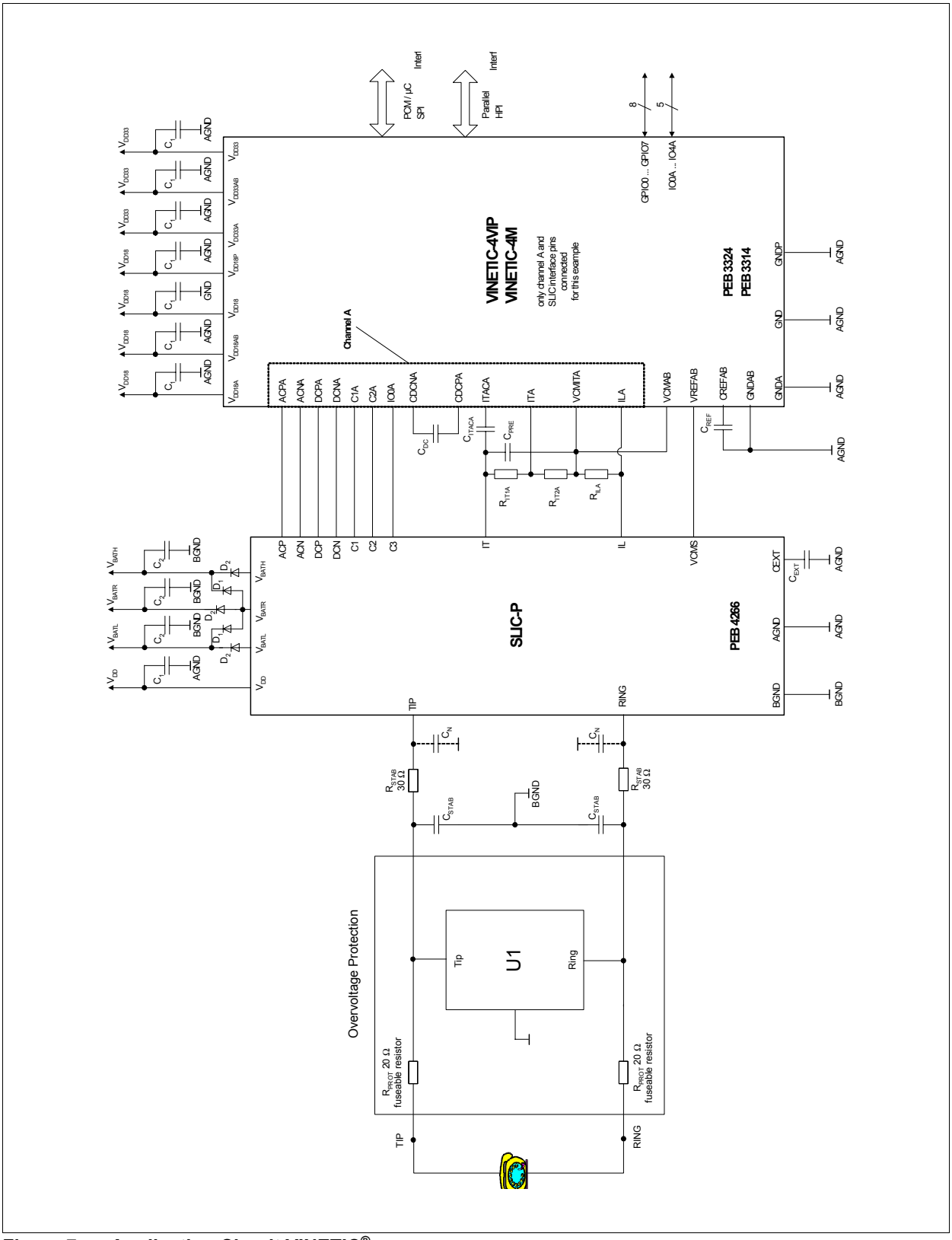


Figure 7 Application Circuit VINETIC®

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage low	V_{BATL}	V_{BATH} - 5	–	0.4	V	Referred to BGND
Battery voltage high	V_{BATH}	V_{BATR} - 0.4	–	0.4	V	Referred to BGND
Battery voltage R	V_{BATR}	–155	–	0.4	V	Referred to BGND
Battery voltage difference	$V_{BATL} - V_{BATR}$, $V_{BATH} - V_{BATR}$	–0.4	–	–	V	–
Total battery supply voltage, continuous	$V_{DD} - V_{BATR}$	–	–	160	V	–
V_{DD} supply voltage	V_{DD}	–0.4	–	7	V	Referred to AGND
Ground voltage difference BGND, AGND	–	–0.4	–	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{CMS}, V_{C1}, V_{C2}, V_{C3}	–0.4	–	V_{DD} + 0.4	V	Referred to AGND
Voltages on current outputs	V_{IT}, V_{IL}	–0.4	–	V_{DD} + 0.4	V	Referred to AGND
Junction temperature	T_j	–	–	150	°C	
ESD voltage, all pins	–	–	–	1	kV	SDM (Socketed Device Model)[1)]

1) EOS/ESD Assn. Standard DS5.3-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Foreign Line Voltages

External voltages applied at the line outputs TIP/RING may cause current flow in the PEB 4266. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, because overtemperature protection cannot react fast enough at high local power density. The value of allowed power dissipation strongly depends on its duration. It can be expressed in terms of voltage and current limits directly at the TIP/RING output pins.

Table 6 Voltage Limits on Output Pins

Duration of Voltage	Pins	Min. Voltage [V]	Max. Voltage [V]
Continuous	TIP, RING	V_{BATR} – 0.4	V_{DD} + 5
< 100 µs	TIP, RING	V_{BATR} – 10	V_{DD} + 20
< 1 µs	TIP, RING	V_{BATR} – 15	V_{DD} + 30

Table 7 Current Limits on Output Pins

Duration of Current	Pins	Min. current [A]	Max. current [A]
Continuous	TIP, RING	– 0.1	0.1
< 100 µs	TIP, RING	– 1.0	1.0
< 1 µs	TIP, RING	– 1.5	1.5

The above limits (**Table 6** and **Table 7**) have to be regarded as typical. Both voltage and current limits are valid simultaneously. Together with external circuitry they determine protection requirements (see **[2]**).

4.3 Operating Range

Table 8 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Battery voltage L[1)]	V_{BATL}	V_{BATH}	–	–15	V	Referred to BGND
Battery voltage H[1)]	V_{BATH}	V_{BATR}	–	–20	V	Referred to BGND
Battery voltage R[1)]	V_{BATR}	–150	–	–20	V	Referred to BGND
Total battery supply voltage	$V_{DD} - V_{BATR}$	–	–	155	V	–
V_{DD} supply voltage	V_{DD}	3.1	–	5.5	V	Referred to AGND
Ground voltage difference	$V_{BGND} - V_{AGND}$	–0.4	–	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	–	V_{DD} - 0.6[2)]	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	–	3.3	V	Referred to AGND
Junction temperature	T_j	–	–	125[3)]	°C	–
Ambient temperature	T_A	–40	–	+ 85	°C	–

1) If only two battery voltages are used, pins VBATL and VBATH should be connected externally.
2) The voltage limitation at IT imposes restrictions on the line current sensing range in reverse polarity; for further details please refer to **[4]**.
3) Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

4.4 Thermal Resistances

Table 9 Thermal Resistances

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Junction to case	$R_{th, jC}$	–	2	–	K/W	PG-DSO-20-24, PG-VQFN-48-15
Junction to ambient	$R_{th, jA}$	–	50	–	K/W	PG-DSO-20-24, without heatsink
		–	20	–	K/W	PG-DSO-20-24, with heatsink
Junction to ambient	$R_{th, jA}$	–	25	–	K/W	PG-VQFN-48-15, 4-layer JEDEC PCB with vias, die pad soldered to PCB (footprint see **Chapter 6.2.1**)

4.5 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at V_{BATH} = –48 V, V_{BATL} = –24 V, V_{BATR} = –80 V and V_{DD} = +3.3 V.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extended temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

4.5.1 Supply Currents and Power Dissipation

Table 10 Supply Currents, Power Dissipation (I_R = I_T = 0)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Power Down High Impedance, Power Down Resistive Ring, Power Down Resistive High							
V_{DD} current	I_{DD}	–	140	200	µA	PDx	1
V_{BATH} current	I_{BATH}	–	0	10	µA	PDH, PDRR	2
		–	60	120	µA	PDRH	3
V_{BATL} current	I_{BATL}	–	0	10	µA	PDx	4
V_{BATR} current	I_{BATR}	–	100	150	µA	PDH, PDRR	5
		–	30	60	µA	PDRH	6
Active Low							
V_{DD} current	I_{DD}	–	0.8	1.1	mA	ACTL	7
V_{BATH} current	I_{BATH}	–	5	15	µA	ACTL	8
V_{BATL} current[1)]	I_{BATL}	–	1.7	2.2	mA	ACTL	9
V_{BATR} current	I_{BATR}	–	10	25	µA	ACTL	10
Active High							
V_{DD} current	I_{DD}	–	0.8	1.1	mA	ACTH	11
V_{BATH} current	I_{BATH}	–	2.1	2.7	mA	ACTH	12
V_{BATL} current	I_{BATL}	–	0	10	µA	ACTH	13
V_{BATR} current	I_{BATR}	–	10	25	µA	ACTH	14
Active Ring							
V_{DD} current	I_{DD}	–	0.8	1.1	mA	ACTR	15
V_{BATH} current	I_{BATH}	–	0	10	µA	ACTR	16
V_{BATL} current	I_{BATL}	–	0	10	µA	ACTR	17
V_{BATR} current[1)]	I_{BATR}	–	2.7	3.5	mA	ACTR	18
High Impedance on RING, High Impedance on TIP, Ring on RING, Ring on TIP							
V_{DD} current	I_{DD}	–	0.7	0.9	mA	HIR, HIT, ROR, ROT	19
V_{BATH} current	I_{BATH}	–	0	10	µA	HIR, HIT, ROR, ROT	20
V_{BATL} current	I_{BATL}	–	0	10	µA	HIR, HIT, ROR, ROT	21
V_{BATR} current	I_{BATR}	–	2.2	2.9	mA	HIR, HIT, ROR, ROT	22

Table 10 Supply Currents, Power Dissipation ($I_R = I_T = 0$) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
High Impedance on RING and TIP							
V_{DD} current	I_{DD}	–	0.5	0.8	mA	HIRT	23
V_{BATH} current	I_{BATH}	–	0	10	µA	HIRT	24
V_{BATL} current	I_{BATL}	–	0	10	µA	HIRT	25
V_{BATR} current	I_{BATR}	–	1.7	2.4	mA	HIRT	26

1) Current depending on supply voltage (see **Table 11**)

The total power dissipated in the SLIC consists of the quiescent power P_Q due to the supply currents and the output stage power P_O caused by any line current I_{TRANS} (see **Table 12**),

$P_{tot} = P_Q + P_O$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATR}| \times I_{BATR} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL}$

The supply currents I_{BATL} , I_{BATH} and I_{HR} are dependent on the respective supply voltages. They can be calculated from the specified values I_{BATL} (-24 V), I_{BATH} (-48 V) and I_{BATR} (-80 V) by the formulas in **Table 11**.

Table 11 Voltage Dependence of Supply Currents

Operating Mode	Equation for I Calculation
ACTL	I_{BATL} (V_{BATL}) = I_{BATL} (-24 V) + (IV_{BATL}I - 24) / 60 kΩ
ACTH	I_{BATH} ($V_{BATH)}$ = I_{BATH} (-48 V) + (IV_{BATH}I - 48) / 60 kΩ
ACTR	I_{BATR} (V_{BATR}) = I_{BATR} (-80 V) + (IV_{BATR}I - 80) / 60 kΩ

Table 12 Output Stage Power Dissipation

Operating Mode	Equation for P_O Calculation
ACTL	$P_O = (1.05 \times \lvert V_{BATL}\rvert - V_{TR}) \times I_{Trans}$
ACTH	$P_O = (1.05 \times \lvert V_{BATH}\rvert - V_{TR}) \times I_{Trans}$
ACTR	$P_O = (1.05 \times \lvert V_{BATR}\rvert - V_{TR}) \times I_{Trans}$ (ohmic load) $P_O = [4 \times V_{BATR} - \pi \times V_P \times \cos \varphi] \times V_P / (2 \times \pi \times Z_L)$ (complex load $Z = Z_L e^{i\varphi}$, V_P ... peak ring voltage)

4.5.2 DC Characteristics

Table 13 DC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Line Termination TIP, RING							
DC line voltage	$V_{TR, DC}$	–0.4	0	0.4	V	$V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} =$ 1.5 V Modes: ACTx	27
		23.5	24	24.5	V	$V_{DCP} - V_{DCN} = 0.8$ V, Mode: ACTH	28
		–24.5	–24	–23.5	V	$V_{DCP} - V_{DCN} = -0.8$ V, Mode: ACTH	29
	$V_{TIP, DC}$	–13	–12	–11	V	Mode: ACTL	30
		–25	–24	–23	V	Mode: ACTH	31
		–41	–40	–39	V	Mode: ACTR	32
DC line voltage drop (see **Figure 8**)	$-V_{BATH} - V_{TR, max}$	–	2	3	V	$I_{Trans} = 20$ mA, $V_{DCP} - V_{DCN} = 2.5$ V Mode: ACTH	33
Output current limit (see **Figure 13**)	$\|I_{R, max}\|$, $\|I_{T, max}\|$	70	90	110	mA	C3 = L, Mode: ACTx	34
	$\|I_{T, max}\|$	70	90	110	mA	Mode: HIR	35
	$\|I_{R, max}\|$	70	90	110	mA	Mode: HIT	36
	$\|I_{R, max}\|$, $\|I_{T, max}\|$	48	60	75	mA	C3 = H, Mode: ACTx	37
	$\|I_{T, max}\|$	48	60	75	mA	Mode: ROT	38
	$\|I_{R, max}\|$	48	60	75	mA	Mode: ROR	39
Open loop resistance TIP to V_{BGND} (see **Figure 14**)	R_{TG}	4.25	5.0	6.0	kΩ	$I_T = 2$ mA, Temp = 25 °C[1)], Mode: PDRH	40
Open loop resistance RING to V_{BATH} (see **Figure 14**)	R_{RB}	4.25	5.0	6.0	kΩ	$I_R = 2$ mA, Temp = 25 °C[1)], Mode: PDRH	41
Open loop line voltage	V_{TR}	–	47	–	V	Mode: PDRH	42
Power down output leakage current	$I_{Leak,R}$	–30	–	30	µA	$V_{BATR} < V_R < V_{DD}$, Mode: PDH	43
	$I_{Leak,T}$	–30	–	30	µA	$V_{BATR} < V_T < V_{DD}$, Mode: PDH	44
High impedance output leakage current	$I_{Leak,R}$	–30	–	30	µA	$V_{BATR} < V_R < V_{DD}$, Mode: HIR, HIRT	45
	$I_{Leak,T}$	–30	–	30	µA	$V_{BATR} < V_T < V_{DD}$, Mode: HIT, HIRT	46

Table 13 DC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Inputs DCP, DCN, ACP, ACN, VCMS							
Input resistance	R_{DC}	–	1	–	kΩ	Mode: ACTR, HIx	47
DCP, DCN		–	2.5	–	kΩ	Mode: all other	48
Input resistance ACP, ACN	R_{AC}	–	12.5	–	kΩ	Mode: all	49
Output resistance on C_{EXT}		–	60	–	kΩ	Mode: all	50
Current Outputs IT, IL							
IT output current (see **Figure 15**)	I_{IT}	–15	0	15	µA	$I_R = I_T = 0$ mA, Mode: ACTx	51
		380	400	420	µA	$I_R = I_T = 20$ mA, Mode: ACTx	52
		–420	–400	–380	µA	$I_R = I_T = –20$ mA, Mode: ACTx	53
Transversal current ratio (guaranteed by design)	$1/G_{IT,DC}$ 2)	49.5	50	50.5	–	$I_R = I_T = 20$ mA, $I_R = I_T = –20$ mA, Mode: ACTx	54
Off-hook output current on IT	–	750	900	1050	µA	TIP/RING shorted, $V_{BATH} = –48$ V Temp = 25 °C 3), Mode: PDRH	55
		1300	1500	1700	µA	$V_{BATR} = –80$ V Temp = 25 °C 3), Mode: PDRR	56
IL output current (see **Figure 15**)	I_{IL}	–20	0	20	µA	$I_R = I_T = 20$ mA, Mode: ACTx	57
		30	50	70	µA	$I_R = 15$ mA, $I_T = 25$ mA, Mode: ACTx	58
		–160	–125	–90	µA	$I_R = 62.5$ mA, $I_T = 37.5$ mA, Mode: ACTx	59
Control Inputs C1, C2, C3							
H-input voltage	V_{IH}	2.7	–	V_{DD} + 0.3	V	Mode: all	60
M-input voltage	V_{IM}	1.2	–	2.1	V	C1, C2	61
L-input voltage	V_{IL}	–0.3	–	0.6	V	Mode: all	62
Input leakage current	I_{Leak}	–5	0	5	µA	Mode: all	63
Thermal overload current C1	I_{therm}	120	150	250	µA	$V_{C1} > 1.20$ V, Mode: ACTx, HIx	64
Thermal overload threshold temperature	T_{jLIM}	–	165	–	°C	Mode: ACTx, HIx	65

1) The systematic temperature dependence is + 0.1 %/°C.
2) The offset ($I_R = I_T = 0$ mA) has to be taken into account.
3) The systematic temperature dependence is - 0.1 % / °C.

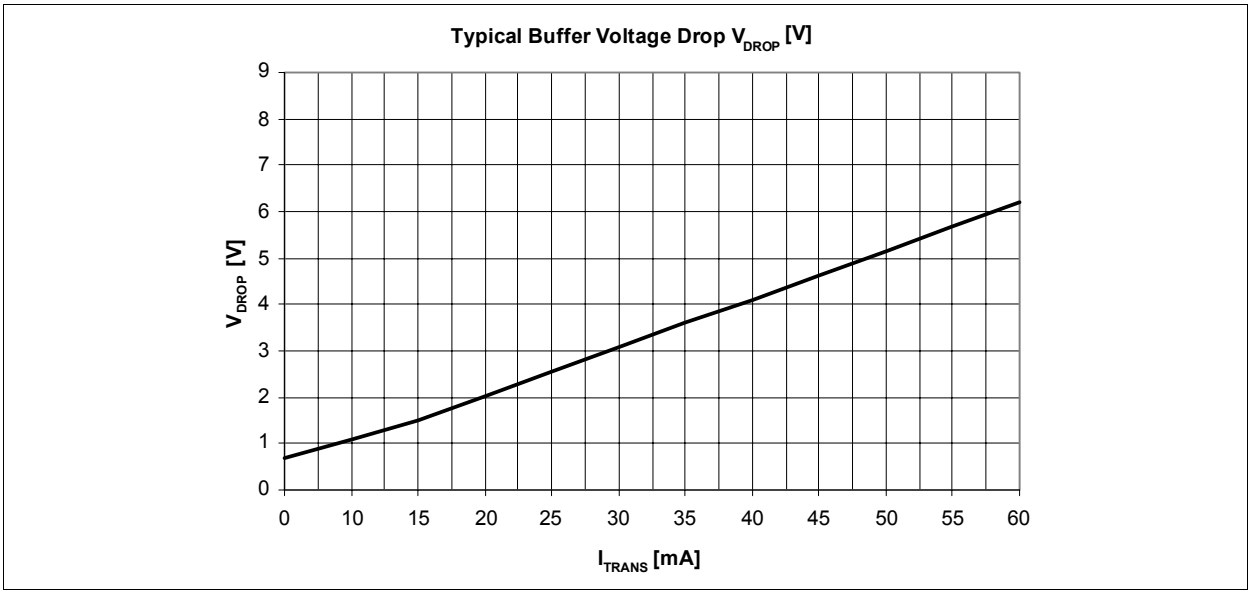


Figure 8 Typical Buffer Voltage Drop in all Operating Modes

4.5.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 14 AC Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Line Termination TIP, RING							
Receive gain (see **Figure 16**)	G_r	5.925	6.0	6.075	–	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	66
Total harmonic distortion V_{TR} (see **Figure 16**)	THD	–	0.03	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	67
Teletax distortion	$THDTTX$	–	0.1	1	%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω	68
		–	1	3	%	$V_{TR,AC}$ = 5 V_{rms}, f = 16 kHz, R_L = 200 Ω, $I_{Trans,DC}$ = 0 mA	69
Psophometric noise (see **Figure 16**)	N_{pVTR}	–	–80	–76	dBmp	–	70
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (see **Figure 17**)	$LTRR$	60	70	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz	71
Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) (see **Figure 18**)	$LTRR\text{-}loop$	54	58	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 1 kHz	72
		52	56	–	dB	3.4 kHz	73

Table 14 AC Characteristics (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	No.
		Min.	Typ.	Max.			
Transversal to longitudinal rejection ratio V_{TR}/V_{long}(see **Figure 19**)	$TLRR$	48	58	–	dB	$V_{ACP} - V_{ACN}$ = 1920 mV_{rms}, 300 Hz < f < 3.4 kHz	74
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mVp, 300 Hz < f < 3.4 kHz	
V_{BATL}/V_{TR}		40	60	–	dB	Mode: ACTL	75
V_{BATH}/V_{TR}		40	60	–	dB	Mode: ACTH	76
V_{BATR}/V_{TR}		33	50	–	dB	Mode: ACTR	77
V_{DD}/V_{TR}(see **Figure 9**,		40	60	–	dB	Mode: ACTL, ACTH	78
Figure 10, **Figure 11**, **Figure 12**)		30	40	–	dB	Mode: ACTR	79
Ringing amplitude TIP/RING	V_{RNG0}	–	85	–	V_{rms}	$V_{DCP} - V_{DCN}$ = 0.15 V (DC) + 1.42 V_{rms} (sine wave),	80
Ringing distortion (see **Figure 20**)	RD	–	0.1	2	%	R_R = 450 Ω, C_R = 3.4 µF, f = 20 Hz, Mode: ACTR	81
Transversal Current IT							
Transversal current ratio (see **Figure 16**)	$1/G_{it}$					$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz,	
		49.5	50	50.5	–	$I_{Trans,DC}$ = 25 mA	82
		49	50	51	–	$I_{Trans,DC}$ = –25 mA	83
Total harmonic distortion V_{IT}	THD_{IT}	–	0.02	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mV_{rms}, f = 1015 Hz	84
Psophometric noise (see **Figure 16**)	N_{pVIT}	–	–110	–105	dBmp	–	85
Longitudinal to transversal current output rejection ratio V_{long}/V_{IT} (see **Figure 17**)	$LITRR$	78	–	–	dB	V_{long} = 3 V_{rms}, 300 Hz < f < 3.4 kHz	86
Power supply rejection ratio	$PSRR$					$V_{SupplyAC}$ = 100 mV_p, 300 Hz < f < 3.4 kHz	
V_{DD}/V_{IT}		50	70	–	dB		87
V_{BATL}/V_{IT}		50	70	–	dB		88
V_{BATH}/V_{IT}		50	70	–	dB		89
V_{BATR}/V_{IT}		50	70	–	dB		90

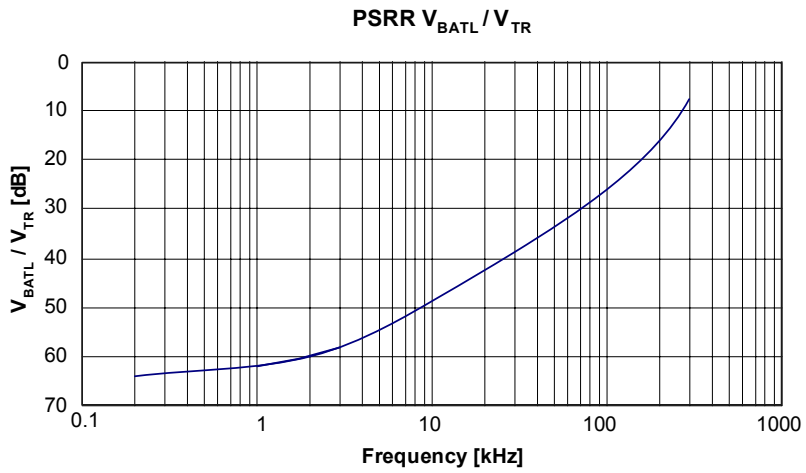


Figure 9 Typical Frequency Dependence of PSRR V_{BATL}/V_{TR}

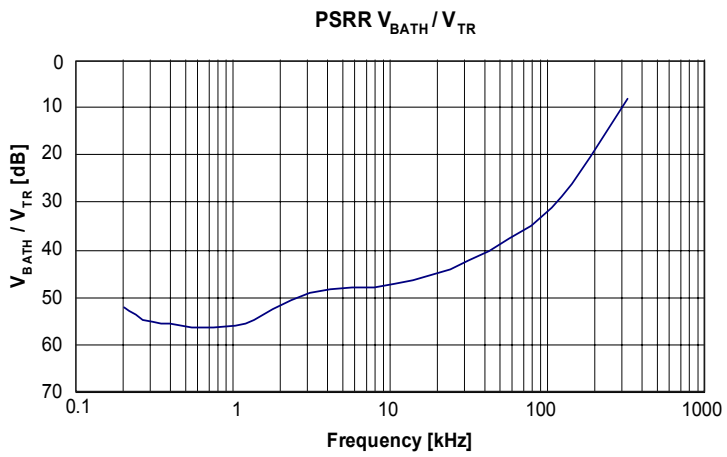


Figure 10 Typical Frequency Dependence of PSRR V_{BATH}/V_{TR}

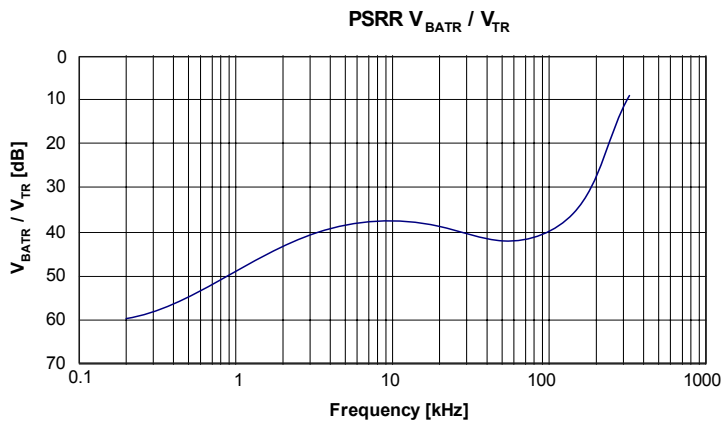


Figure 11 Typical Frequency Dependence of PSRR V_{BATR}/V_{TR}

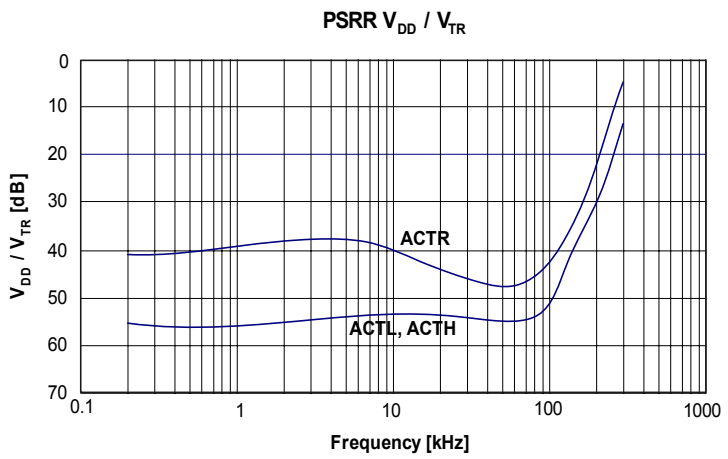


Figure 12 Typical Frequency Dependence of PSRR V_{DD}/V_{TR}

5 Test Figures

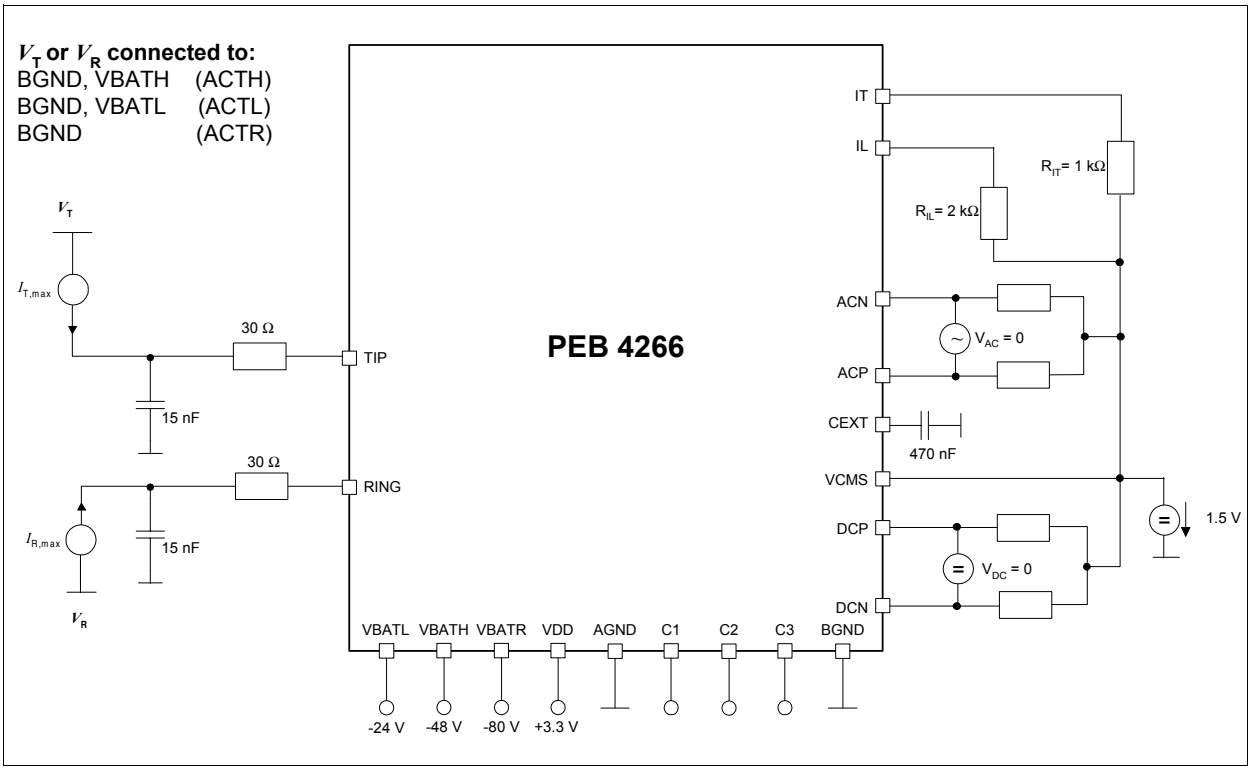


Figure 13 Output Current Limit

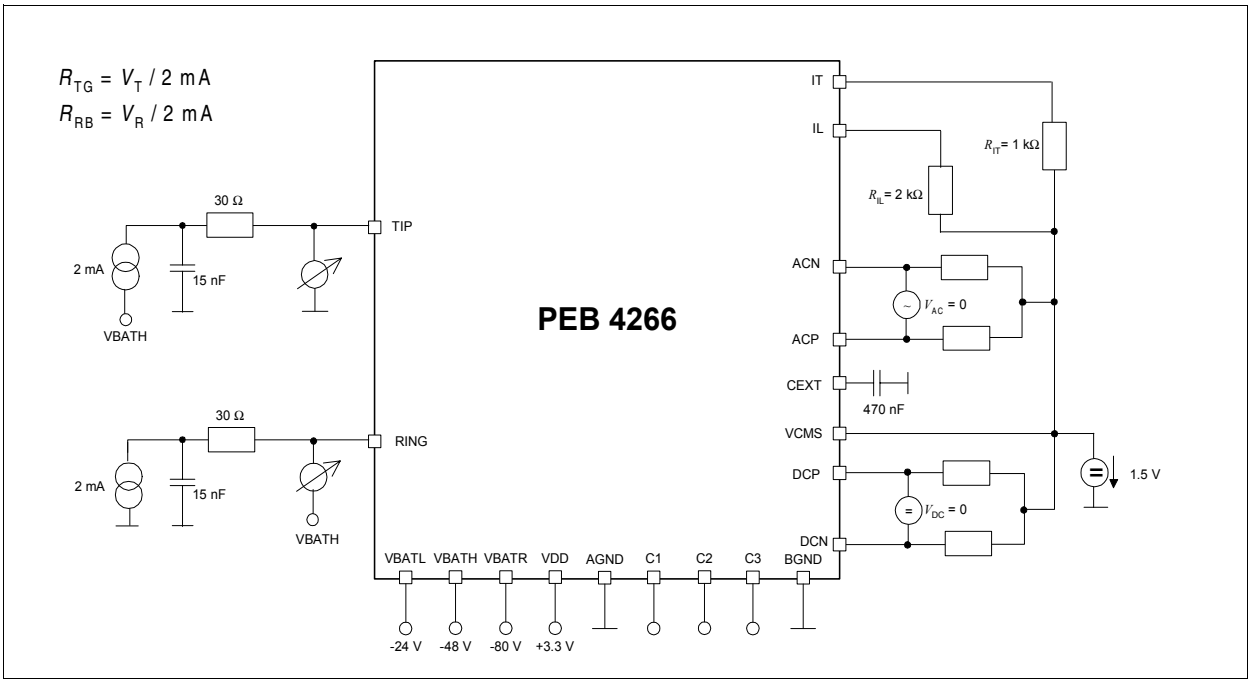


Figure 14 Output Resistance PDRH, PDRHL

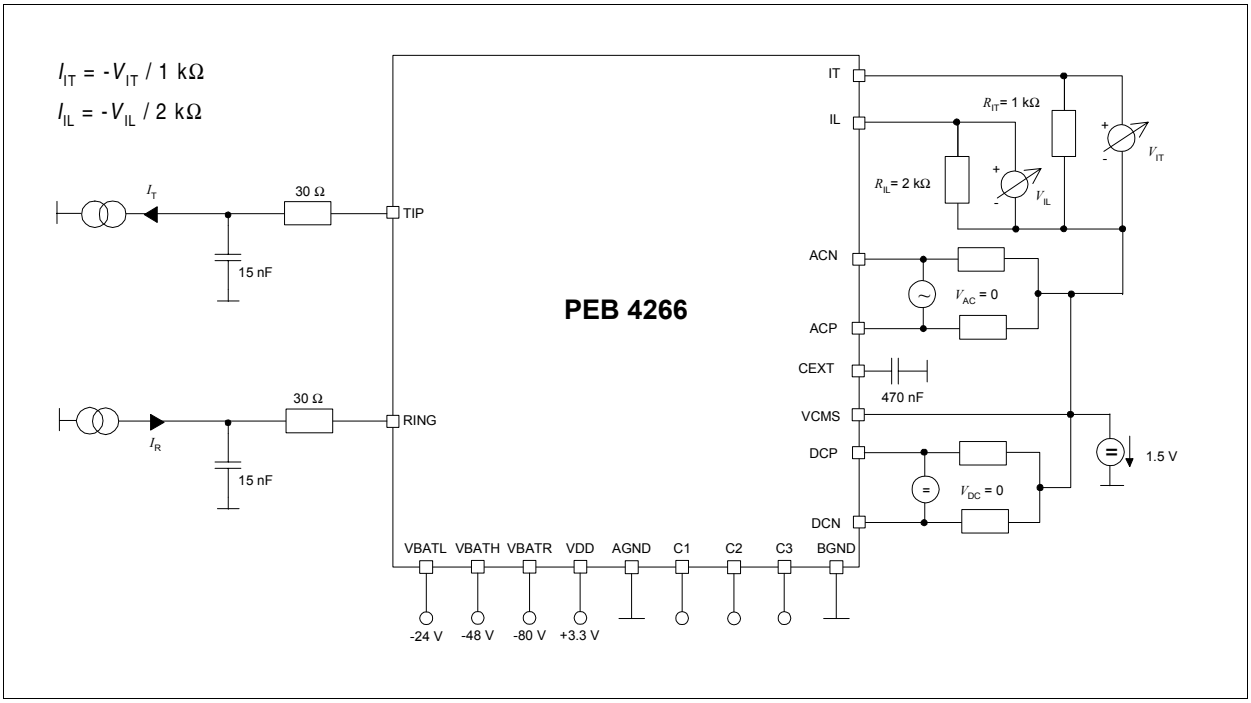


Figure 15 Current Outputs IT, IL

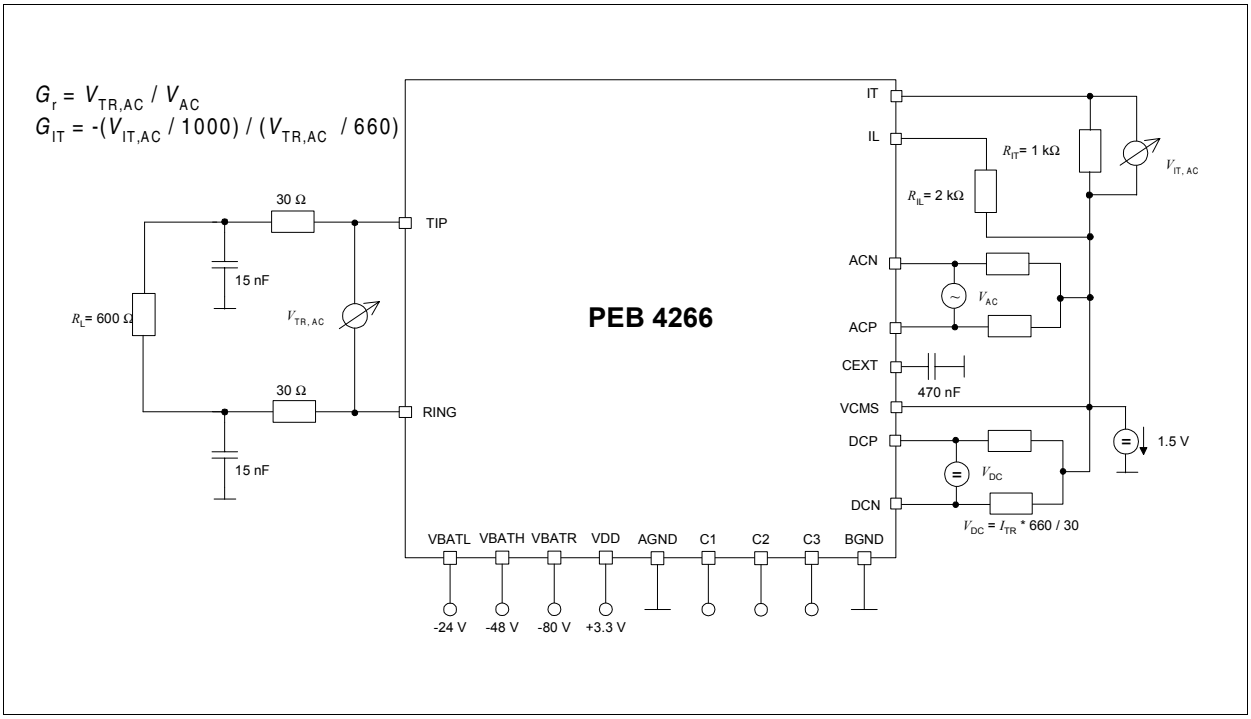


Figure 16 Transmission Characteristics

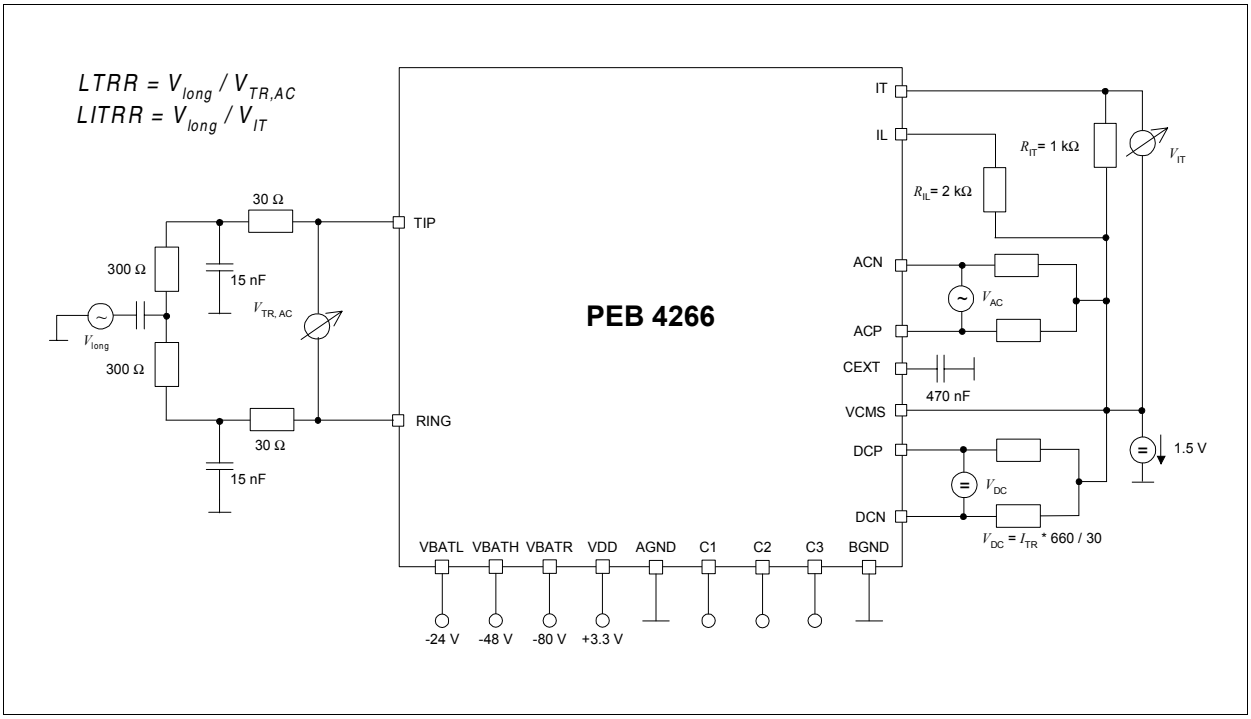


Figure 17 Longitudinal to Transversal Rejection

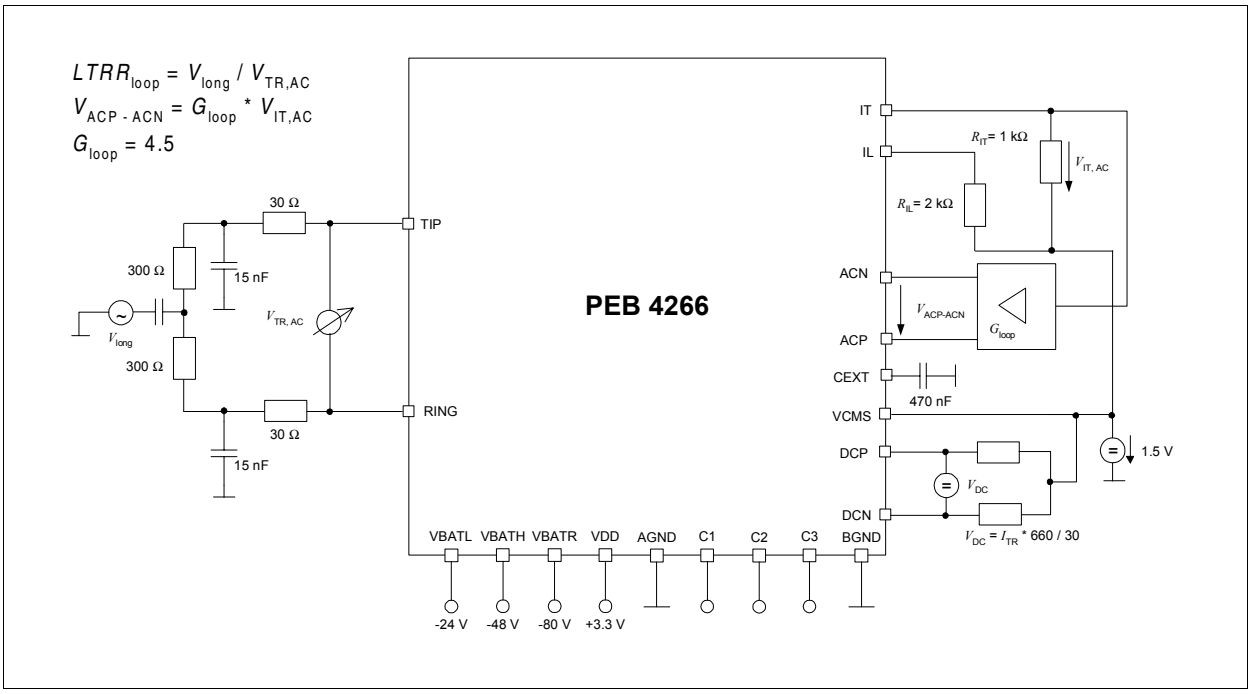


Figure 18 Longitudinal to Transversal Rejection Loop

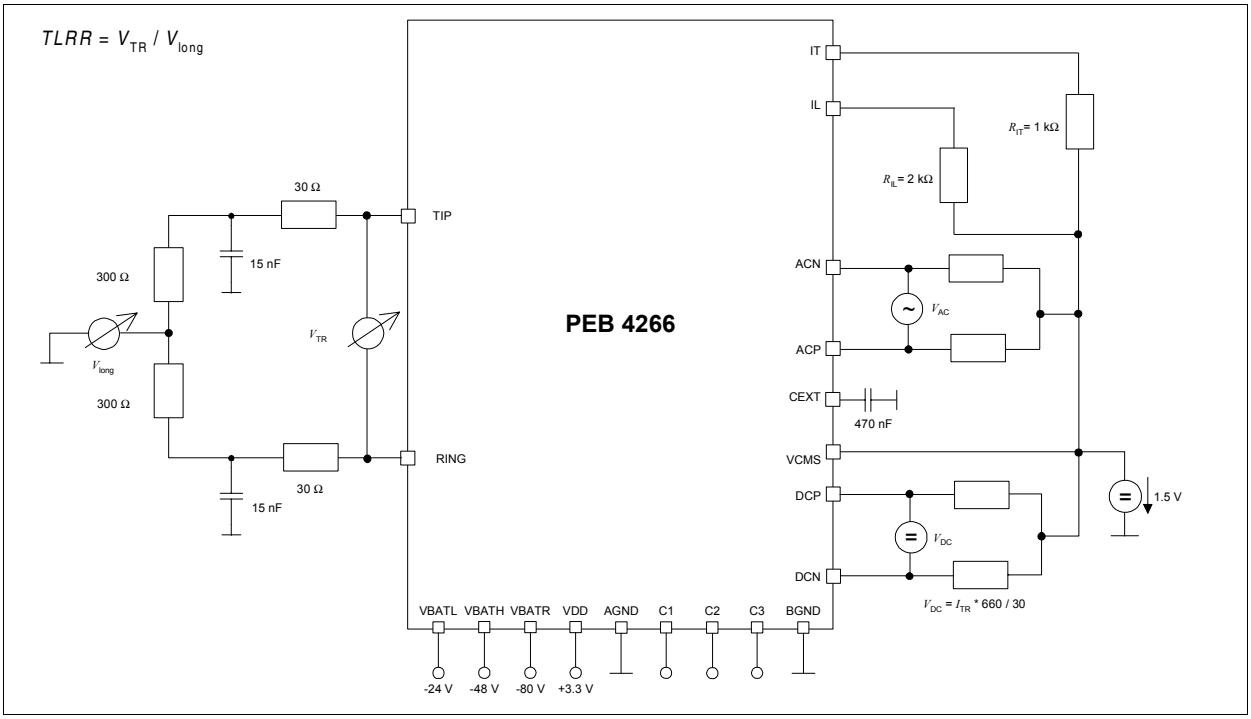


Figure 19 Transversal to Longitudinal Rejection

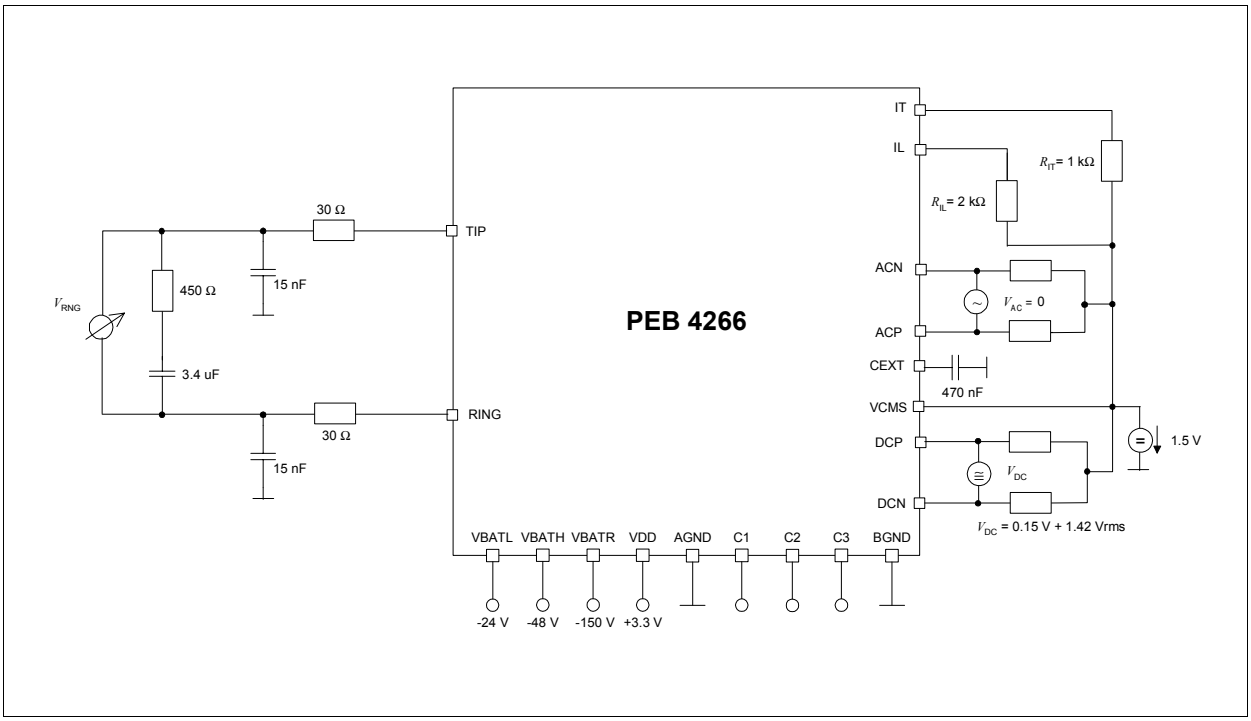


Figure 20 Ring Amplitude

6 Package Outlines

6.1 PG-DSO-20-24 Package

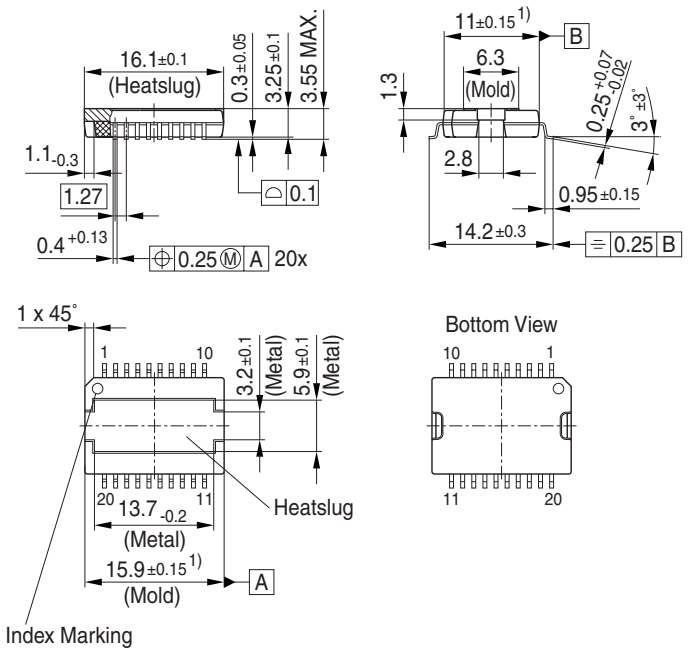


Figure 21 PG-DSO-20-24 (Plastic Green Dual Small Outline)

Notes

1. *Dimensions in mm.*
2. *The PG-DSO-20-24 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).*

Attention: The heatsink (see Figure 21) is connected to VBATR via the chip substrate. Due to the high voltage of up to 150 V between VBATR and BGND, touching of the heatsink or any attached conducting part can be hazardous.

6.2 PG-VQFN-48-15 Package

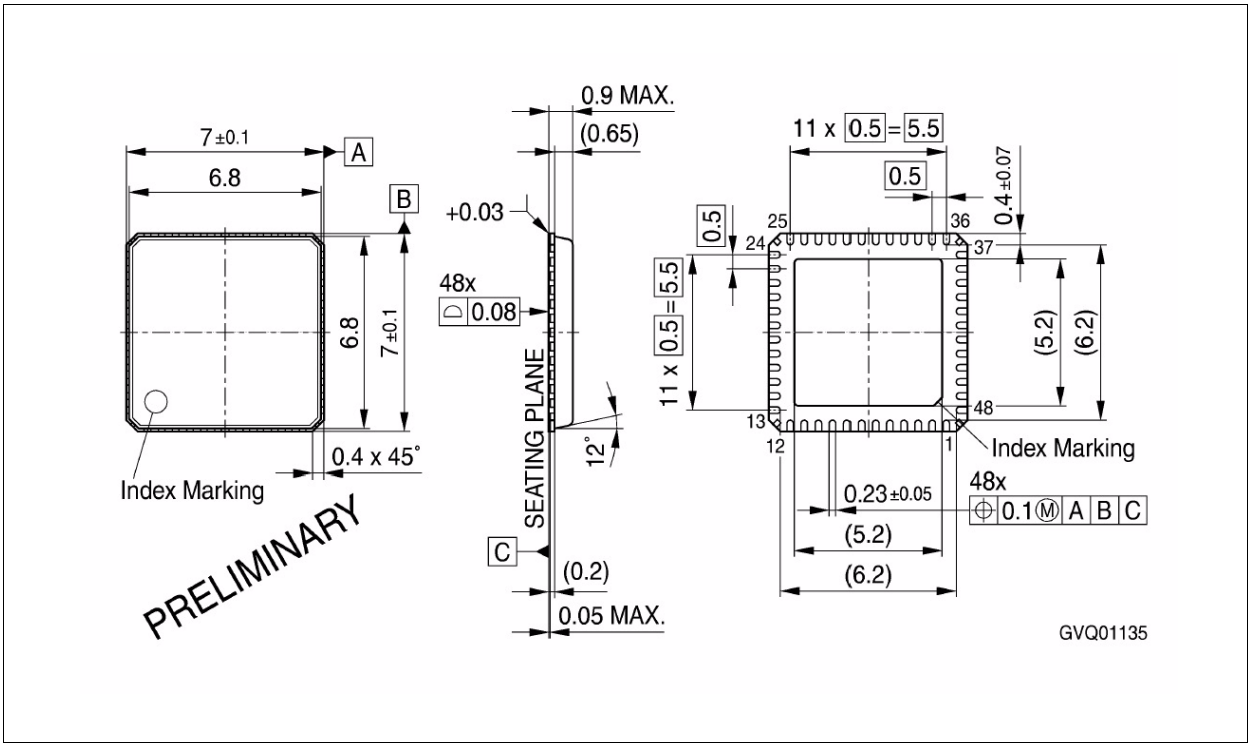


Figure 22 **PG-VQFN-48-15** (Plastic Green Very Thin Profile Quad Flat Non Leaded)

Note: Dimensions in mm.

Attention: The exposed die pad and die pad edges are connected to VBATR via the chip substrate. Due to the high voltage of up to 150 V between VBATR and BGND, touching of the die pad or any attached conducting part can be hazardous.

6.2.1 Recommended PCB Foot Print Pattern for PG-VQFN-48-15 Package

For detailed information on PCB related thermal and soldering issues of the PG-VQFN-48-15 package see **[5]**, chapter 3 and 4.

References

[1] SLIC-S/-S2 / TSLIC-S (PEF 4264/-2 / PEF 4364) Application Note “Protection for SLIC-S/-S2 against Overvoltages and Overcurrents according to ITU-T K. 20/K.21/K.45” Rev. 1.0, 2003-07-18

[2] VINETIC® Version 1.4 Prel. Application Note External Components Rev. 2.0, 2005-09-06

[3] VINETIC® Version 2.1/2.2 Preliminary Hardware Design Guide Rev. 2.0, 2005-05-19

[4] Prel. Addendum Rev. 1.0 to VINETIC® Version 1.4 Prel. User´s Manual System Reference DS1, 2005-03-10

[5] Recommendations for Printed Circuit Board Assembly of Infineon P(G)-VQFN Packages, Application Support, DS3, 2006-03-03

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