National Semiconductor

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TP3155 Time Slot Assignment Circuit

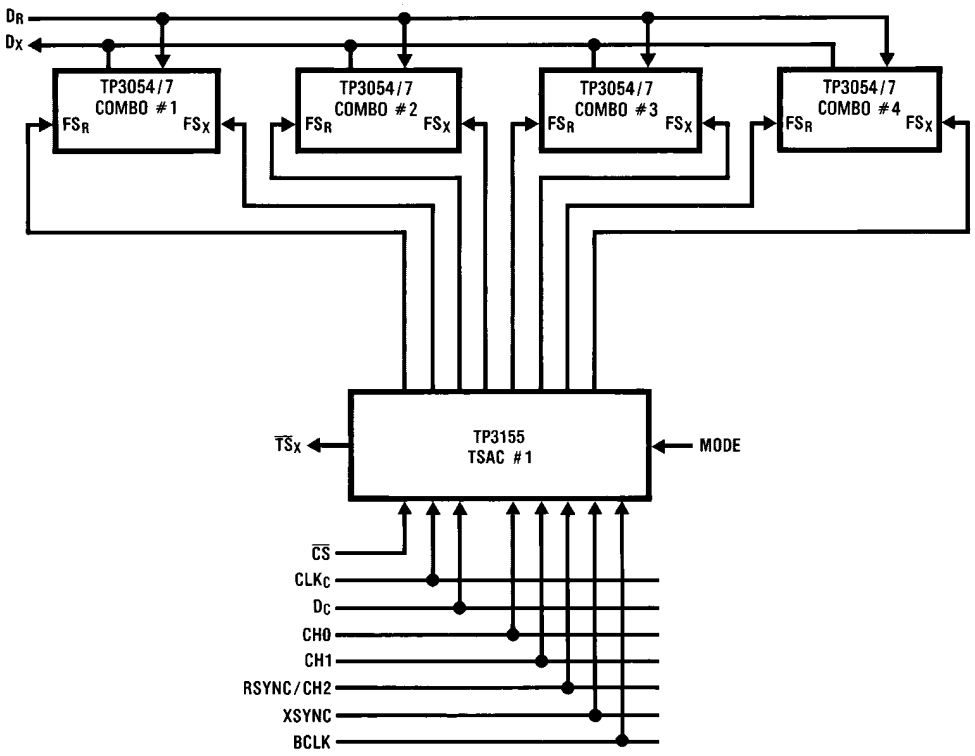
General Description

The TP3155 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for up to 8 COMBO™ CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 32 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to COMBO CODEC/Filters to be made.

Features

- Controls up to 8 COMBO CODEC/Filters
- Independent transmit and receive time slot assignments
- 8-channel unidirectional mode
- Up to 32 time slots per frame
- Serial control interface compatible with TP3020/TP3021 CODECs
- LS TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



TL/H/5118–1

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Relative to GND	7V
Voltage at Any Input or Output	V_{CC} + 0.3V to GND −0.3V
Operating Temperature Range (Ambient)	−25°C to +125°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating to be determined.

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic Low				**0.7**	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	**−1**		**1**	μA
MODE	V_{IN} = 0V	**−100**			μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X and FS_R Outputs, I_{OL} = 5 mA			0.4	V
	TS_X Output, I_{OL} = 5 mA			**0.4**	V
Power Dissipation Operating Current	BCLK = 2.048 MHz, All Outputs Open-Circuit		1	**1.5**	mA

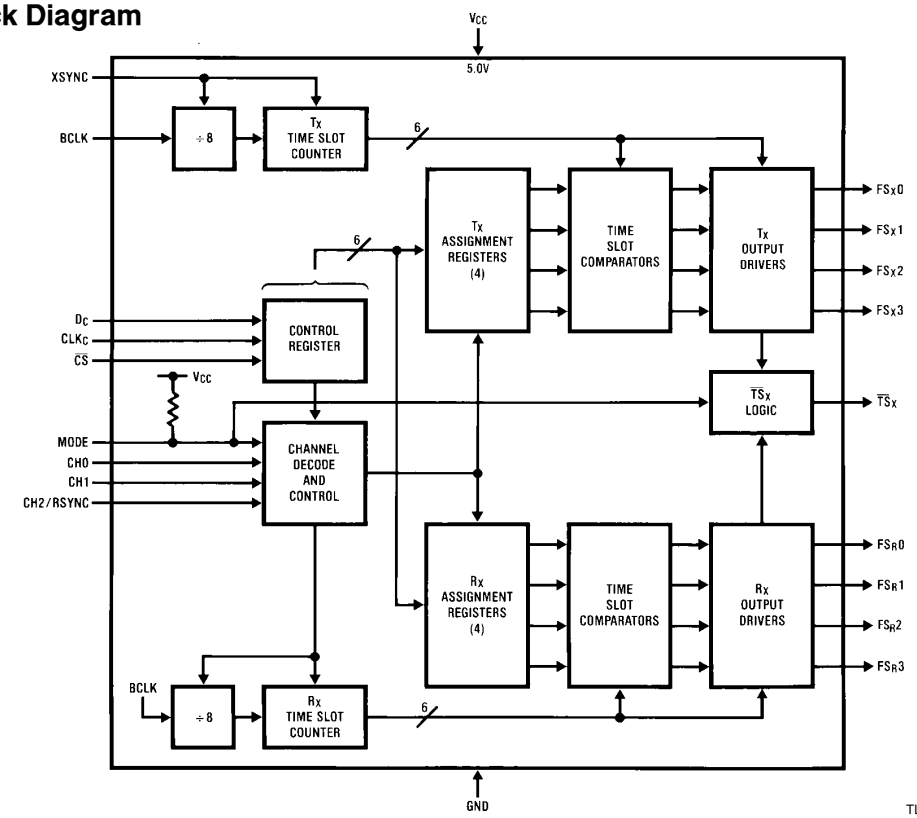
Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	BCLK, CLK_C	**480**		ns
t_{WCH}	Width of Clock High	BCLK, CLK_C	**160**		ns
t_{WCL}	Width of Clock Low	BCLK, CLK_C	**160**		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		**50**		ns
t_{HCD}	Hold Time from CLK_C to D_C		**50**		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		**30**		ns
t_{HCC}	Hold Time from CLK_C to $\overline{CS}$		**100**		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		**50**		ns
t_{HCHC}	Hold Time from Channel Select to CLK_C		**50**		ns
t_{DBF}	Delay Time from BCLK Low to $FS_{X/R}$ 0–3 High or Low	C_L = 50 pF		**100**	ns
t_{HSYNC}	Hold Time from BCLK to Frame Sync		**50**		ns
t_{SSYNC}	Set-Up Time from Frame Sync to BCLK		**100**		ns
t_{DTL}	Delay to $\overline{TS_X}$ Low	C_L = 50 pF		**140**	ns
t_{DTH}	Delay to $\overline{TS_X}$ High	R_L = 1k to V_{CC}	**30**	**140**	ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	BCLK, CLK_C		50	ns

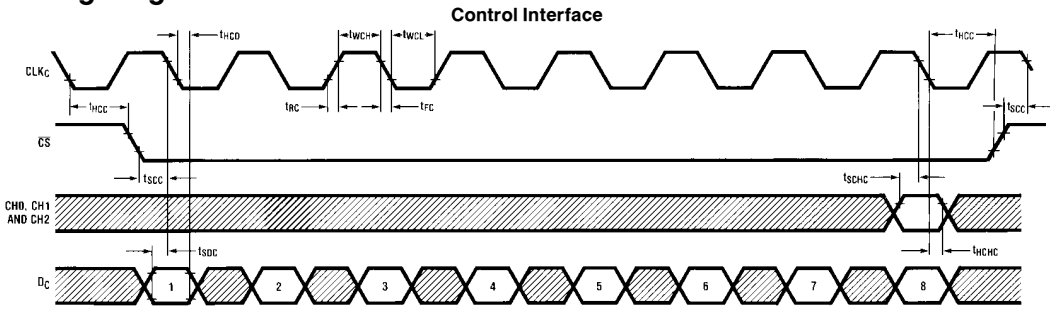
Block Diagram



TL/H/5118–2

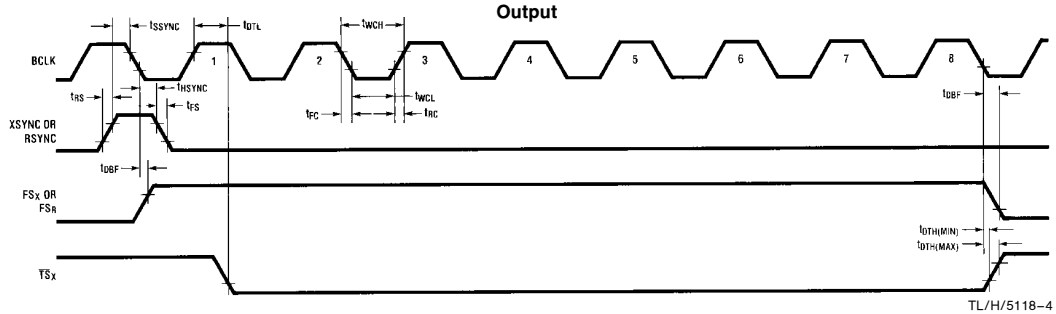
Timing Diagrams

Control Interface



TL/H/5118–3

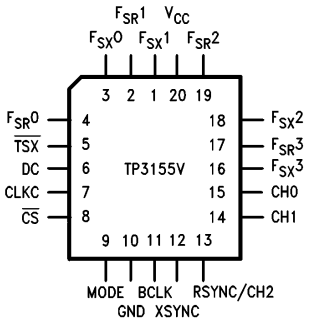
Output



TL/H/5118–4

Connection Diagrams

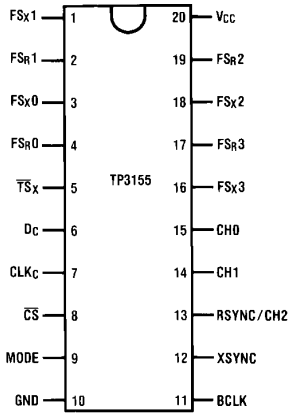
Plastic Chip Carrier (PCC) Package



TL/H/5118–5

Order Number TP3155V
See NS Package Number V20A

Dual-In-Line Package



TL/H/5118–6

Top View

Order Number TP3155N
See NS Package Number N20A

Pin Descriptions

Symbol	Description
FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
FS_X0	A transmit frame sync output similar to pin 1.
FS_R0	A receive frame sync output similar to pin 2.
$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.
D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.
CLK_C	The clock input for the control interface.
$\overline{CS}$	The active-low chip select for the control interface.
MODE	The mode select input. When left open-circuit or connected to V_{CC}, mode 1 is selected, and when connected to GND, mode 2 is selected.
GND	The 0V ground connection to the device.

Symbol	Description
BCLK	The bit clock input, which should run at the same rate as that for the COMBO CODEC/Filter COMBO.
XSYNC	The transmit TS0 sync pulse input. Must be synchronous with BCLK.
RSYNC/CH2	The function of this input is determined by the MODE input (pin 9). In mode 1 this is the receive TS0 sync pulse, RSYNC, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
CH1	The input for the next significant bit of the channel select word.
CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
FS_X3	A transmit frame sync output similar to pin 1.
FS_R3	A receive frame sync output similar to pin 2.
FS_X2	A transmit frame sync output similar to pin 1.
FS_R2	A receive frame sync output similar to pin 2.
V_{CC}	The positive supply to the device. 5V $\pm$5%.

Functional Description

OPERATING MODES

The TP3155 control interface requires an 8-bit serial control word which is compatible with the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 31. A frame sync output is active-high for one time slot, which is always 8 cycles of BCLK. A frame may consist of any number of time slots up to 32. If a timeslot is assigned which is beyond the number of time slots in a frame, the FS_X or FS_R output to which it was assigned will remain inactive.

Two modes of operation are available. Mode 1 is for systems requiring different time slot assignments for the transmit and receive direction of each channel. Mode 1 is selected by leaving pin 9 (MODE) open-circuit or connecting it to V_{CC}. In this case, Pin 13 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0–FS_R3, are assigned with respect to RSYNC. The XSYNC input defines the start of each transmit frame and outputs FS_X0–FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia).

Mode 2 provides the option of assigning all 8 frame sync outputs with respect to the XSYNC input. Mode 2 is selected by connecting pin 9 (MODE) to GND. This makes the TP3155 TSAC useful for either an 8-channel undirectional controller or for systems in which the transmit and receive directions of each channel are always assigned to the same time slot as the other, i.e., the FS_X and FS_R inputs on the COMBO CODEC/Filter are hard-wired together. In this case, logical selection of the channel to be assigned is made via inputs CH0, CH1 and CH2 (see Table Ib).

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0–FS_X3 and FS_R0–FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (and CH2 in mode 2), see Tables Ia and Ib.

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

A new time slot assignment is transferred to the selected assignment register on the high going transition of $\overline{CS}$. The new assignment is re-synchronized to the system clock such that the new FS output pulses will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of BCLK. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of BCLK after RSYNC goes high defines the start of receive TS0, and outputs FS_R0–FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS}_X$ OUTPUT

In mode 1 (separate transmit and receive assignments), this output pulls low whenever any FS_X output pulse is being generated. In mode 2, this output pulls low whenever any FS_X or FS_R output is being generated. At all other times it is open-circuit, allowing the $\overline{TS}_X$ outputs of a number of TSACS to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE Ia. Control Mode 1
(TP3020/TP3021 Compatible)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into the D_C input.

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	X	X	X	X	X	(Note 1)

CH1	CH0	Channel Selected
0	0	Assign to FS_x0 and/or FS_R0
0	1	Assign to FS_x1 and/or FS_R1
1	0	Assign to FS_x2 and/or FS_R2
1	1	Assign to FS_x3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE Ib. Control Mode 2

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	
1	0	
1	1	Disable selected output

Note 1: When T5 = 1, then the appropriate FS_X or FS_R output is inactive.

Definitions and Timing Conventions

DEFINITIONS

V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ns.
Period	The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as $t_{Dxxyy[\ \|H\|L]}$, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

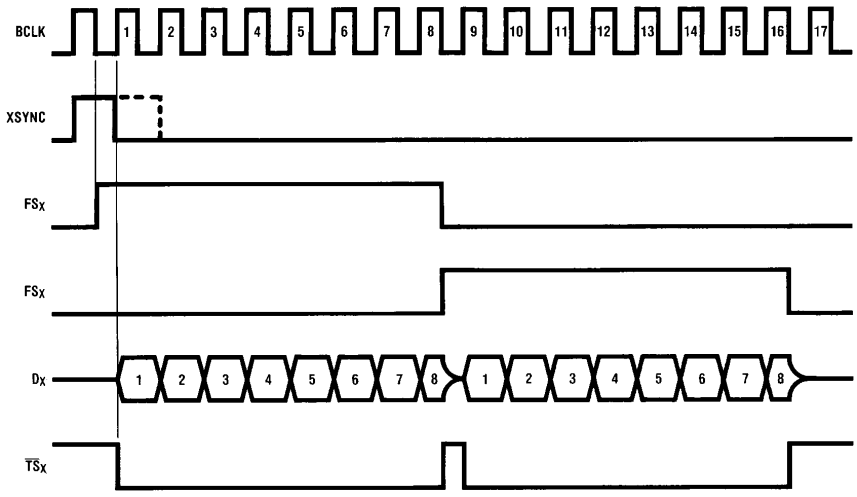
Applications Information

A combination of the TP3155 TSAC and any CODEC/Filter COMBO from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before BCLK goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eight bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

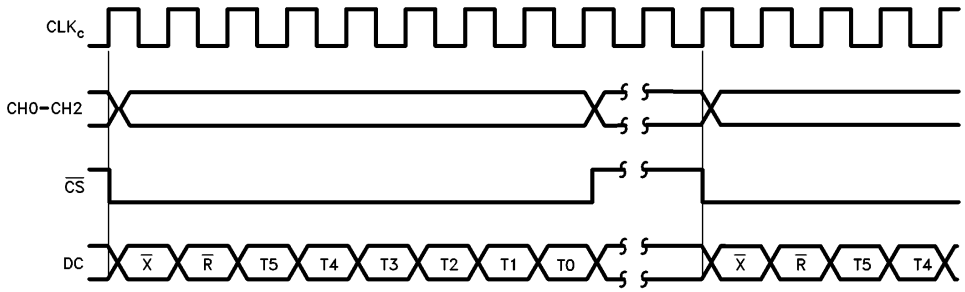
Figure 2 shows typical timing for the control data interface.

Figure 3 shows the digital interconnections of a typical line card application.



TL/H/5118–7

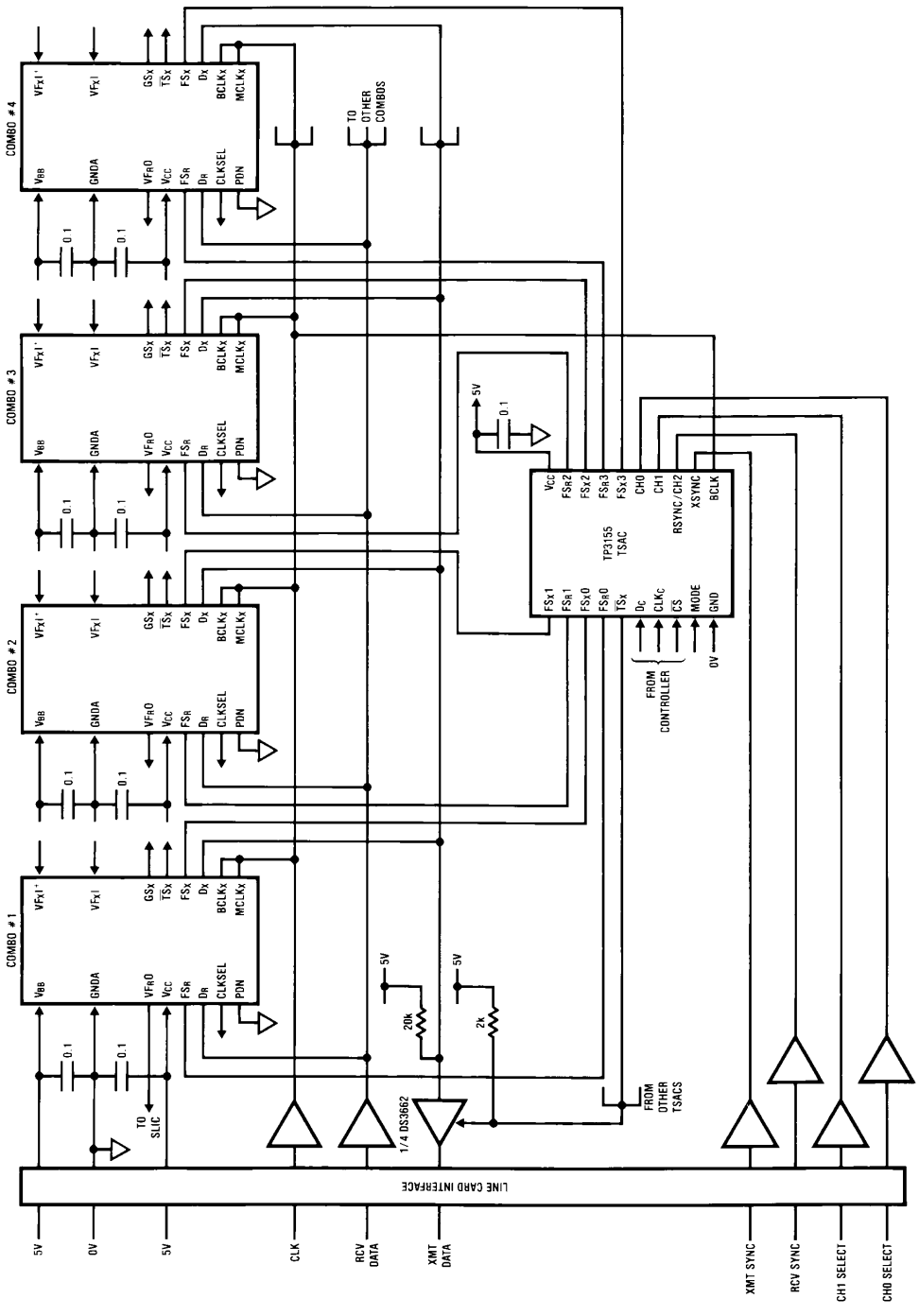
FIGURE 1. Transmit Data Timing



TL/H/5118–8

FIGURE 2. Control Data Timing

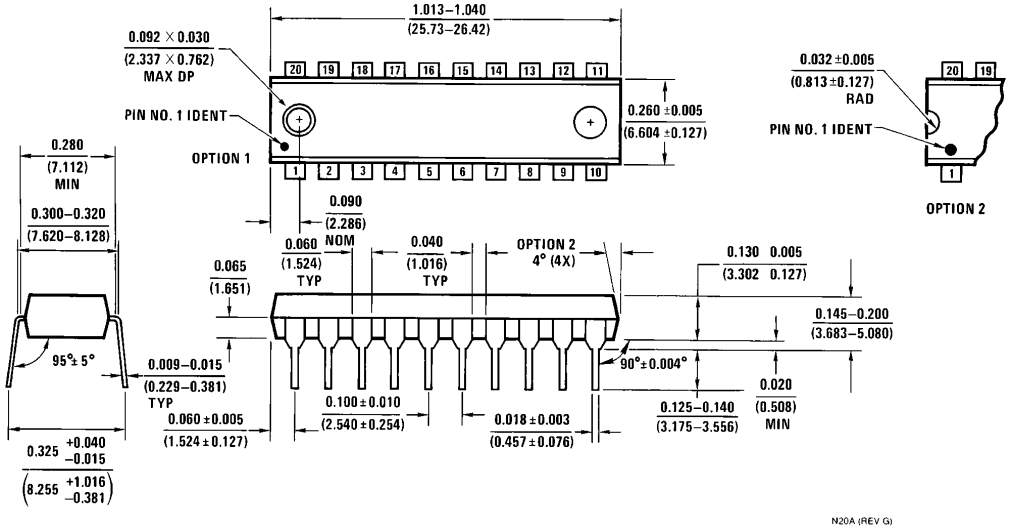
Application Information (Continued)



TL/H/5118–9

FIGURE 3. Digital Interconnections on a Typical Synchronous Line Card

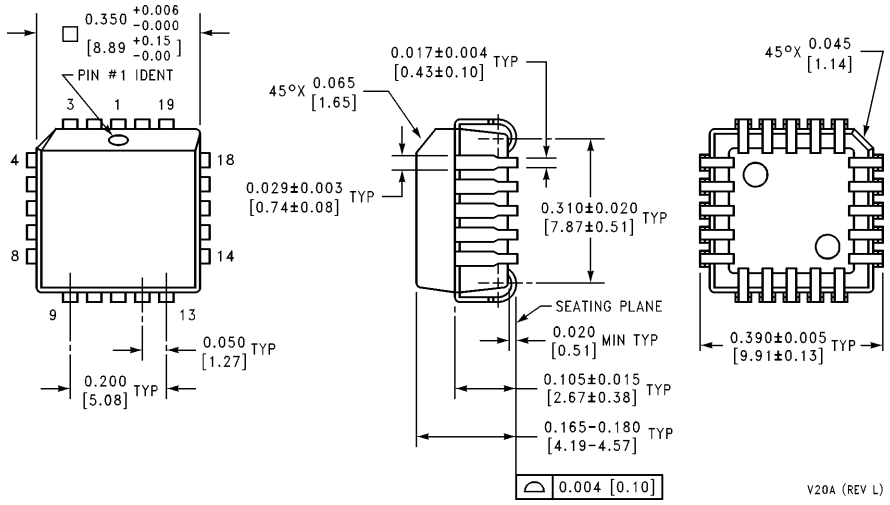
Physical Dimensions inches (millimeters)



Molded Dual-In-Line Package (N)
Order Number TP3155N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 113982



Plastic Chip Carrier Package (V)
Order Number TP3155V
NS Package Number V20A

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