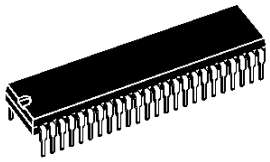
SGS-THOMSON MICROELECTRONICS

MK50H27

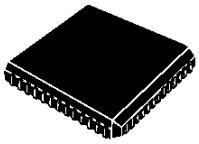
Signalling System 7 Link Controller

SECTION 1 - FEATURES

- Complete Level 2 Implementation of SS7.
- Compatible with 1988 CCITT, AT&T, ANSI, and Bellcore Signalling System Number 7 link level protocols.
- Optional operation to comply with Japanese TTC JT-Q703 specification requirements
- Pin-for-pin and architecturally compatible with MK50H25 (X.25/LAPD), MK50H29 (SDLC), and MK50H28(Frame Relay).
- System clock rates up to 33 MHz (MK50H27 - 33), or 25 MHz (MK50H27 - 25).
- Data rate up to 4 Mbps continuous for SS7 protocol processing, 20 Mbps for transparent HDLC mode, or up to 51 Mbps bursted (gapped data clocks, non-continuous data).
- On chip DMA control with programmable burst length.
- DMA transfer rate of up to 13.3 Mbytes/sec using optional 5 SYSCLK DMA cycle (150 nS) at 33 MHz SYSCLK.
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- Selectable BEC or PCR retransmission methods, including forced retransmission for PCR.
- Handles all 7 SS7 Timers, plus the additional Signal Unit interval timers for Japanese SS7.
- Handles all SS7 frame formatting:
  - Zero bit insert and delete
  - FCS generation and detection
  - Frame delimiting with flags
- Programmable minimum Signal Unit spacing (number of flags between SU's)
- Handles all sequencing and link control.
- Selectable FCS of 16 or 32 bits.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- Programmable for full or half duplex operation Programmable Watchdog Timers for RCLK and TCLK (to detect absence of data clocks)



DIP48



PLCC 52

- Available in 52 pin PLCC, 84 pin PLCC(for use with external ROM), or 48 pin DIP packages.

SECTION 2 - INTRODUCTION

The SGS - Thomson SS7 Signalling Link Controller (MK50H27) is a VLSI semiconductor device which provides a complete level 2 data communication control conforming to the CCITT, ANSI, BELLCORE, and AT&T versions of SS7, as well as options to allow conformance to TTC JT-Q703 (Japanese SS7). This includes signal unit formatting, transparency (so-called "bit-stuffing"), error recovery by two types of retransmission, error monitoring, sequence number control, link status control, and fill in signal unit generation.

One of the outstanding features of the MK50H27 is its buffer management which includes on-chip DMA. This feature allows users to handle multiple MSU's of receive and transmit data at a time. (A conventional data link control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK50H27 will move multiple blocks of receive and transmit data directly into

INTRODUCTION (Continued)

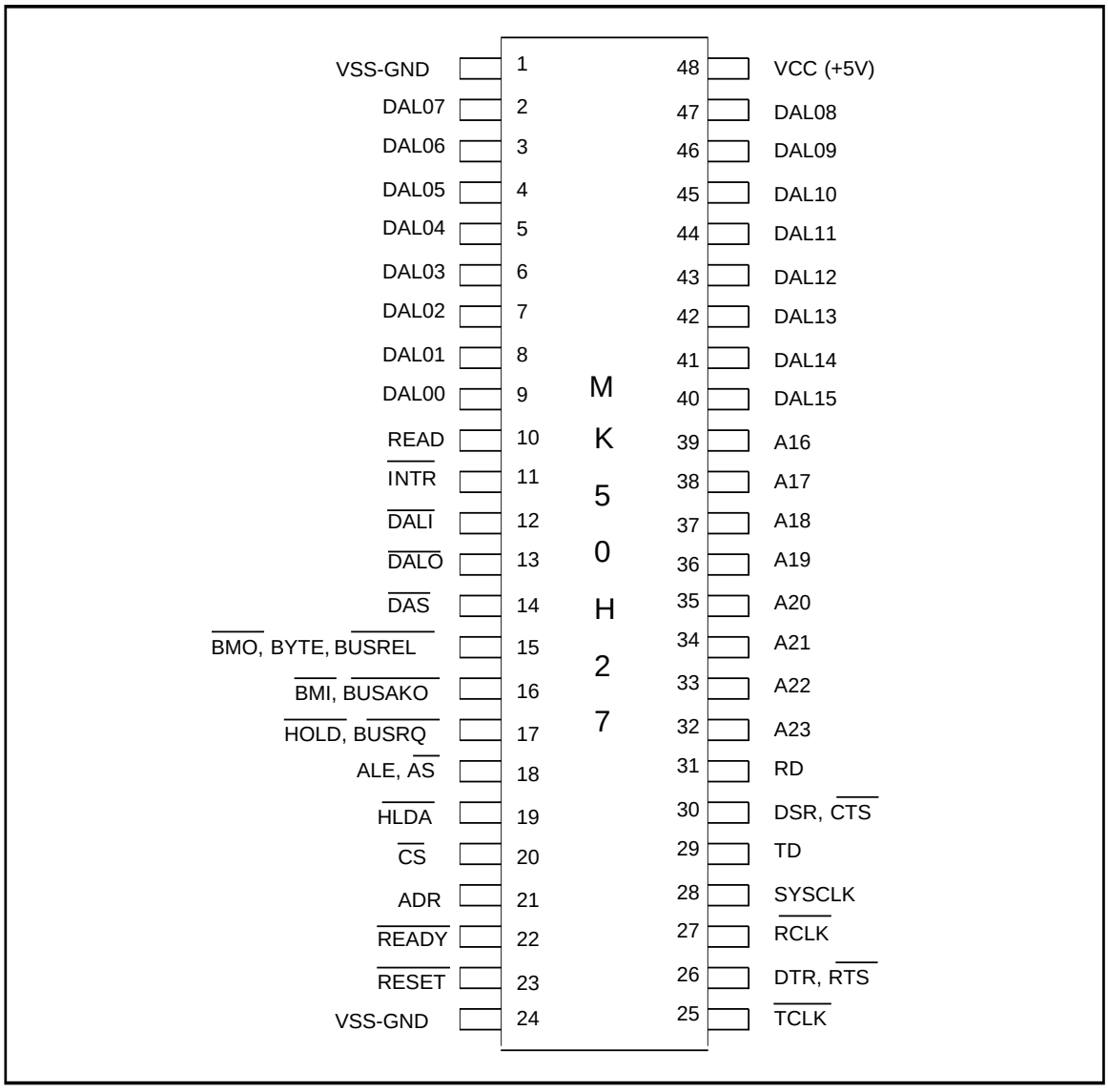
and out of memory through the Host's bus. A possible system configuration for the MK50H27 is shown in figure 1.

For added flexibility a transparent mode provides an HDLC transport mechanism without link layer support. In this mode no protocol processing is done, all data received between opening flag and CRC is written to the shared memory buffer and it is up to the user to take care of the upper level software.

The MK50H27 may be used with any of several popular microprocessors, such as: 68040 ... 68000, 6800, Z8000, Z80, 80486 ... 8086, i960, etc.

The MK50H27 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins. All signal pins on the MK50H27 are TTL compatible. This has the advantage of making the MK50H27 independent of the physical interface. As shown in figure 1, line drivers and receivers are used for electrical connection to the physical layer.

DIP48 PIN CONNECTION (Top view)



PLCC52 PIN CONNECTION (Top view)

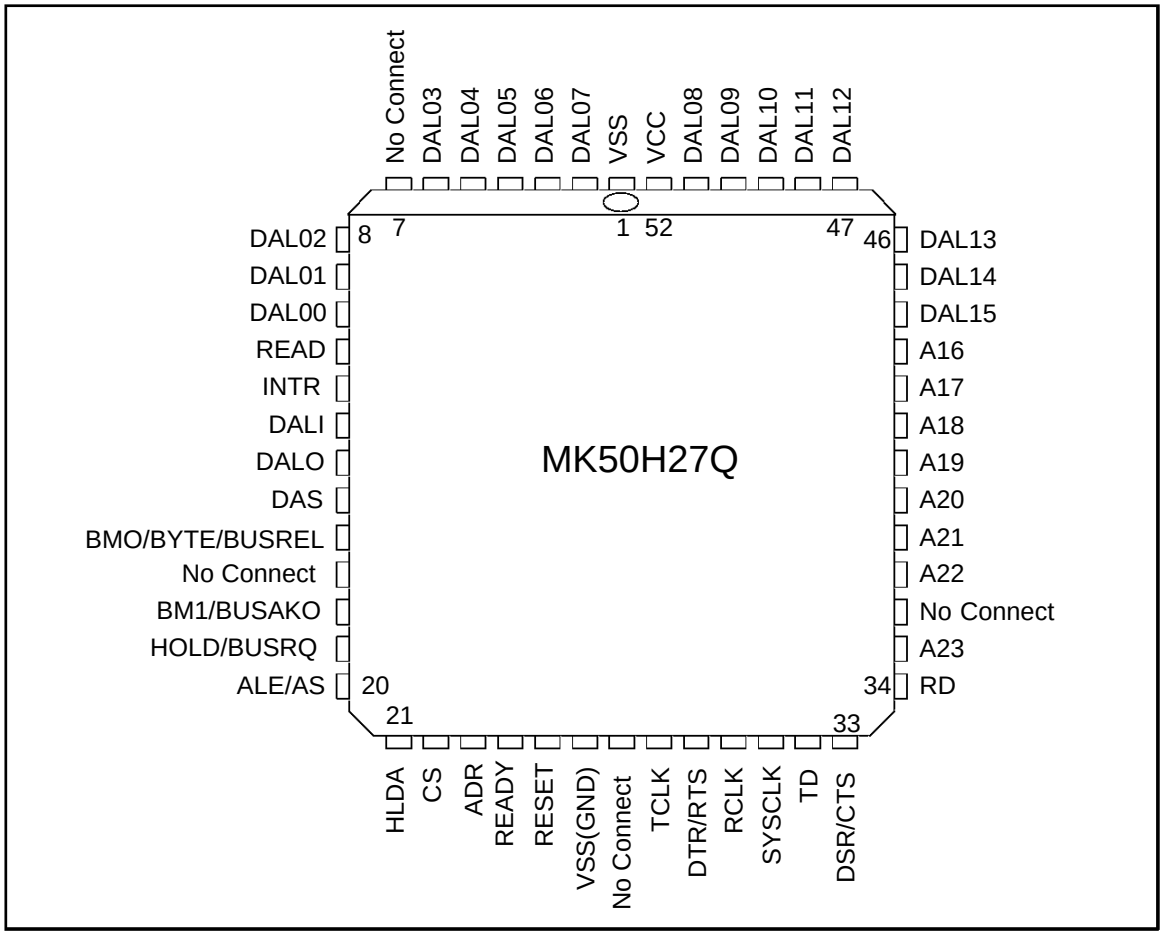


TAble 1 - PIN DESCRIPTION

LEGEND:

I	Input only	O	Output only
IO	Input / Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Note: Pin out for 52 pin PLCC is shown in brackets.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
DAL<15:00>	2-9 40-47 [2-10 44-51]	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	10 [11]	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK50H27 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK50H27 as a Bus Slave : READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK50H27 as a Bus Master : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
INTR	11 [12]	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
DALI	12 [13]	O/3S	DAL IN is an external bus transceiver control line. DALI is driven by the MK50H27 only while it is the BUS MASTER. DALI is asserted by the MK50H27 when it reads from the DAL lines during the data portion of a READ transfer. DALI is not asserted during a WRITE transfer.
DALO	13 [14]	O/3S	DAL OUT is an external bus transceiver control line. DALO is driven by the MK50H27 only while it is the BUS MASTER. DALO is asserted by the MK50H27 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
DAS	14 [15]	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition, data is stable and valid at the low to high transition of DAS. This signal is driven by the MK50H27 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
BMO BYTE BUSREL	15 [16]	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input BUSREL and is used by the host to signal the MK50H27 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16.
BM1 BUSAKO	16 [18]	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = BMO (O/3S) I/O PIN 16 = BM1 (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. MK50H27 drives these lines only as a Bus Master. MK50H27 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. BM1 BM0 TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			If CSR4<00> BCON = 1, I/O PIN 15 = BYTE (O/3S) I/O PIN 16 = BUSAKO (O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK50H27 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE BUSAKO is a bus request daisy chain output. If MK50H27 is not requesting the bus and it receives HLDA, BUSAKO will be driven low. If MK50H27 is requesting the bus when it receives HLDA, BUSAKO will remain high Note: All transfers are entire word unless the MK50H27 is configured for 8 bit operation.
HOLD BUSRQ	17 [19]	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0, I/O PIN 17 = HOLD HOLD request is asserted by MK50H27 when it requires a DMA cycle, if HLDA is inactive, regardless of the previous state of the HOLD pin. HOLD is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1, I/O PIN 17 = BUSRQ BUSRQ is asserted by MK50H27 when it requires a DMA cycle if the prior state of the BUSRQ pin was high and HLDA is inactive. BUSRQ is held low for the entire ensuing bus transaction.
ALE AS	18 [20]	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK50H27 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = AS As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register. AS is effectively the inversion of ALE.
HLDA	19 [21]	I	HOLD ACKNOWLEDGE is the response to HOLD. When HLDA is low in response to MK50H27's assertion of HOLD, the MK50H27 is the Bus Master. HLDA should be deasserted ONLY after HOLD has been released by the MK50H27.
CS	20 [22]	I	CHIP SELECT indicates, when low, that the MK50H27 is the slave device for the data transfer. CS must be valid throughout the entire transaction.
ADR	21 [23]	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when CS is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
READY	22 [24]	IO/OD	When the MK50H27 is a Bus Master, READY is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			As a Bus Slave, the MK50H27 asserts $\overline{\text{READY}}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. READY is a response to DAS and it will be released after $\overline{\text{DAS}}$ or $\overline{\text{CS}}$ is negated.
RESET	23 [25]	I	RESET is the Bus signal that will cause MK50H27 to cease operation, clear its internal logic and enter an idle state with the Stop bit of CSR0 set.
TCLK	25 [28]	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of TCLK. The frequency of TCLK may not be greater than the frequency of SYSCL
$\overline{\text{DTR}}$ $\overline{\text{RTS}}$	26 [29]	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{\text{RTS}}$ or as programmable IO pin $\overline{\text{DTR}}$. If configured as $\overline{\text{RTS}}$, the MK50H27 will assert this pin if it has data to send and throughout the transmission of a signal unit.
RCLK	27 [30]	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of RCLK. The frequency of RCLK may not be greater than the frequency of SYSCLK.
SYSCLK	28 [31]	I	SYSTEM CLOCK. System clock used for internal timing of the MK50H27. SYSCLK should be a square wave, of frequency up to 33 MHz.
TD	29 [32]	O	TRANSMIT DATA. Transmit serial data output.
$\overline{\text{DSR}}$ $\overline{\text{CTS}}$	30 [33]	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{\text{CTS}}$ or as programmable IO pin $\overline{\text{DSR}}$. If configured as $\overline{\text{CTS}}$, the MK50H27 will transmit all ones while $\overline{\text{CTS}}$ is high.
RD	31 [34]	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39 [37-43]	O/3S	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK50H27 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4<7> BAE bit.
VSS-GND	1,24 [1,26]		Ground Pins
VCC	48 [52]		Power Supply Pin +5.0 VDC ± 5%

SECTION 3
OPERATIONAL DESCRIPTION

The SGS-Thomson MK50H27 Multi-Logical Link Communications Controller device is a VLSI product intended for high performance data communication applications requiring SDLC link level control. The MK50H27 will perform all frame formatting, such as: frame delimiting with flags, FCS (CRC) generation and detection, and zero bit insertion and deletion for transparency. The MK50H27 also handles all supervisory (S) and unnumbered (U) frames (see Tables A & B). The MK50H27 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames for each active channel or DLCI. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit.

The MK50H27 can be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK50H27 is shown in Figure 1. This document assumes that the processor has a byte addressable memory organization.

The MK50H27 will move multiple blocks of receive and transmit data directly in and out of memory through the Host's bus.

The MK50H27 may be operated in full or half duplex mode. In half duplex mode the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK50H27 are TTL compatible. This has the advantage of making the MK50H27 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

Figure 1: Possible System Configuration for thr MK50H27

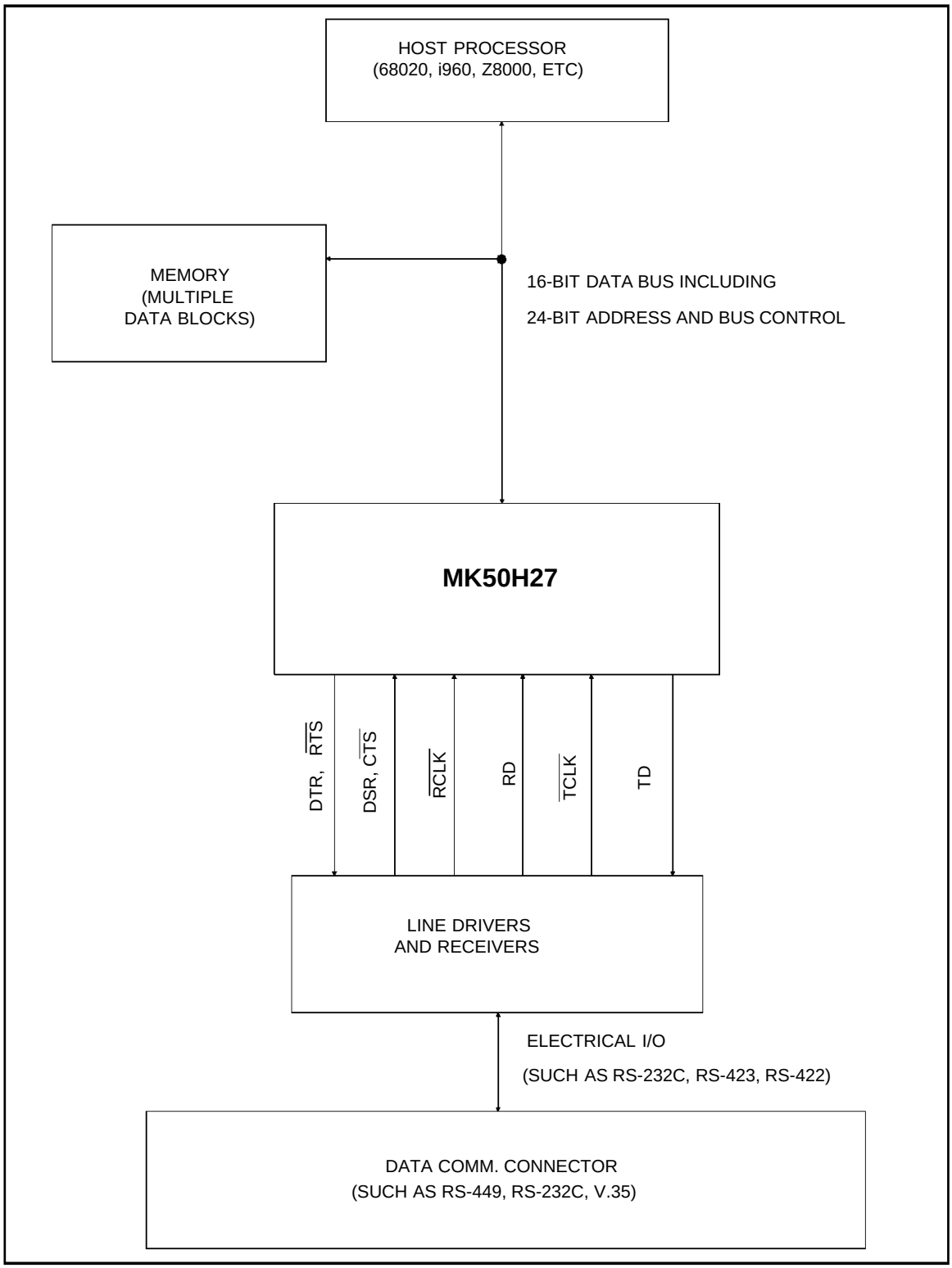
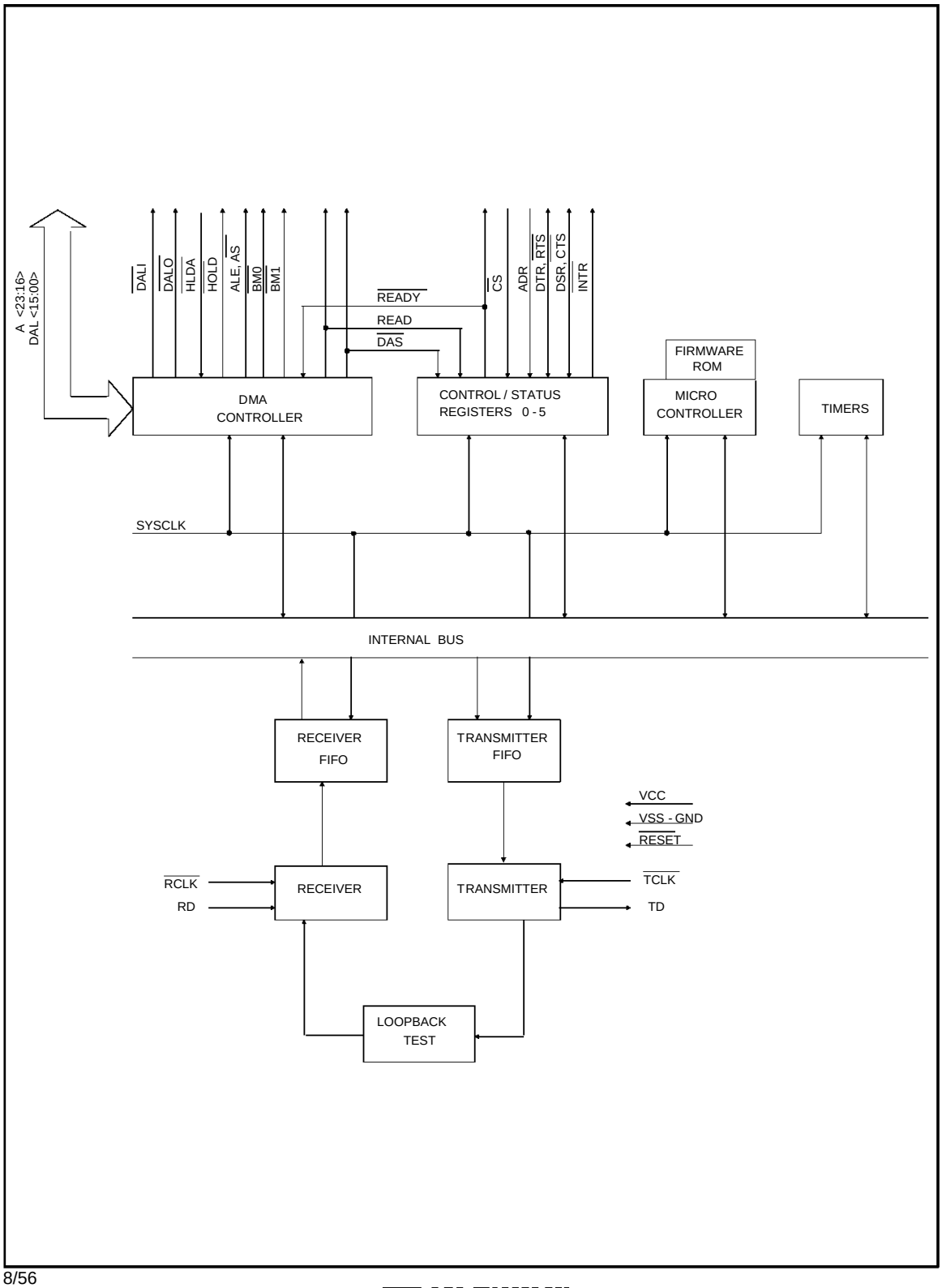


Figure 2: MK50H27 Simplified Block Diagram



3.1 Functional Blocks

Refer to the block diagram in Figure 2.

The MK50H27 is primarily initialized and controlled through six 16-bit Control and Status Registers (CSR0 thru CSR5). The CSR's are accessed through two bus addressable ports, the Register Address Port (RAP), and the Register Data Port (RDP). The MK50H27 may also generate an interrupt(s) to the Host. These interrupts are enabled and disabled through CSR0.

The on-chip microcontroller is used to control the movement of parallel receive and transmit data, and to handle the Address field filtering.

3.1.1 Microcontroller

The microcontroller controls all of the other blocks of the MK50H27. The microcontroller performs frame processing and protocol processing. All primitive processing and generation is also done here. The microcode ROM contains the control program of the microcontroller.

3.1.2 Receiver

Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good & bad CK (CheckK bit seq.)
5. Monitoring Receiver FIFO status.
6. Detection of Receiver Over-Run.
7. Odd byte detection.

   NOTE: If frames are received that have an odd number of bytes then the last byte of the frame is said to be an odd byte.

8. Detection of non-octet aligned frames. Such frames are treated as invalid.

3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.
2. Generating and appending the CK (CRC).
3. Framing outgoing frame with flags.
4. Zero bit insertion for transparency.
5. Transmitter Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS control.

3.1.4 Check Bit Sequence or Cyclic Redundancy Check

The CK (CRC) on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual CK computation circuits. The characteristics of the CK are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynomial 16 bit:
$X^{16} + X^{12} + X^5 + 1$

Remainder 16 bit (if received correctly):
High order bit-->0001 1101 0000 1111

Polynomial 32 bit:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

Remainder 32 bit (if received correctly):
high order bit-->1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller for service until it contains enough data to reach the watermark level, or an end of frame is received. This watermark level can be programmed in CSR4 (FWM) to occur when the FIFO contains at least 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmability , along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK50H27 must use the host bus. For more information, see CSR4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK50H27 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK50H27. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to burst read data from the host's memory buffers; making both the MK50H27 and the host bus more efficient.

The transmit FIFO has a watermark scheme similar to the one described for the receive FIFO above, and uses the same FWM value selections in CSR4 for the watermark. Once filled to within FWM of being full (by DMA from TX buffer in shared memory), the transmit FIFO will not interrupt the microcontroller until it empties enough to fall below the watermark level.

3.1.7 DMA Controller

The MK50H27 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK50H27 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK50H27 will begin transferring data to or from memory. The MK50H27 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case, it will complete all bus transfers before releasing bus mastership back to the host. If during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK50H27 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode,it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words or 16 bytes is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed separately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on control status register 4.

3.1.8 Bus Slave Circuitry

The MK50H27 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in Section 4 and bus signal timing is described in Figures 9 and 10.

3.2 Buffer Management Overview

Refer to Fig. 3.

3.2.1 Initalization Block

Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 200 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST, and is accessed by the MK50H27 during initialization. The Initialization Block is comprised of:

A. Mode of Operation.

B. Counter/Timer Preset Values.

C. Protocol Parameters or Options

D. Location and size of Receive and Transmit Descriptor Rings.

E. Optional Transmit Window SIze Value

F. Location of Status Buffer.

G. Optional JT-Q703 Signal Unit Interval Timer Values

H. Statistics and Error Counters.

3.2.2 The Circular Queue

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK50H27. The descriptor ring has a descriptor assigned to each buffer. Each descriptor holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each descriptor also contains two control bits called OWNA and OWNB, which denote whether the MK50H27, the HOST, or an I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK50H27 owns the buffer, the MK50H27 is allowed and commanded to transmit the buffer. When the MK50H27 does not own the buffer, it will not transmit that buffer. For receive, when the MK50H27 owns a buffer, it may place received data into that buffer. Conversely, when the MK50H27 does not own a receive buffer, it will not place received data into that buffer.

The MK50H27 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK50H27 tests the next descriptor in the descriptor ring in a "look ahead" manner. If the frame is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK50H27 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, protocol options, the number of entries for the transmitter

and receiver descriptor rings, etc. The starting address for the Initialization block, IADR, is defined in the CSR2 and CSR3 registers inside the MK50H27.

3.2.3 **Signal Unit Repertoire**

The frame format supported by the MK50H27 is shown in Table A. Each signal unit (SU) may consist of a programmable number of leading flag patterns (01111110), Backward Sequence Number, Backward Indicator Bit, Forward Sequence Number, Forward Indicator Bit, Lenght Indicator Field, followed by Signalling Information Octet, Service Information Field, or Status Field, depending on SU type, and then ended with a CK (CRC) of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags transmitted is programmable through the Mode Register in the Initialization Block. Received signal units may have as few as one flag between adjacent signal units

The symbols and definitions for the signal unit types handled by the MK50H27 are:

NAME	DEFINITION
MSU	Message Signal Unit
LSSU	Link Status Signal Unit
FISU	Fill In Signal Unit
F	Flag Sequence (01111110)
FSN	Forward Sequence Number
BSN	Backward Sequence Number
FIB	Forward Indicator Bit
BIB	Backward Indicator Bit
LI	Lenght Indicator
X	Reserved - programmed as zeroes
PRI	Priority Indication (JT-Q703 only)
SIO	Signalling Information Octe
SIF	Service Information Field
SF	Status Field
CK	Check bit Sequence (CRC)

TABLE A - MK50H27 Signal Unit Repertoire

TABLE A - MK50H27 Signal Unit Repertoire

Message Signal Unit (MSU)

F	CK	SIF	SIO	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8n,n>=2	8	2	6	1	7	1	7	8

Link Status Signal Unit (LSSU)

F	CK	SF	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8/16	2	6	1	7	1	7	8

Values for SF:

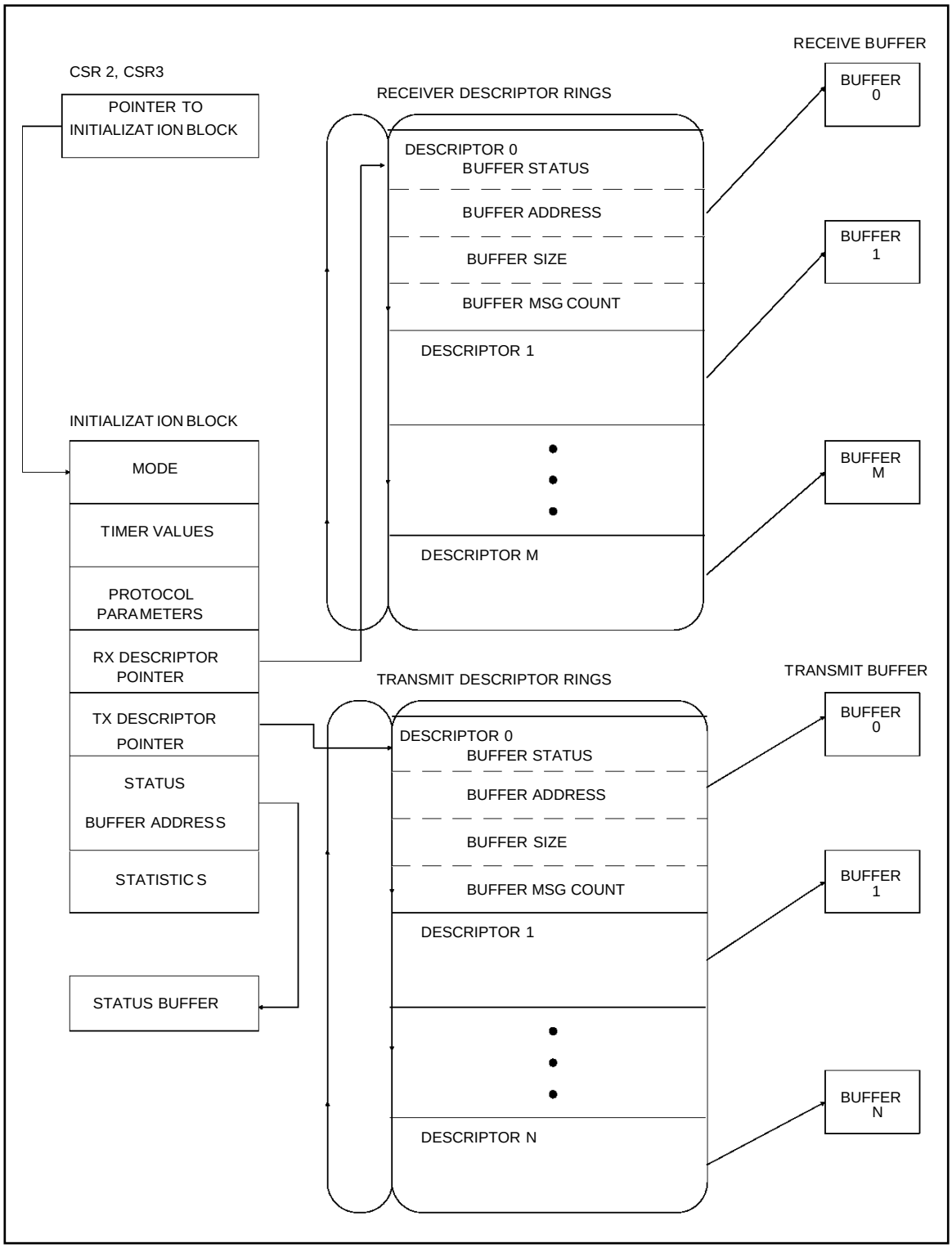
0 - SIO,	Out of alignment	3 - SIOS,	Out-of-service
1 - SIN,	Normal alignment	4 - SIPO,	Processor outage
2 - SIE,	Emergency	5 - SIB,	Congestion (Busy)

Fill-in Signal Unit (FISU)

F	CK	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	2	6	1	7	1	7	8

Right-most fields are transmitted first

Figure 3: MK50H27 Memory Management Structure



SECTION 4

PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK50H27.

4.1 Control and Status Registers

There are six Control and Status Registers (CSR's) resident within the MK50H27. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP), thus requiring only two locations in the system memory or I/O map.

4.1.1 Accessing the Control & Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten or upon a bus reset. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

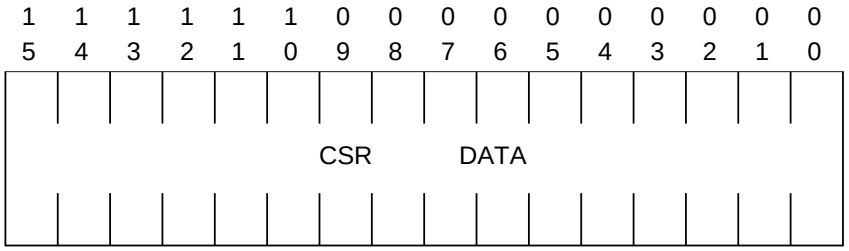
ADR	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

4.1.1.1 Register Address Port (RAP)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	BM8	0	0	0	CSR <2:0>			HBYTE

BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit transfers; this provides compatibility with 8 bitmicroprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
06:04	RESERVED	Must be written as zeroes
03:01	CS3<2:0>	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR<2:0> CSR 0 CSR0 1 CSR1 2 CSR2 3 CSR3 4 CSR4 5 CSR5
00	HBYTE	Determines which byte is addressed for 8 bit mode. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful in 8 bit mode and must be written as zero if BM8=0. HBYTE is READ/WRITE and cleared on bus reset.

4.1.1.2 **Register Data Port (RDP)**

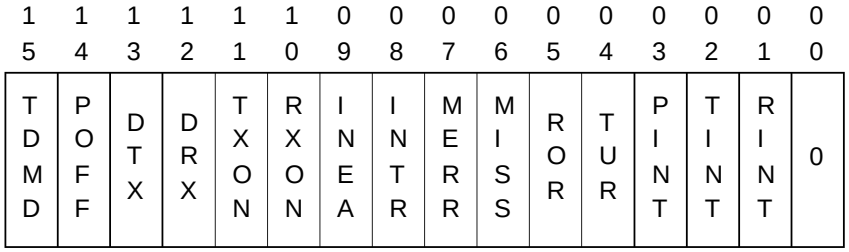


BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0



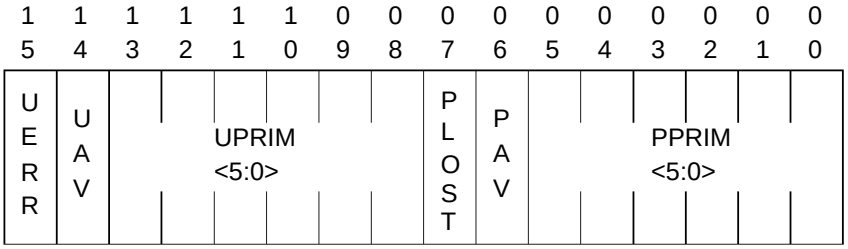
BIT	NAME	DESCRIPTION
15	TDMD	TRANSMIT DEMAND, when set, causes MK50H27 to access the Transmit Descriptor Ring without waiting for the transmit polltime interval to elapse. TDMD need not be set to transmit a MSU, it merely hastens MK50H27's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is Write With ONE ONLY and cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.
14	POFF	POFF, when set, indicates that MK50H27 is operating in the Power Off phase of operation. All external activity is disabled and internal logic is reset. MK50H27 remains inactive except for primitive processing until a Power On primitive is issued. POFF IS READ ONLY and set by Bus RESET or a Power Off primitive. Writing to this bit has no effect.
13	DTX	Transmitter ring disable prevents the MK50H27 from further access to the Transmitter Descriptor Ring and terminates transmitter polling. No transmissions are attempted after finishing transmission of any signal unit in transmission at the time of DTX being set. TXON acknowledges changes to DTX, see below. DTX is READ/WRITE.

4.1.2.1 Control and Status Register 0 (CSR0)

BIT	NAME	DESCRIPTION
12	DRX	Disable the Receiver prevents the MK50H27 from further access to the Receiver Descriptor Ring. No received signal units are accepted after finishing reception of any signal unit in reception at the time of DRX being set. RXON acknowledges changes to DRX, see below. DRX is READ/WRITE.
11	TXON	TRANSMITTER ON indicates that the transmit ring access is enabled. TXON is set as the Power On primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by sending a Power Off primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing to this bit has no effect.
10	RXON	RECEIVER ON indicates that the receive ring access is enabled. RXON is set as the Power On primitive is issued if DRX=0, or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a Power Off primitive in CSR1, or by a Bus RESET. RXON is READ ONLY; writing to this bit has no effect.
09	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0 the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit, by Bus RESET, or while in the Power Off phase. INEA may not be set while in the Power Off phase.
08	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: MISS, MERR, RINT, TINT, PINT. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a Power Off primitive.
07	MERR	MEMORY ERROR is set when the MK50H27 is the Bus Master and READY has not been asserted within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on theDAL lines. When a Memory Error is detected, the MK50H27 releases the bus, the receiver and transmitter are turned off, and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Power Off primitive.
06	MISS	MISSED MSU is set when the receiver loses a MSU because it does not own a receive buffer indicating loss of data. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Power Off primitive.
05	ROR	RECEIVER OVERRUN indicates that the Receiver FIFO was full When the receiver was ready to input data to the Receiver FIFO. The signal unit being received is lost but is recoverable according to the Link Level protocol. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Power Off primitive.

04	TUR	TRANSMITTER UNDERRUN indicates that the MK50H27 has aborted a signal unit since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a signal unit. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by RESET or by issuing a Power Off primitive.
03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive. When PINT is set, an interrupt is generated if INEA =1. PINT is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by RESET or by issuing a Power Off primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. When TINT is set, an interrupt is generated if INEA =1. TINT is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by RESET or by issuing a PowerOff primitive.
01	RINT	RECEIVER INTERRUPT is set after the MK50H27 updates an entry in the Receive Descriptor Ring. When RINT is set, an interrupt is generated if INEA =1. RINT is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Power Off primitive.
00	0	This bit is READ ONLY and will always read as a zero.

4.1.2.2 Control and Status Register 1 (CSR1)



RAP <3:1> = 1

BIT	NAME	DESCRIPTION
15	UERR	USER PRIMITIVE ERROR is set by the MK50H27 when a primitive is issued by the user which is in conflict with the current status of the link. UERR is READ/CLEAR ONLY and is set by MK50H27 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.
14	UAV	USER PRIMITIVE AVAILABLE is set by the user when a primitive is written into UPRIM. It is cleared by the MK50H27 after the primitive has been processed. This bit is also cleared by a Bus RESET.
13:08	UPRIM	USER PRIMITIVE is written by the user, in conjunction with setting UAV, to control the MK50H27 link procedures. The following primitives are available:
	0	Power Off: causes the MK50H27 to enter the Power Off state. All DMA activity ceases, the transmitter transmits all ones, and all received data is ignored. Valid in all states except Power Off.
	1	Power On: valid only in the Power Off phase and must be issued after the Init primitive and prior to the Start primitive. Causes the MK50H27 to exit the Power Off phase and to enter the Out of Service phase and

to continuously transmit SIOS signal units.

2 Init: instructs the MK50H27 to read the initialization block from memory. Valid only in the Power Off mode.

3 Trans: instructs the MK50H27 to enter the HDLC Transparent phase of operation. Data frames are transmitted and received out of the descriptor rings but no protocol processing is done. Address and Control fields are not prepended to the frames, but CK processing works normally. HDLC Transparent Mode may be exited only with a Power Off primitive or by a bus RESET. Valid only in the Power Off phase.

4 Status Request: instructs the MK50H27 to write the current link status into the STATUS BUFFER. Valid in all states, but only after the Init primitive has been previously issued.

5 Self-Test Request: instructs the MK50H27 to perform the built in internal self test. Valid only in the Power Off phase. See section 4.4.8 for the self test procedure.

6 Stop: forces all DMA activity to cease. Causes the MK50H27 to enter the Out of Service phase and to continuously transmit SIOS signal units. Valid in all phases except the Power Off and Out of Service phase.

7 Start: initial alignment begins and the descriptor rings are reset. Start should only be issued when in the Out of Service phase, after the initialization block has been read.

8 Local Processor Outage: issued to the MK50H27 to indicate that level 3 or higher levels cannot accept signalling messages. All subsequent MSU's are ignored by the MK50H27 & SIPO signal units are transmitted.

9 Local Processor Recovered: indicates end of Local Processor Outage condition. The MK50H27 may resume transmitting FISUs and MSUs.

10 Emergency: indicates that the emergency proving period is to be used for initial alignment.

11 Emergency Ceases: Indicates that the normal proving period is to be used for initial alignment (this is the default proving period).

12 Retrieve BSNT: causes the entire STATUS BUFFER to be updated including the last transmitted Backward Sequence Number (BSNT). When completed, PPRIM 18 will be issued.

13 Retrieval request and FSNC: indicates that the FSNC has been written to the Status Buffer and requests the MK50H27 to update the retransmission buffer. The MK50H27 should then place the updated retransmission index into the Status Buffer.

14 Congestion: causes the MK50H27 to enter a congestion state and send SIB signal units at T5 timer interval. It is recommended that the DRX bit in CSR0 also be set when issuing this primitive so that MSUs cannot be received during congestion.

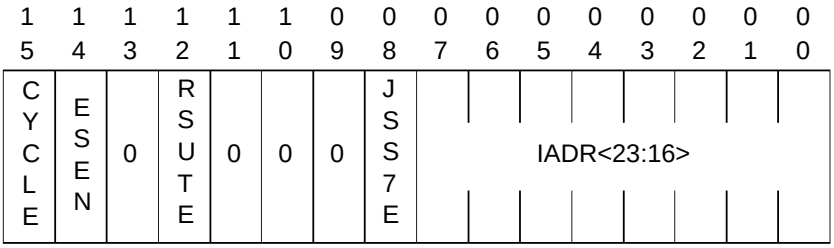
15 Clear Congestion: This primitive should be used only to clear the Congestion state caused by UPRIM 14. If DRX is set, it should be cleared just prior to issuing this primitive. If congestion state was entered due to a MISSed signal unit then the congestion state should be cleared by clearing MISS.

16 Start Sending SIOS: If JSS7E=1, this primitive can be used to resume sending of SIOS signal units, stopped by issuance of UPRIM 17. Valid only in Out Of Service phase when JSS7E=1 (CSR2).

17 Stop Sending SIOS: If JSS7E=1, this primitive can be used to stop the transmission of SIOS signal units while the MK50H27 is in the Out of Service phase. *TTC specification JT-Q703 requires that transmission of SIOS stop some period of time after going Out Of Service; this primitive provides the mechanism for meeting that requiremnt. Transmis-*

		sion of SIOS can be resumed by issuing UPRIM 16 described above. Valid only in Out Of Service phase when JSS7E=1 (CSR2).
07	PLOST	PROVIDER PRIMITIVE LOST is set by MK50H27 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared and by a Bus RESET. Writing to this bit has no affect.
06	PAV	PROVIDER PRIMITIVE AVAILABLE is set by the MK50H27 when a new provider primitive has been placed in PPRIM. PPRIM is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET. Under normal operation the host should clear the PAV bit after PPRIM is read.
05:00	PPRIM	PROVIDER PRIMITIVE is written by the MK50H27, in conjunction with setting the PAV bit, to inform the user of link control conditions. Valid Provider Primitives are as follows:
	0	Init Confirmation: indicates that the initialization has completed.
	1	In Service: indicates that alignment has completed successfully.
	2	In Service Yellow: indicates alignment completed succesfully with CCITT Yellow Book definitions for SINs & SIEs (SF = 9 & 10 respectively). This primitive will occur only if enabled by RYEL=1 in Protocol Options.
	3	Transmit Clock Watchdog Timer Expired: indicates that the watchdog timer for TCLK has expired due to no transition on TCLK for more than the number of SYSCLK cycles as selected by CSR4<15:14>.
	4	Receive Clock Watchdog Timer Expired: indicates that the watchdog timer for RCLK has expired due to no transition on RCLK for more than the number of SYSCLK cycles as selected by CSR4<13:12>.
	5	Received SU Timer timeout: indicates that no signal units have been received within the previous 32xTP time (where TP is the poll timer). This primitive is only issued if RSUTE=1 (CSR2<12>).
	8	Alignment Out of Service: indicates that a transfer to Out of Service phase has occured, due to an alignment failure. Alignment will fail if AERM is exceeded, timer T2 times out, or timer T3 times out.
	9	LSSU Out of Service: indicates that a transfer to the Out of Service phase has occured, due to a received LSSU.
	10	T1 Out of Service: indicates that a transfer to the Out of Service phase has occured, due to a timer T1 time out.
	11	Transmit Out of Service: indicates that a transfer to the Out of Service phase has occured, due to a transmit link failure. The transmit link will fail if timers T6 or T7 time out.
	‘ 12	Receive Out of Service: indicates that a transfer to the Out of Service phase has occured due to receive link failure. A receive link failure will occur when more than 2 out of 3 signal units have a FIB or BSN error.
	13	SUERM Out of Service: indicates that a transfer to the Out of Service phase has occured, due to SUERM being exceeded.
	16	Remote Processor Outage: indicates that a SIPO has been received indicating that a remote processor outage condition has occured.
	17	Remote Processor Outage Recovered: an FISU or an MSU has been received since remote processor outage condition has been reported.
	18	Received message BSNT: indicates that the MK50H27 has written the BSNT to the Status Buffer as requested by UPRIM 12.
	19	Retrieval complete: retrieval request and FSNC completed successfully. The pointer to the retransmission buffer is available in STATUS buffer.
	20	Remote Processor Busy: an SIB has been received indicating that the remote node has entered into congestion.
	21	Remote Processor Busy Recovered: the remote node has acknowledged

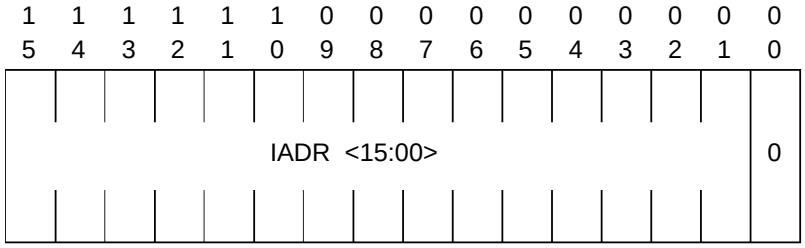
the receipt of an MSU after having entered congestion. This primitive indicates that the remote node congestion has abated.



4.1.2.3 Control and Status Register 2 (CSR2)

RAP<3:1> = 2

BIT	NAME	DESCRIPTION
15	CYCLE	Setting this bit selects a shorter DMA cycle (5 vs 6 SYSCLKs for bursting or 5 vs 7 SYSCLKs for single DMA). See Figures 7a and 8a for details.
14	ESEN	Extended Scaler Enable. Setting this bit enables the use of the 16-bit timer pre-scaler at IADR+24 rather than the 8-bit Scaler at IADR+02. Using the 16-bit Scaler allows longer timer values at higher SYSCLK rates. Set ESEN=0 for backward compatibility with the MK50H27.
13	0	Reserved, must be written as zeroes.
12	RSUTE	Received SU Timer Enable. Setting this bit enables a timer for detecting more than 32xTP time between received Signal Units. If RSUTE=1, PPRIM=5 will be issued upon expiry of the Received SU Timer. A typical use for RSUT is to detect breaking of the serial data connection.
11:09	0	Reserved, must be written as zeroes.
08	JSS7E	Japanese SS7 Enable. Setting this bit enables TTC JT-Q703 compliance. When JSS7E=1 the MK50H27 will align using only SIEs, timers Tf, Ts, To, Ta, and Te will be activated appropriately, and the SUERM will act in accordance with JT-Q703 requiring interchanging the location of the T and D fields in the Initialization Block. *If JSS7E=1 the MK50H27 will NOT comply with all CCITT/ITU, ANSI, or AT&T specifications.*
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.



4.1.2.4 Control and Status Register 3 (CSR3)

RAP<3:1> = 3

BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization block must begin on a word boundary.

4.1.2.5 Control and Status Register 4 (CSR4)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
XWD1	XWD0	RWD1	RWD0	0	0	FWM		BAE	BUSR	BSWPC	BURST	1:0	BSWPD	ACON	BCON

CSR4 allows redefinition of the bus master interface.
RAP<3:1> = 4

BIT	NAME	DESCRIPTION
15:12	XWD0/1, RWD0/1	These bits enable and determine the timer values for the Transmit and Receive Watchdog Timers. These timers are independently programmable and are reset by any transition on the TCLK and RCLK pins respectively. The Watchdog timers will expire after approximately Wn SYSCLK cycles (if not reset by transition on TCLK / RCLK pins) and Provider Primitive 3 or 4 will be issued. The following table shows the selections for Wn:

XWD1/RWD1	XWD0/RWD0	Wn
0	0	Disabled
0	1	2^{18}
1	0	2^{19}
1	1	2^{20}

11:10	0	Reserved, must be written as zero.
09:08	FWM	These bits define the FIFO watermarks. FIFO watermarks prevent the MK50H27 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive data, data will only be transferred to the data buffers after the FIFO has at least N 16-bit words or an end of signal unit has been reached. Conversely, for transmit data, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows:

FWM<1:0>	N
11	1 word
10*	9 words
01	17 words
00	25 words

* Suggested setting

07	BAE	Bus Address Enable: if BAE is set then the A23-A20 pins are driven by the MK50H27 constantly providing the ability to use A23-A20 for memory bus selection. If clear, A23-A20 behave identically to A19-A16.
06	BUSR	If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear then pin 15 is either BM0 or BYTE depending on bit 00. For more information see the description for pin 15 in this document. BUSR is READ/WRITE and cleared on bus Reset.
05	BSWPC	This bit determines the byte ordering of all "non-data" DMA transfers.

"Non-data DMA transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows the MK50H27 to operate with memory organizations that have bits 07:00 at even addresses and with bits 15:08 at odd addressses or vice versa. BSWPC is Read/Write and cleared by BUS RESET.
With BSWPC = 1:

This memory organization is used with the 8086 family of microprocessors.
With BSWPC = 0:

This memory organization is used with the 68000 and the Z8000 microprocessors.

04:03 BURST — This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on bus Reset.

BURST <1:0>	8 bit mode	16 bit mode
00	2 bytes	1 words
10*	16 bytes	8 words
01	unlimited	unlimited

* Suggested setting

02 BSWPD — This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.

01 ACON — ALE CONTROL defines the assertive state of pin 18 when the MK50H27 is a Bus Master. ACON is READ/ WRITE and cleared by Bus RESET.

ACON	PIN18	NAME
0	ASSERTED HIGH	ALE
1	ASSERTED LOW	$\overline{AS}$

00 BCON — BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN16	PIN15	PIN17
0	$\overline{BM1}$	$\overline{BM0}$	HOLD
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

4.1.2.6 Control and Status Register 5 (CSR5)

CSR5 facilitates control and monitoring of modem controls.
RAP<3:1> = 5

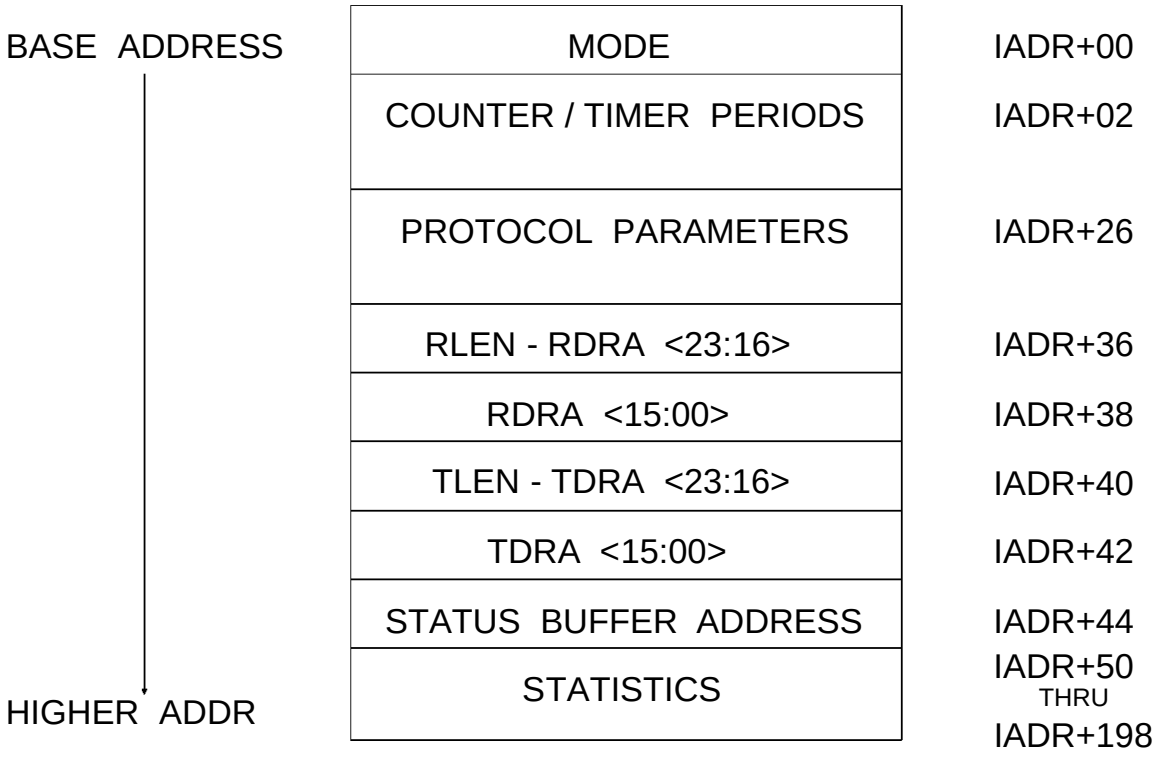
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	XEDGE	RTSEN	DTRD	DSRD	DTR	DSR

BIT	NAME	DESCRIPTION
15:05	0	Reserved, must be written as zeroes.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set, pin 26 becomes RTS and pin 30 becomes CTS. RTS is driven low whenever the MK50H27 has data to transmit and is kept low during transmission. RTS will be driven high after the closing flag of a signal unit is transmited if either no other frames are in the FIFO or if the minimum signal unit spacing is higher than 2 (see Mode Register). The MK50H27 will not begin transmission and TD will remain HIGH if CTS is high. If RTSEN = 0 then pins 26 and 30 become programmable I/O pins DTR and DSR. The direction and behavior of DSR and DTR are controlled by the following bits.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR pin. If DTRD = 0, the DTR pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR pin. If DSRD = 0, the DSR pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR pin.
0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR pin. If DSRD = 1 this bit becomes READ/WRITE and any value written to this bit appears on the DSR pin.

4.2 Initialization Block

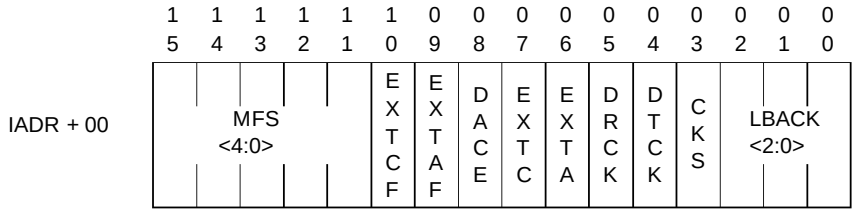
MK50H27 initialization includes the reading of the initialization block in memory to obtain the operating parameters. The Initialization Block is defined below. Upon receiving an Init primitive, portions of the Initialization block are read by the MK50H27. The remainder of the Initialization block will be read as needed by the MK50H27.

Figure 4: Initialization Block



4.2.1 Mode Register

The Mode Register allows alteration of the MK50H27's operating parameters.



BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK50H27. This only affects frames transmitted by the MK50H27 and does not restrict the spacing of the frames received by the MK50H27. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See the following table for encoding of this field.

NUMBER OF FLAGS	MFS<4:0>	NUMBER OF FLAGS	MFS<4:0>
1	1	32	28
2	0	34	24
4	2	36	17
6	4	38	3
8	9	40	6
10	18	42	13
12	5	44	27
14	11	46	23
16	22	48	14
18	12	50	29
20	25	52	26
22	19	54	21
24	7	56	10
26	15	58	20
28	31	60	8
30	30	62	16

10	EXTCF	Extended Control Force. Must be reset to zero for both SS7 and HDLC transparent mode
09	EXTAF	Extended Address Force. If set along with EXTA, the receiver will assume the address to be two otets long regardless of the first bit of the address. See EXTA below. Must be set to a 1 for SS7 operation. Must be reset to a zero for HDLC transparent mode.
08	DACE	Disable Address and Control field Extraction. DACE should be written with "0" for normal SS7 operation and with "1" for HDLC Transparent mode. The MK50H27 however, has a feature to allow shifting of the alignment of the data in the MSU buffers. If DACE is set to "1" for SS7 mode, the received LI will be placed in the first byte of the receive buffer, followed by the SIO in the second byte and so on. If DACE = 1, on transmit the LI must be placed in the first byte of the transmit buffer rather than in the SUL field of the Transmit Descriptor Entry (TMD2).
07	EXTC	Extended Control Field. Must be reset to zero for both SS7 and HDLC transparent mode.
06	EXTA	Extended address Field. Must be set to a 1 for SS7 operation. Must be reset to a zero for HDLC transparent mode.

05	DRCK	Disable Receiver CK. When DRCK = 0, the receiver will extract and check the CK field at the end of each signal unit. When DRCK = 1, the receiver continues to extract the last 16 or 32 bits of each signal unit, depending on CKS, but no check is performed to determine whether the CK is correct. The CK is not stored into the Receive buffer.
04	DTCK	Disable Transmitter CK. When DTCK = 0, the transmitter will generate and append the CK to each signal unit. When DTCK = 1, the CK logic is disabled, and no CK is generated with transmitted signal units. Setting DTCK=1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect CK.
03	CKS	CK Select. When CKS = 1, the 16 bit CK is selected otherwise the 32 bit CK is used.
02:00	LBACK	Loopback Control puts the MK50H27 into one of several loopback configurations.

LBACK	DESCRIPTION
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock. Transmit clock must be supplied externally
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with td pin forced to all ones.
7	Silent clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. The TD pin is forced to all ones.

4.2.2 Timers

There are ten independent counter-timers defined in SS7. The upper 8 bits of IADR+02 are used as a scaler for T1 through T7, and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is the maximum number of signal units allowed for retransmission (transmission window size) and N2 is the maximum number of bytes allowed for retransmission. The value for N1 is set to 128.

The Host will write the period of N2, T1-T7, and TP into the Initialization Block.

TIMER	DESCRIPTION
SCALER	TIMER PRESCALER. Timers T1-T7 and TP are scaled by this number. The prescaler is incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. The MK50H27 multiplies this value by 16 when it is read into the device. Note: a prescale value of one gives the smallest amount of scaling to the timers (512 clock pulses), zero gives the largest (131584 clock pulses).
N2	Octet window size. N2 gives the maximum number of MSU octets allowed for retransmission. N2 includes the opening and closing flags, BSN/BIB, FSN/FIB, LI, and the CK octets. This value is expressed as a positive integer. Bits <14:8> of IADR + 02 represent the most significant bits of N2.
T1	ALIGNED READY TIMER PERIOD. T1 determines the maximum time the MK50H27 will stay in the ALIGNED READY state before signalling link failure. Represented as two's complement.
T2	NOT ALIGNED TIMER PERIOD. T2 determines the maximum time the MK50H27 will wait in the NOT ALIGNED state before signalling link failure. Represented as two's complement.

T3	ALIGNED TIMEOUT TIMER PERIOD. T3 determines the maximum time the MK50H27 will wait in the ALIGNED state before signalling link failure. Represented as two's complement.
T4n	NORMAL PROVING PERIOD. T4n determines the length of the normal proving period as defined in CCITT Q.703. Represented as two's complement.
T4e	EMERGENCY PROVING PERIOD. T4e determines the length of the emergency proving period as defined in CCITT Q.703. Represented as two's complement.
T5	BUSY TRANSMIT PERIOD. T5 determines the amount of time the MK50H27 will wait between transmissions of status indication "B" while in congestion state. Represented as two's complement.
T6	EXCESSIVE BUSY TIMER PERIOD. T6 determines the amount of time the MK50H27 will allow a remote site to remain in the congested state before signalling link failure. Represented as two's complement.
T7	EXCESSIVE ACKNOWLEDGE TIMER PERIOD. T7 determines the maximum amount of time the MK50H27 will wait for an expected acknowledgement of an MSU before signalling link failure. Represented as two's complement.
TP	TRANSMIT POLLING PERIOD. This scaled timer determines the length of time between transmit signal unit checks. Unless TDMD (see CSR0) is set or a signal unit is received on the link, no attempt to transmit a signal unit in the transmit descriptor ring is made until TP expires. At TP expiration all transmit signal units in the transmit descriptor ring are sent. Represented as two's complement.
RESERVED/ 16-bit Scaler	Can be programmed as all zeroes for compatibliity with existing MK50H27 applications. However, if ESEN=1 (CSR2<14>), then this field is defined as a 16-bit scaler for all of the timers, and it will be used instead of the Scaler at IADR+02. This prescaler is incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. This 16-bit scaler is NOT multiplied by 16 when read into the MK50H27.

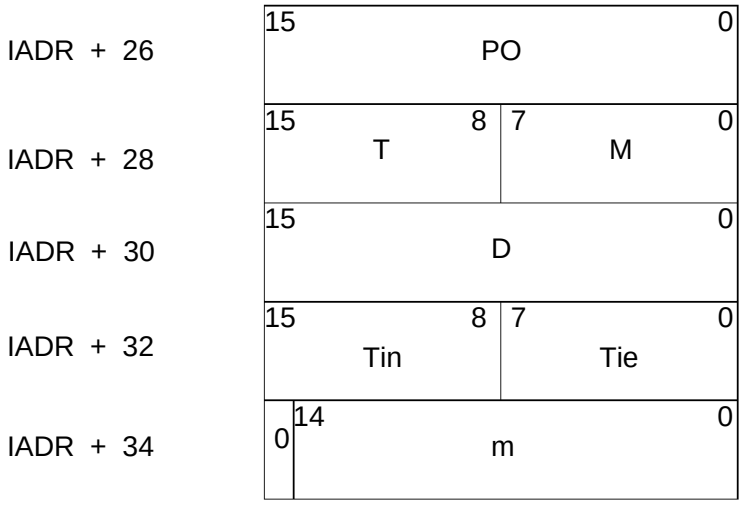
Timers For Optional TTC JT-Q703 Compliance

Tf	FISU Sending Interval timer. This timer, located at **IADR + 144** will determine the amount of time between transmission of FISUs when in TTC JT-Q703 compliant mode (CSR2<08> JSS7E=1). Represented as two's complement.
Ts	SIOS Sending Interval timer. This timer, located at **IADR + 146** will determine the amount of time between transmission of SIOS signal units when in TTC JT-Q703 compliant mode (CSR2<08> JSS7E=1). Represented as two's complement.
To	SIO Sending Interval timer. This timer, located at **IADR + 148** will determine the amount of time between transmission of SIOsignal units when in TTC JT-Q703 compliant mode (CSR2<08> JSS7E=1). Represented as two's complement.
Ta	SIE Sending Interval timer. This timer, located at **IADR + 150** will determine the amount of time between transmission of SIE signal units when in TTC JT-Q703 compliant mode (CSR2<08> JSS7E=1). Represented as two's complement.

Note: The Tf, Ts, To, & Ta timers are only active and valid when JSS7E=1 (CSR2<08>).

IADR + 02	0	14 8 Counter N2	7 0 SCALER
IADR + 04	15 0 COUNTER N2		
IADR + 06	15 0 TIMER T1		
IADR + 08	15 0 TIMER T2		
IADR + 10	15 0 TIMER T3		
IADR + 12	15 0 TIMER T4n		
IADR + 14	15 0 TIMER T4e		
IADR + 16	15 0 TIMER T5		
IADR + 18	15 0 TIMER T6		
IADR + 20	15 0 TIMER T7		
IADR + 22	15 0 TIMER TP		
IADR + 24	15 0 RESERVED / 16-Bit SCALER (if ESEN=1)		

4.2.3 Protocol Parameters



PARM **DESCRIPTION**

PO PROTOCOL OPTIONS. Defines the SS7 protocol options to be used.

BIT	NAME	DEFINITION
00	DBUSY	DBUSY = 1: Disables busy mechanisms on both transmit and receive. Missed MSU interrupts (CSR0<06>, MISS) are not affected by this bit.
01	XYEL	XYEL= 0: Transmitted SINs and SIEs conform to CCITT Red/Blue Book definitions (SF = 1 and 2 respectively). XYEL= 1: Transmitted SINs and SIEs conform to CCITT Yellow Book definitions (SF = 9 & 10 respectively).
02	RYEL	RYEL= 0: Only CCITT Red/Blue Book definitions for received SINs and SIEs are accepted. RYEL= 1: Either CCITT Yellow or Red/Blue Book definitions for received SINs and SIEs are accepted.
03	RMODE	Defines the retransmission method to be used. RMODE = 0: specifies Basic Error Recovery (BEC). RMODE = 1: specifies Preventive Cyclic Redundancy(PCR).
04	BECDOUBLE	Provides double transmission of all MSUs in BEC. All MSU's including those sent during negative acknowledgement are transmitted twice. If RMODE= 0 then the following definitions apply: BECDOUBLE = 0: specifies normal BEC. BECDOUBLE = 1: specifies BEC with doubletransmission. NOTE: BECDOUBLE must be 0 if RMODE = 1.
05	ERMEN	Enables the AERM and SUERM error rate monitors. ERMEN = 0: disables the AERM and SUERM. ERMEN = 1: enables the AERM and SUERM.
06	OCTEN	Enables octet counting. OCTEN = 0: disables octet counting. OCTEN = 1: enables octet counting.
07	2/3EN	Enables 2/3 errored FIB/BSN error monitoring. 2/3EN = 0: disables 2/3 error monitoring. 2/3EN = 1: enables 2/3 error monitoring.
08	ANSIT6/T7	Selects ANSI or ITU compliance for SS7 T6 & T7 timers ANSIT6/T7 =0: T6 & T7 timer operation complies with ITU Q.703 ANSIT6/T7 =1: T6 & T7 timer operation complies with ANSI T1.111.3
15-09		RESERVED Must be programmed with all zeroes.

T / *TTC D*	SUERM THRESHOLD. Number of consecutive signal units received in error that will cause an error rate high indication. *When operating in TTC compliant mode (CSR2 JSS7E=1), this field should contain the D value (typically 16) used for TTC JT-Q703 SUERM operation.*
M	PROVING ABORT LIMIT. Number of consecutive aborted proving periods that cause the MK50H27 to return to the OUT-OF-SERVICE state.
D / *TTC T*	SUERM ERROR RATE. The lowest acceptable number of signal units per signal unit error. *When operating in TTC compliant mode (CSR2 JSS7E=1), this field should contain the T SUERM Threshold value (typically 285) used for TTC JT-Q703 SUERM operation.* This field should be expressed as a two's complement value.
Tin	NORMAL AERM THRESHOLD. Number of signal unit errors that cause the abortion of a normal proving period.
Tie	EMERGENCY AERM THRESHOLD. Number of signal unit errors that cause the abortion of an emergency proving period.
m	Maximum frame length. Number of bytes allowed in the information portion of received MSUs before octect counting begins.

NOTE:

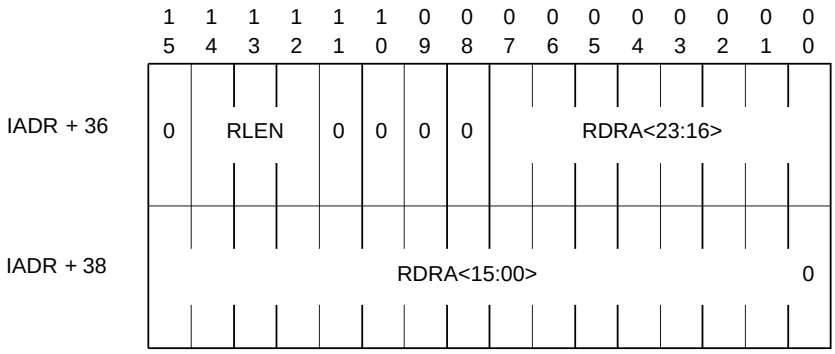
The operation of the SUERM (Signal Unit Error Rate Monitor) is different between CCITT / ITU compliant systems and TTC JT-Q703 compliant systems. Although both SUERM schemes operate based upon a leaky bucket principle, there are some major differences in their implementation.

For CCITT/ITU Q.703 the SUERM count is incremented by 1 for each errored SU received until a threshold T (typically 64) is reached, at which time a link failure is declared.. For every D (typically 256) good SUs received the SUERM Count, Cs, is decremented by 1 (not to go less than 0).

For TTC JT-Q703 the SUERM count is updated once every monitor time Te (typically 24 ms) regardless of the number of SUs received during the time Te. If the last SU received was errored, then the SUERM count is incremented by D (typically 16) when Te expires. If the last SU received was good, then the SUERM count is decremented by 1 (not to go less than 0) when Te expires. If the SUERM count should ever reach the threshold T (typically 285), then a link failure is declared. For the MK50H27 the value used for time Te is the same value as programmed for time Tf (typically 24 ms for both).

Due to this difference in SUERM operation, the fields in the MK50H27 Initialization Block that are used for D and T are exchanged if JSS7E=1 selecting Japanese SS7 (TTC JT-Q703 compliance).

4.2.4 Receive Descriptor Ring Pointer

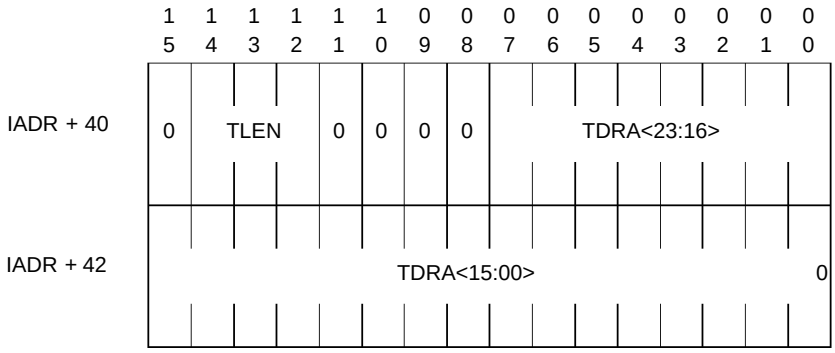


BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	RLEN	RECEIVE RING LENGTH is the number of entries in the Receive Descriptor Ring expressed as a power of two.

RLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

11:08	0	Reserved, must be written as zeroes.
07:00/15:00	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Receive Descriptor Ring. The Receive Descriptor Address must begin on a word boundary.

4.2.5 Transmit Descriptor Ring Pointer



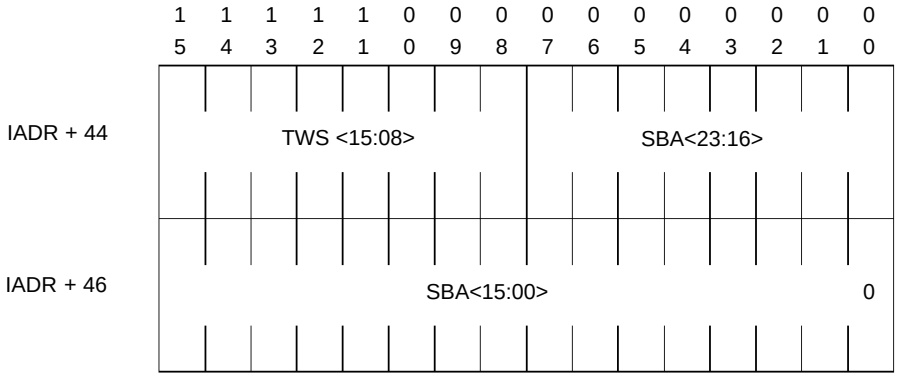
4.2.5 Transmit Descriptor Ring Pointer (continued)

BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	TLEN	TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

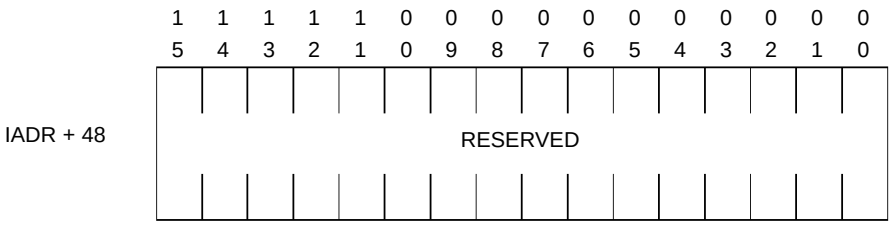
11:08	0	Reserved, must be written as a zero.
07:00/15:00	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring. The Transmit Descriptor Ring Address must begin on a word boundary.

4.2.6 Status Buffer Address



BIT	NAME	DESCRIPTION
15:08	TWS	TRANSMIT WINDOW SIZE is used to determine the maximum number of MSUs that can be transmitted without acknowledgement. For compliance with Japanese TTC JT-Q703 this value should typically be 40. For compliance with CCITT/ITU Q.703 this value should be 127. *For compatibility with the original MK50H27, this field may be programmed with all zeroes, causing the MK50H27 to use a default value of 127 as did the MK50H27.*
07:00/15:00	SBA	STATUS BUFFER ADDRESS points to the status buffer into which link status information is placed upon the issuance of the Status Request primitive by the HOST. The status buffer must begin on a word boundary.

4.2.7 Reserved



BIT	NAME	DESCRIPTION
15:00	0	Reserved, must be written as zeroes.

4.2.8 Statistics

A significant portion of the initialization buffer is reserved for statistical information collected by the MK50H27. When a statistic is updated, the MK50H27 will read the appropriate statistic, increment it, and then write it back out to memory. These statistics are intended for the use of the Host CPU for statistical analysis. The MK50H27 will only increment these counters; it is up to the user to clear and preset these counters. The statistics collected are:

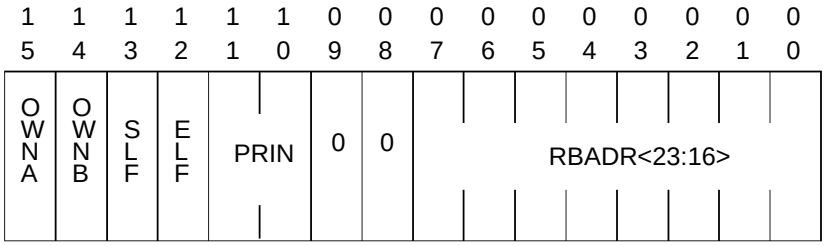
Memory Address	Error Counter
IADR + 50	SL Failure - number of link failures due to abnormal FIB/BSN received.
IADR + 52	SL Failure - number of link failures due to excessive delays of acknowledgement caused by timer T7 time out.
IADR + 54	SL Failure - number of link failures due to excessive SUERM error rate.
IADR + 56	SL Failure - number of link failures due to excessive congestion caused by timer T6 time out.
IADR + 58	Number of alignment failures due to timers T2 or T3 timing out.
IADR + 60	Number of alignment failues due to AERM exceeded.
IADR + 62	Number of negative acknowledgements received.
IADR + 64	Number of Signal Units in error.
IADR + 66 - 122	Reserved. Must be programmed as zeroes.
IADR + 124	Number of SIB's transmitted.
IADR + 126	Number of SIB's received.
IADR + 128	Number of forced retransmissions caused by N1.
IADR + 130	Number of forced retransmissions caused by N2.
IADR + 132	Number of MSU's retransmitted.
IADR + 134	Number of MSU octets retransmitted. This value includes the opening and closing flags, BSN/BIB, FSN/FIB, LI, and the CK octets.
IADR + 136 - 198	Reserved. Must be programmed as zeroes.
Note:	
IADR+144 - 151	Used for TTC JT-Q703 compliant timers Tf, Ts, To, and Ta if JSS7E=1. See page 27 for details.

4.3 Receive and Transmit Descriptor Rings

Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

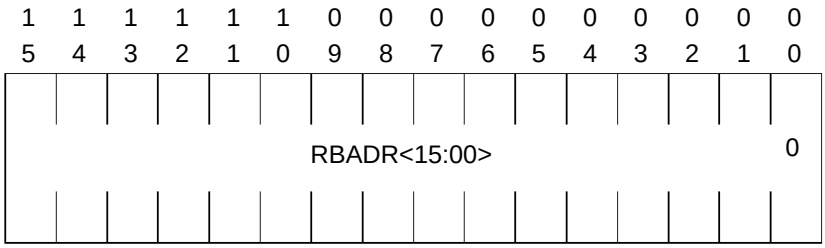
4.3.1 Receive Message Descriptor Entry

4.3.1.1 Receive Message Descriptor 0 (RMD0)



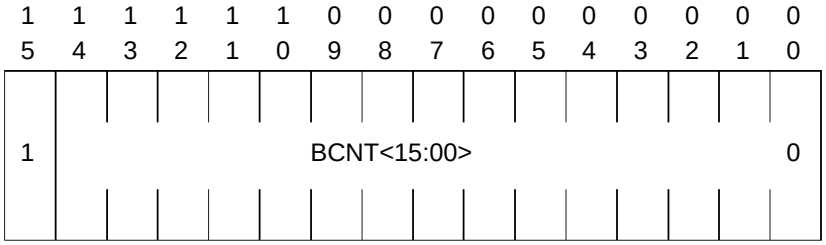
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK50H27 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided a valid signal unit has been received. The Host sets the OWNA bit after emptying the buffer. Once the MK50H27, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the Host or the Layer 3 I/O Processor owns the buffer when OWNA is a zero. The MK50H27 never uses this bit. This bit is provided to facilitate use of a Layer 3 I/O processor.
13	SLF	Start of Long Signal Unit indicates that this is the first buffer used by MK50H27 for this signal unit. It is used for data chaining buffers. SLF is set by the MK50H27. NOTE: A "Long Signal Unit" is any MSU which needs data chaining.
12	ELF	End of Long Signal Unit indicates that this the last buffer used by MK50H27 for this signal unit. It is used for data chaining buffers. If both SLF and ELF were set, the signal unit would fit into one buffer and no data chaining would be required. ELF is set by the MK50H27.
11:08	0	Reserved, must be written as zeroes for CCITT/ITU compliant operation.
11:10	PRIN	These bits indicate the content of the Priority Indication bits of the received frame when JSS7E=1 (TTC JT-Q703 compliant mode).
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H27.

4.3.1.2 Receive Message Descriptor 1 (RMD1)



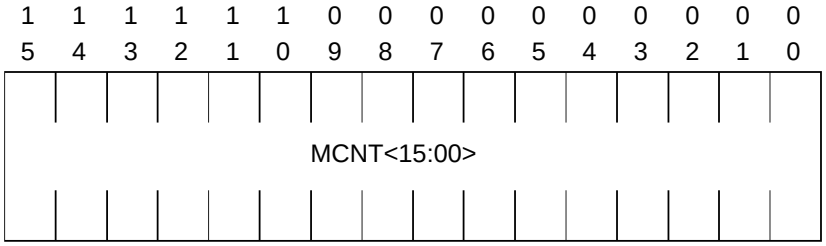
BIT	NAME	DESCRIPTION
15:01	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK50H27. The receive buffers must be word aligned.

4.3.1.3 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK50H27. The value of BCNT must be an even number.

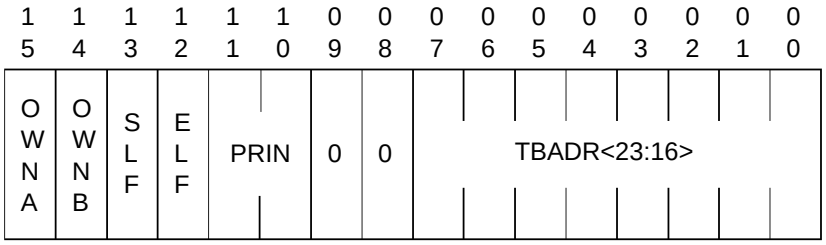
4.3.1.4 Receive Message Descriptor 3 (RMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the received signal unit. MCNT is valid only when ELF is set to a one. MCNT is written by MK50H27 and read by the Host. If ELF is set to a zero the entire buffer has been utilized and the message byte count is given in BCNT above. The value of this field is expressed in two's complement.

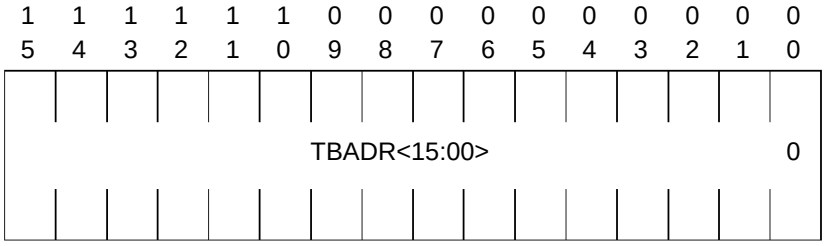
4.3.2 Transmit Message Descriptor Entry

4.3.2.1 Transmit Message Descriptor 0 (TMD0)



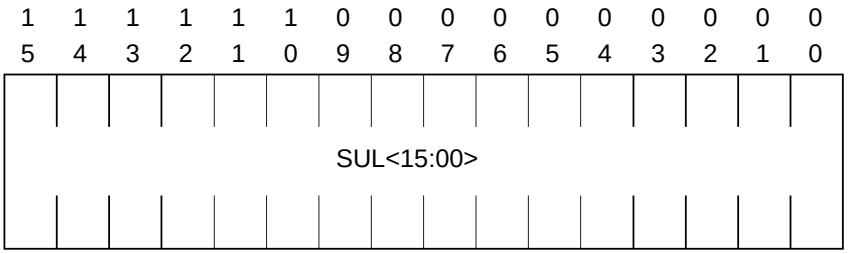
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK50H27 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK50H27 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the receiver. After the MK50H27, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the Host or the Layer 3 I/O Processor owns the buffer when OWNA is a zero. The MK50H27 never uses this bit. This bit is provided to facilitate use of a Layer 3 I/O processor.
13	SLF	Start of Long Signal Unit indicates that this is the first buffer used by the MK50H27 for this signal unit. It is used for data chaining buffers. SLF is set by the Host. When not chaining, SLF should be set to a one. NOTE: A "Long Signal Unit" is any MSU which needs data chaining.
12	ELF	End of Long Signal Unit indicates that this is the last buffer used by the MK50H27 for this signal unit. It is used for data chaining buffers. If both SLF and ELF were set the signal unit would fit into one buffer and no data chaining would be required. ELF is set by the Host. When not chaining, ELF should be set to a one.
11:08	0	Reserved, must be written as zeroes for CCITT/ITU operation.
11:10	PRIN	These bits determine the content of the Priority Indication bits of the transmitted frame when JSS7E=1 (TTC JT-Q703 compliant mode).
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H27.

4.3.2.2 Transmit Message Descriptor 1 (TMD1)



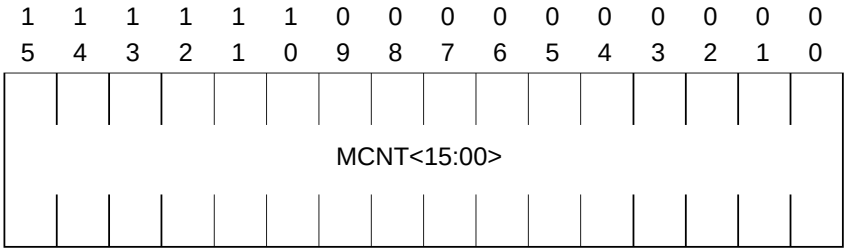
BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor TBADR is written by the Host and unchanged by MK50H27. The least significant bit is zero since the descriptor must be word aligned.

4.3.2.3 Transmit Message Descriptor 2 (TMD2)



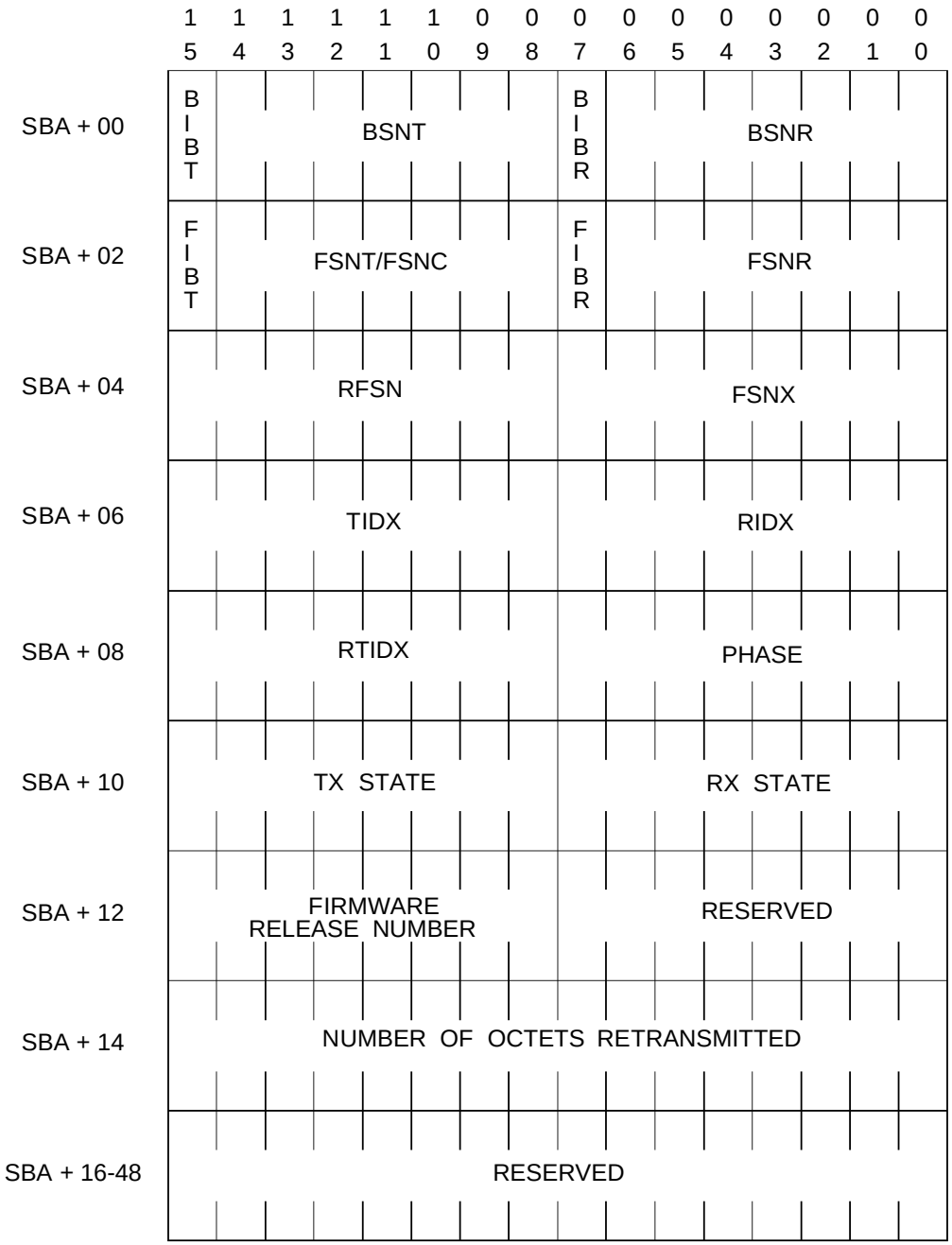
BIT	NAME	DESCRIPTION
15:00	SUL	Signal Unit Length. Only required when in the first descriptor of a signal unit (SLF = 1) and when DACE = 0. Contains the length of the SIF and the SIO fields of the signal unit, in octets, to be transmitted. The value of this field is expressed as a positive integer.

4.3.2.4 Transmit Message Descriptor 3 (TMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in octets, of the data contained in the corresponding buffer. The value of this field is expressed in two's complement.

Figure 4a: MK50H27 Status Buffer



4.3.3 Status Buffer

FIELD	DESCRIPTION
BIBT	The value of the last BIB transmitted.
BSNT	The value of the last BSN transmitted. 0 ≤ BSNT ≤ 127.
BIBR	The value of the last BIB received.
BSNR	The value of the last BSN received. 0 ≤ BSNR ≤ 127.
FIBT	The value of the last FIB transmitted.
FSNT/FSNC	Under normal operation this is the value of the last FSN transmitted. If a UPRIM 13 is to be issued in CSR1 then the FSNC value to be read by the MK50H27 must be placed here by the host. 0 ≤ FSNT/FSNC ≤ 127.
FIBR	The value of the last FIB received.
FSNR	The value of the last FSN received. 0 ≤ FSNR ≤ 127.
RFSN	The value of the oldest unacknowledged FSNT in the retransmission buffer. 0 ≤ RFSN ≤ 127.
FSNX	The value of the next expected FSN to be received. 0 ≤ FSNX ≤ 127.
TIDX	Index to the descriptor of the current transmission buffer.
RIDX	Index to the descriptor of the current receive buffer.
RTIDX	Index to the first descriptor of the retransmission buffer.
PHASE	Indicates the current phase of operation for the device. 0:Power Off. 2:Out of Service. 4: Initial alignment not aligned. 5:Initial alignment aligned. 6:Initial alignment proving. 7:Alignment not ready. 8:Alignment ready. 9:In Service. 10:Processor outage. 11:Transparent mode. 12:Memory Error.
TX STATE	Indicates the current state of the transmitter. 0: The transmitter is waiting to transmit a Signal Unit. 1:A Signal Unit is currently being transmitted. 2:A Signal Unit transmission has completed.
RX STATE	Indicates the current state of the receiver. 0:The receiver is expecting the beginning of a Signal Unit. 1:A MSU is being transferred to the receive buffer(s). 2:End of frame detected. 3:Receive data being ignored. 4:Buffer chaining requested.
FIRMWARE RELEASE NUMBER	Indicates the release number of the firmware within the MK50H27.
NUMBER OF OCTETS RETRANSMITTED	This value represents the lower two bytes of the total number of octets retransmitted. The number of octets retransmitted statistics counter represents the upper two bytes of the total number of octets re-transmitted. This two byte status buffer value together with the two byte error counter value provide a 32 bit value for the total number of octets retransmitted.
RESERVED	Must be programmed as ZEROES.

4.4 Detailed Programming Procedures

4.4.1 Initialization

The following procedure should be followed to intialize the MK50H27:

1. Setup bus control information in CSR4.
2. Setup the Initialization Block and Desciptor Rings.
3. Load the address of the initialization block information into CSR's 2 and 3.
4. Issue the INIT primitive through CSR1 instructing the MK50H27 to read the initialization block pointed to by CSR's 2 and 3.
5. Wait for the INIT confirmation primitive from the MK50H27.
6. For SS7 operation, issue the PON primitive through CSR1, SIOS's will now be continuously transmitted. For HDLC Transparent mode, issue the TRANS primitive through CSR1, flags will now be continously transmitted.
7. Enable interrupts in CSR0 if desired.

4.4.2 Alignment

1. For SS7 operation issue the START primitive through CSR1 to begin alignment.
2. Wait for the IN SERVICE provider primitive.

4.4.3 Sending Data

Use the following procedure to send a MSU:

1. Wait for the OWNA bit of the current transmit descriptor to be cleared, if it is not already.
2. Fill the buffer associated with the current transmit descriptor with the data to be sent, or set the descriptor buffer address to any already filled buffer.
3. Repeat steps 1 and 2 for the next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.

4.4.4 Receiving Data

The following procedure should be followed when receiving a MSU:

1. Make sure the OWNA bit of the current receive descriptor is clear.
2. Read data out of the buffer associated with the current receive descriptor.
3. Set the OWNA bit of the current receive descriptor.
4. If the ELF bit of the current receive descriptor is clear, then go on to the next descriptor and repeat the above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

4.4.5 Link Disconnection

The following procedure should be followed to disconnect an established link:

1. For SS7 operation, issue the STOP primitive through CSR1. The MK50H27 will enter the Out of Service state and continuously transmit SIOS's.

4.4.6 Disabling the MK50H27

The following procedure should be followed to disable the MK50H27:

1. Issue the POFF primitive through CSR1. This will disable the MK50H27 from receiving or transmitting. The TD pin will be held high while the MK50H27 is in the Power Off state. The POFF bit in CSR0 will be set and interrupts will be disabled. If a link is currently established, then data may be lost.

4.4.7 Re-enabling the MK50H27

The same procedure should be followed for re-enabling the MK50H27 as was used to initalize upon power up. If the Initialization Block and the hardware configuration have not changed, then steps 1,2,3, 4 and 5 of the intialization sequence may be omitted.

4.4.8 MK50H27 Internal Self Test

The MK50H27 contains an easy to use internal self test designed to test, with a high fault coverage, all of the major blocks of the device except the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute the internal self test:

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK50H27.
5. After the PAV bit is set, read CSR1. The success or failure of the test is indicated in the PPRIM field as follows:

PPRIM	RESULT
00	Passed self test.
17	Failed the reset test of the self test.
18	Failed the self test in the micro controller RAM.
19	Failed the self test in the ALU.
20	Failed the self test in the timers.
21	Failed the self test in the transmitter and/or receiver.
22	Failed the self test in the CSR's and/or bus master.
Otherwise	Failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHZ), then the MK50H27 is unable to respond to the Self Test Request and will not complete successfully.

   If the self test passes, then it may be immediately reexecuted from step 3, otherwise re-execution should proceed from step 1.

SECTION 5
ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{UB}	Temperature Under Bias	-25 to +100	°C
T_{stg}	Storage Temperature	-65 to +150	°C
V_G	Voltage on any pin with respect to ground	-0.5 to V_{CC}+0.5	V
P_{tot}	Power Dissipation	0.5	W

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0 °C to 70 °C, V_{CC} = +5 V ±5 percent unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IL}		-0.5		+0.8	V
V_{IH}		+2.0		V_{CC}+0.5	V
V_{OL}	@ IOL = 3.2 mA			+0.5	V
V_{OH}	@ IOH= -0.4 mA	+2.4			V
I_{IL}	@ VIN = 0.4 to V_{CC}			+10	mA
I_{CC}	@ TSCT = 100 ns		50		µA

CAPACITANCE

f = 1MHz

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{IN}	Capacitance on Input pins			10	pF
C_{OUT}	Capacitance on Output Pins			10	pF
C_{IO}	Capacitance on I/O pins			20	pF

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

MK50H27					-16	-25	-33	-16/25/33	
No	Signal	Symbol	Parameter	Test Condition	Min.	Min.	Min.	Max.	Units
1	SYSCLK	T_{SCT}	SYSCLK period		60	40	30	10000	ns
2	SYSCLK	T_{SCL}	SYSCLK low time		24	16	12		ns
3	SYSCLK	T_{SCH}	SYSCLK high time		24	16	12		ns
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0	0	0	8	ns
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0	0	0	8	ns
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		20	20	20		ns
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		8	8	8		ns
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		8	8	8		ns
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$	CL = 50 pF	0	0	0	8	ns
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0	0	0	8	ns
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	CL = 50 pF				13	ns
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$		5	5	5		ns

AC TIMING SPECIFICATIONS CONTINUED - MK50H27 -25

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

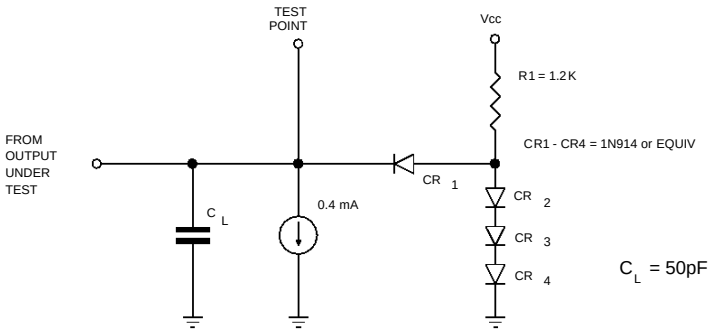
					MK50H27 -25			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
13	$\overline{\text{RCLK}}$	T_{RCT}	$\overline{\text{RCLK}}$ period		20			ns
14	$\overline{\text{RCLK}}$	T_{RCH}	$\overline{\text{RCLK}}$ high time		8			ns
15	$\overline{\text{RCLK}}$	T_{RCL}	$\overline{\text{RCLK}}$ low time		8			ns
16	$\overline{\text{RCLK}}$	T_{RCR}	Rise time of $\overline{\text{RCLK}}$		0		8	ns
17	$\overline{\text{RCLK}}$	T_{RCF}	Fall time of $\overline{\text{RCLK}}$		0		8	ns
18	RD	T_{RDR}	RD data rise time		0		8	ns
19	RD	T_{RDF}	RD data fall time		0		8	ns
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{\text{RCLK}}$		2			ns
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{\text{RCLK}}$		8			ns
22	ALE/$\overline{\text{DAS}}$	T_{DOFF}	Bus Master driver disable	Output Delay	0		20	ns
23	ALE/$\overline{\text{DAS}}$	T_{DON}	Bus Master driver enable after rising edge T1 SYSCLK	Output Delay	0		20	ns
24	$\overline{\text{HLDA}}$	T_{HHA}	Delay to falling edge of $\overline{\text{HLDA}}$ from falling edge of HOLD (Bus Master)		0			ns
25	$\overline{\text{HLDA}}$	T_{HLAH}	$\overline{\text{HLDA}}$ input setup time		10			ns
26	$\overline{\text{HLDA}}$	T_{HLAS}	Delay to rising edge $\overline{\text{HLDA}}$ from rising edge $\overline{\text{HOLD}}$		10			ns
27	A	T_{XAS}	Address setup time	Output Delay			30	ns
28	A	T_{XAH}	Address hold time	Output Delay			20	ns
29	DAL	T_{AS}	Address setup time	Output Delay			35	ns
30	DAL	T_{AH}	Address hold time	Output Delay	0		20	ns
31	DAL	T_{RDAS}	Data setup time (Bus Master read)		15			ns
32	DAL	T_{RDAH}	Data hold time (Bus Master read)		10			ns
33	DAL	T_{WAH}	Address hold time (Bus Master write)	Output Delay			15	ns
34	DAL	T_{WDS}	Data setup time (Bus Master write)	Output Delay			25	ns
35	DAL	T_{WDH}	Data hold time (Bus Master write)	Output Delay			25	ns
36	DAL	T_{SRDS}	Data setup time (Bus Slave read)				25	ns
37	DAL	T_{SRDH}	Data hold time (Bus slave read)				25	ns
38	DAL	T_{SWDH}	Data hold time (Bus slave write)		10			ns
39	DAL	T_{SWDS}	Data setup time (Bus slave write)		10			ns
40	ALE	T_{ALES}	ALE setup time	Output Delay			30	ns
41	ALE	T_{ALHB}	ALE hold time (asserted to de-asserted) (DMA Burst)	Output Delay			15	ns
42	ALE	T_{ALHS}	ALE hold time (asserted to 3-State) (Single DMA cycle)	Output Delay			20	ns
43	$\overline{\text{DAS}}$	T_{DASS}	DAS setup time from falling edge of T2 SYSCLK (Bus Master)	Output Delay			25	ns
44	$\overline{\text{DAS}}$	T_{DASH}	DAS hold time from rising edge of SYSCLK (Bus Master)	Output Delay	5		15	ns
45	$\overline{\text{DALI}}$/$\overline{\text{DALO}}$ BM)/BM1	T_{BMDE}	Bus Master driver enable (from 3-State to driven) (Bus Master)	Output Delay			25	ns
46	$\overline{\text{DALI}}$	T_{RIS}	$\overline{\text{DALI}}$ setup time (Bus Master read)	Output Delay			15	ns
47	$\overline{\text{DALI}}$	T_{RIH}	$\overline{\text{DALI}}$ hold time (Bus Master read)	Output Delay			25	ns
48	$\overline{\text{DALI}}$	T_{BMDD}	Bus Master driver disable (from driven to 3-State) (Bus Master)	Output Delay			20	ns

AC TIMING SPECIFICATIONS CONTINUED - MK50H27 -25

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

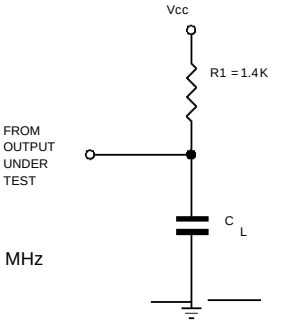
					MK50H27 -25			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
49	$\overline{\text{DALO}}$	T_{ROS}	$\overline{\text{DALO}}$ setup time (Bus Master read)	Output Delay			30	ns
50	$\overline{\text{DALO}}$	T_{ROH}	$\overline{\text{DALO}}$ hold time (Bus Master read)	Output Delay			30	ns
52	$\overline{\text{CS}}$	T_{CSH}	$\overline{\text{CS}}$ hold time		10			ns
53	$\overline{\text{CS}}$	T_{CSS}	$\overline{\text{CS}}$ setup time		10			ns
54	ADR	T_{SAH}	ADR hold time		10			ns
55	ADR	T_{SAS}	ADR setup time		10			ns
56	$\overline{\text{DAS}}$	T_{SDAS}	$\overline{\text{DAS}}$ input setup time (Bus slave)		10			ns
57	$\overline{\text{DAS}}$	T_{SDSH}	$\overline{\text{DAS}}$ input hold time (Bus slave)		10			ns
58	$\overline{\text{READY}}$	T_{RDYS}	$\overline{\text{READY}}$ setup time (Bus slave)	Output Delay			15	ns
59	$\overline{\text{READY}}$	T_{SRYH}	$\overline{\text{READY}}$ hold time after rising edge of $\overline{\text{DAS}}$ (Bus slave read)				15	ns
60	$\overline{\text{READY}}$	T_{RSH}	$\overline{\text{READY}}$ setup time (Bus Master)		18			ns
61	$\overline{\text{READY}}$	T_{SRS}	$\overline{\text{READY}}$ hold time (Bus Master)		10			ns
62	READ	T_{REDS}	READ setup time (Bus slave)		10			ns
63	READ	T_{REDH}	READ hold time (Bus slave)		10			ns
64	$\overline{\text{HOLD}}$	T_{HLDS}	$\overline{\text{HOLD}}$ setup time (Bus Master)	Output Delay			15	ns
65	$\overline{\text{HOLD}}$	T_{HLDH}	$\overline{\text{HOLD}}$ hold time (Bus Master)	Output Delay			35	ns

Figure 5a: TTL Output Load Diagram



NOTE: This load is used on all outputs except INTR, HOLD, READY.

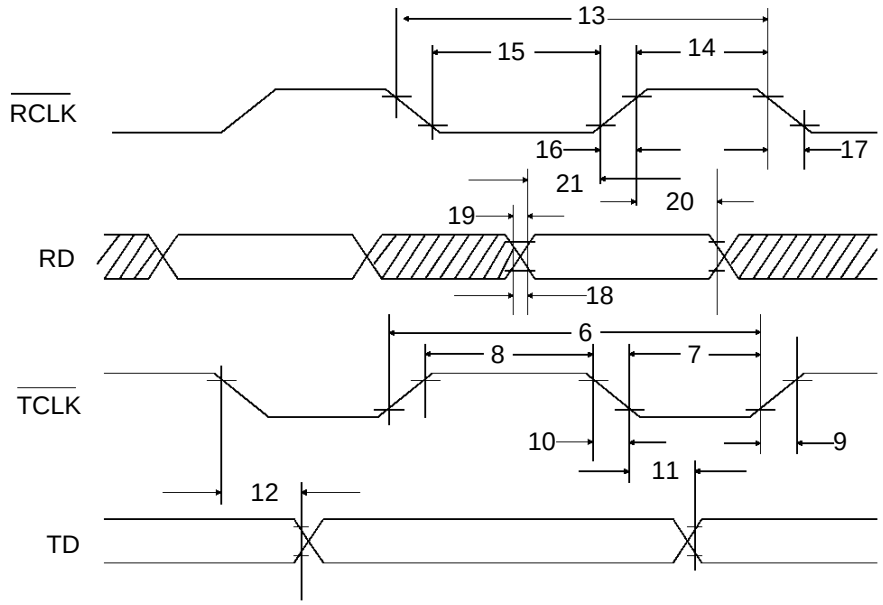
Figure 5b: Open Drain Output Load Diagram



C_L = 50pF min @ 1 MHz

NOTE: This load is used on open drain outputs $\overline{\text{INTR}}$, HOLD, READY.

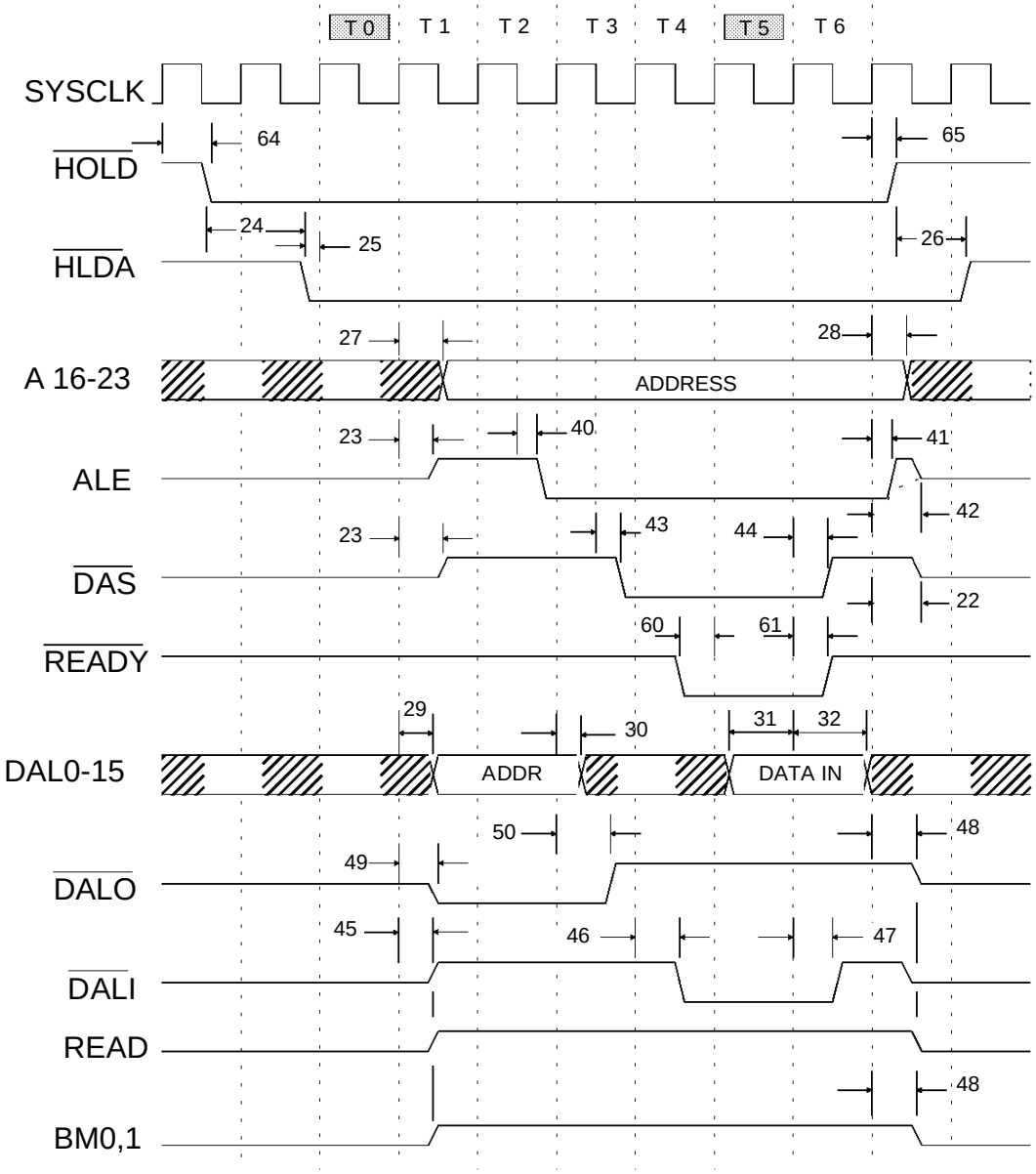
Figure 6: MK50H27 Serial Link Timing Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

	"1"	"0"
OUTPUT	2.0 V	O.8 V
INPUT	2.0 V	O.8 V
FLOAT	10 %	90 %

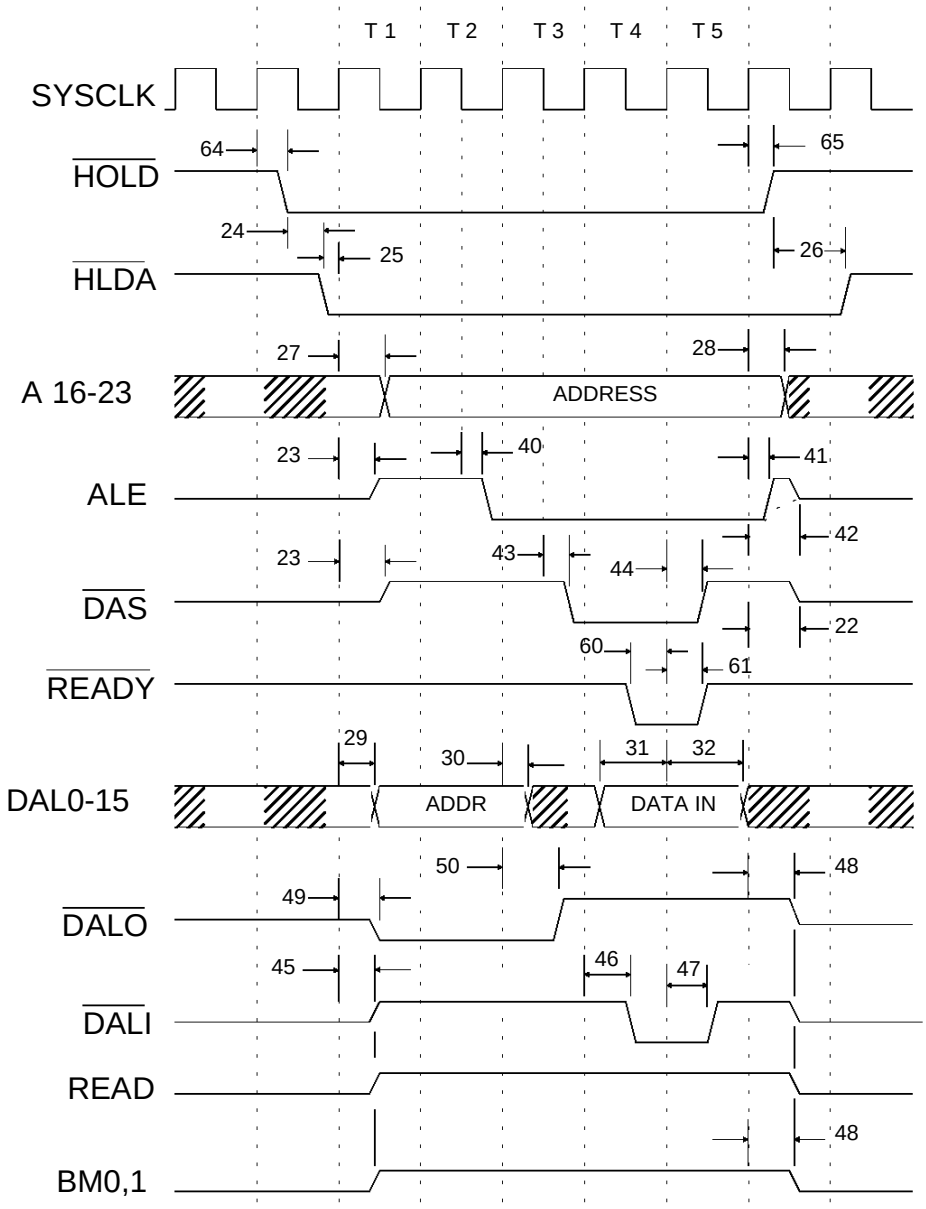
Figure 7: MK50H27 BUS Master Timing (Read) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 7a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

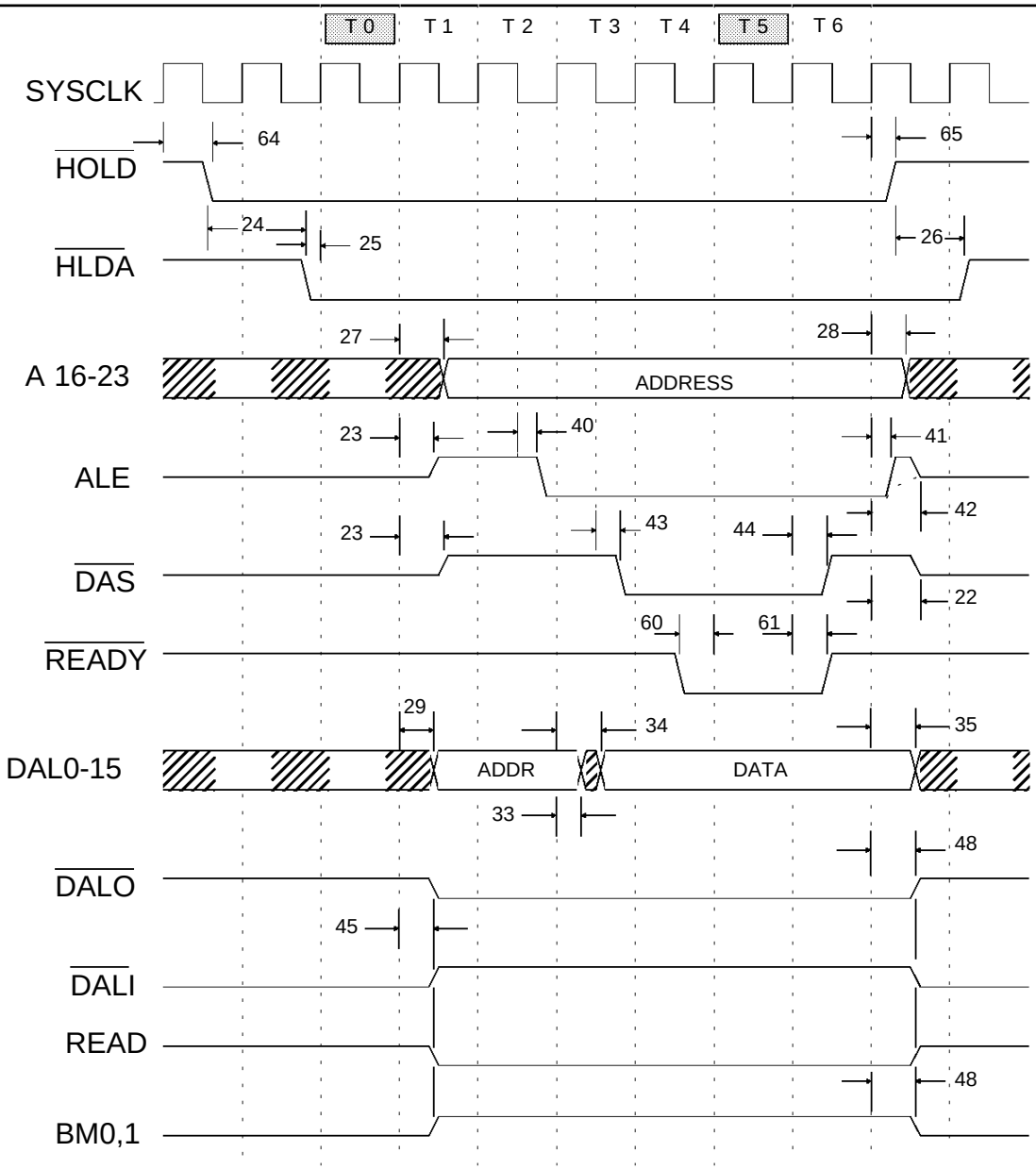
Figure 7a: MK50H27 Reduced Cycle BUS Master Timing (Read) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE =1.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

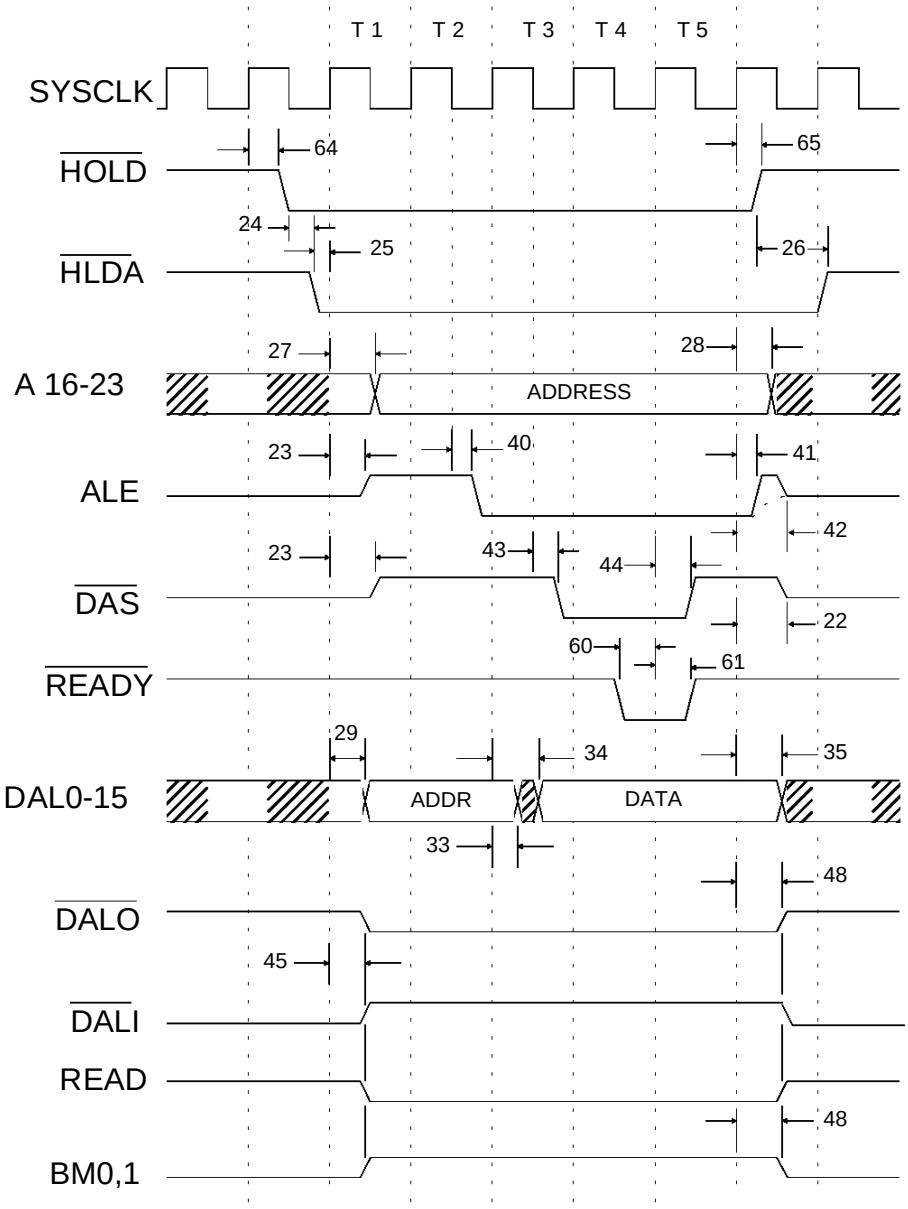
Figure 8: MK50H27 BUS Master Timing Diagram (Write) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 8a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 8a MK50H27 Reduced Cycle BUS Master Timing (Write) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This Reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE = 1. Times T0 and T5 from the standard DMA Cycle are removed for this reduced timing.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 8b: BUS Master BURST Timing (Reduced Cycle - Write)

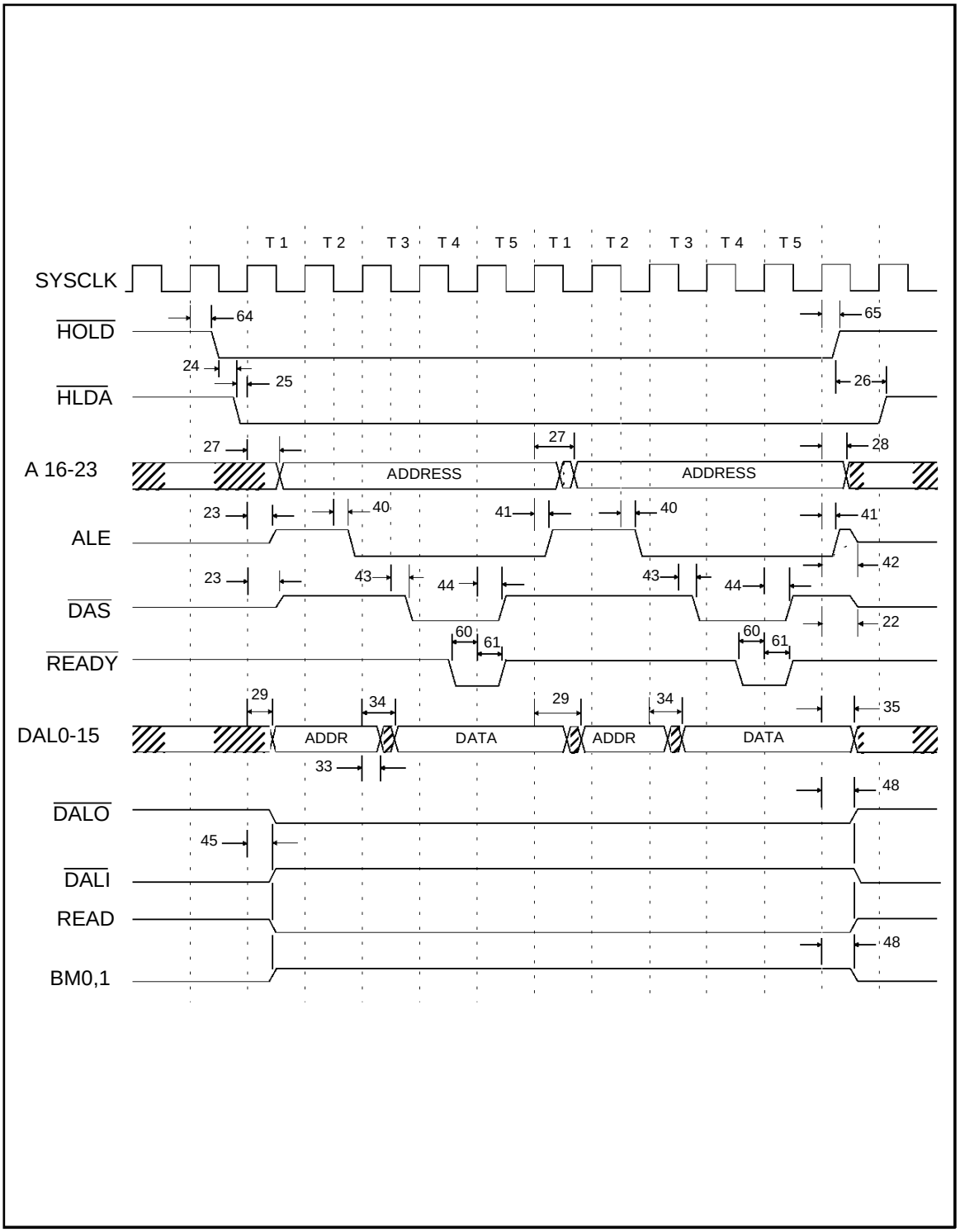
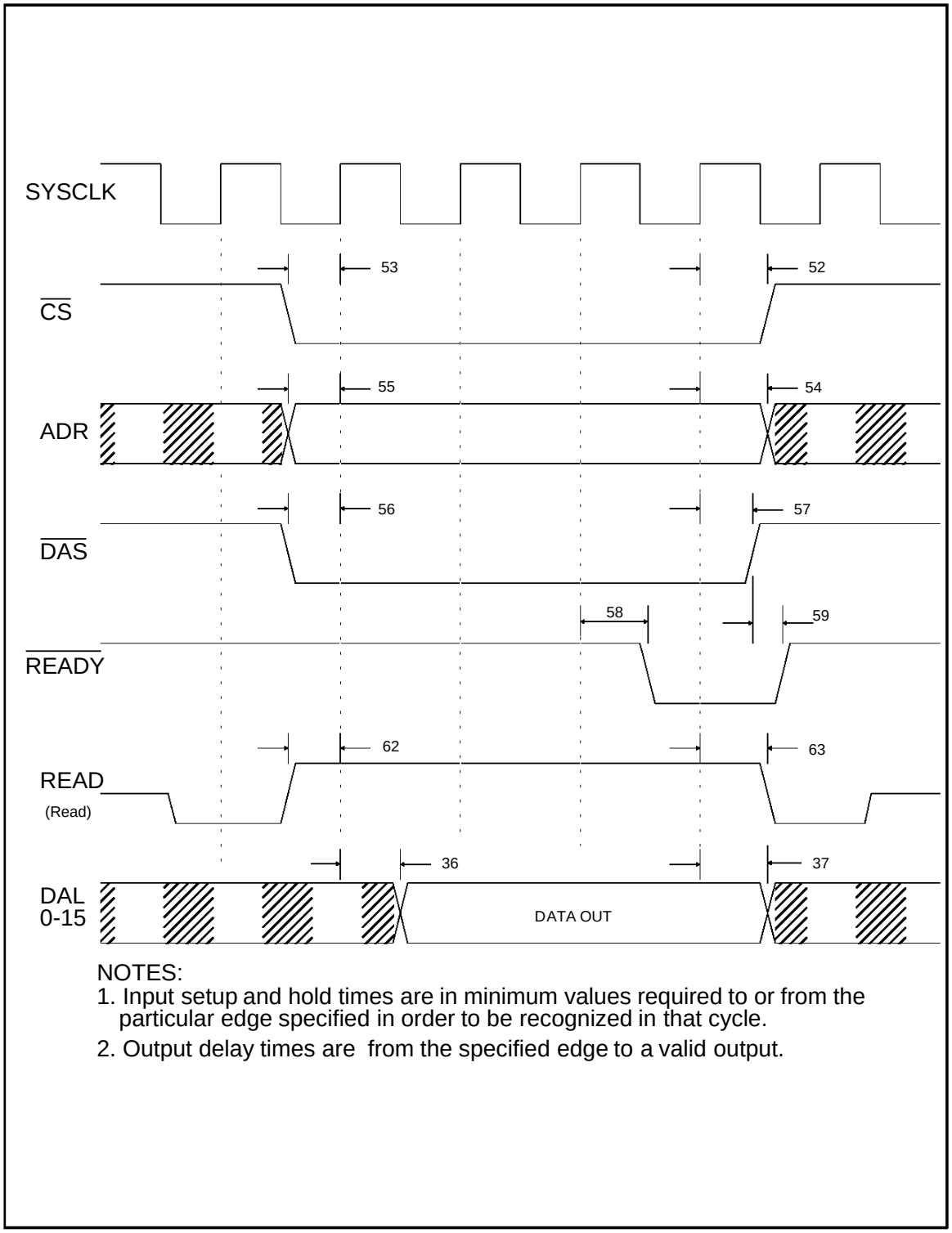
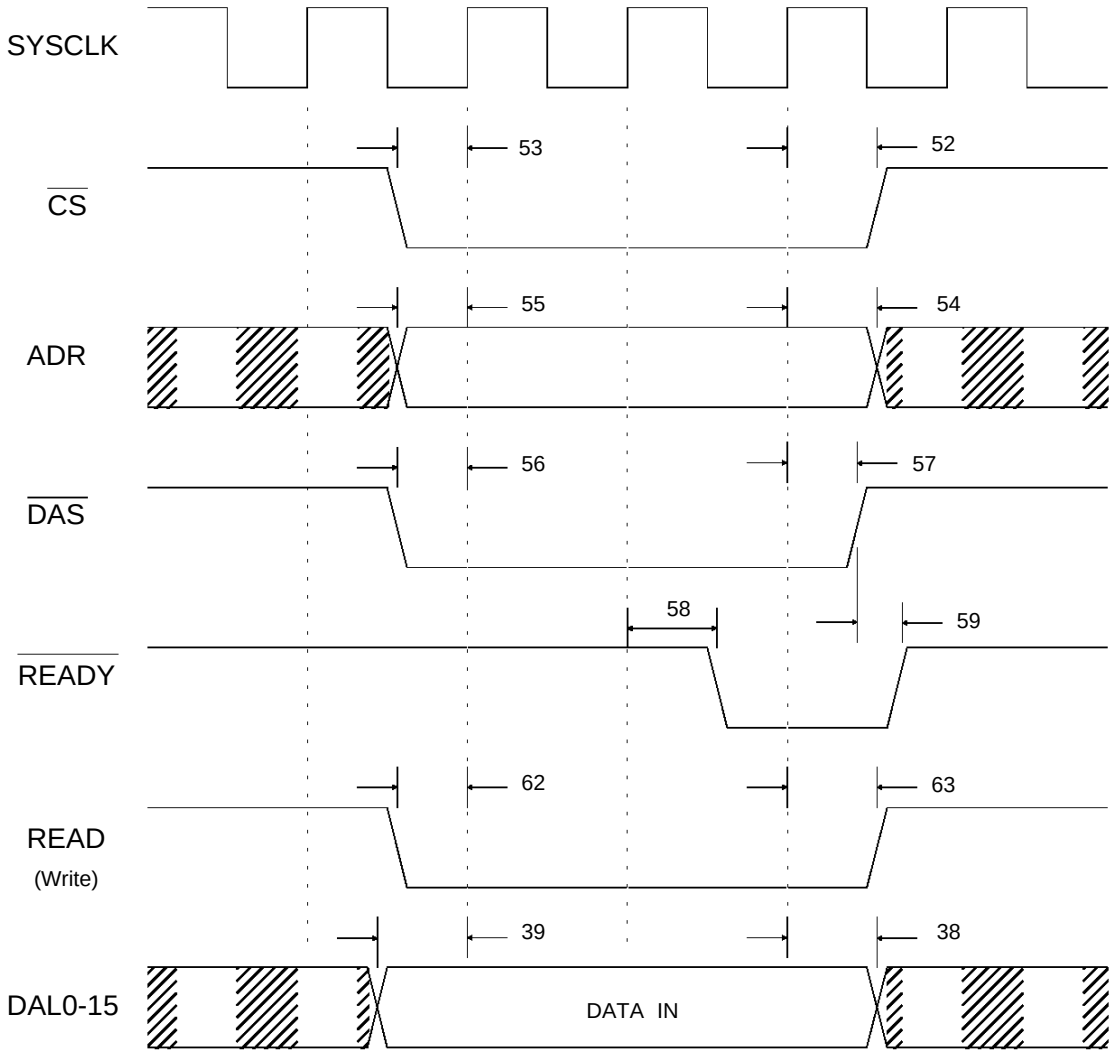


Figure 9: MK50H27 BUS Slave Timing Diagram (Read)



NOTES:
1. Input setup and hold times are in minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

Figure 10: MK50H27 BUS Slave Timing Diagram (Write)



NOTES:

1. Input setup and hold times are the minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

ORDERING INFORMATION

MK50H27 Q XX

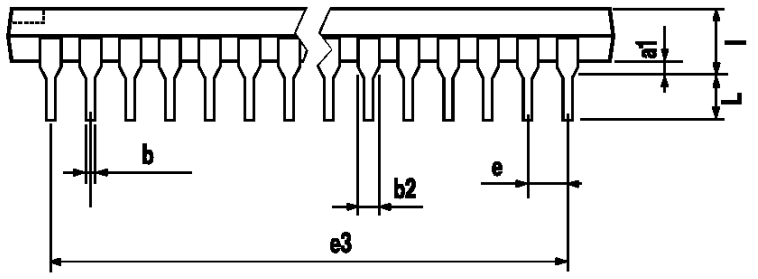
SPEED SORT
25 = 25MHz SYSCLK

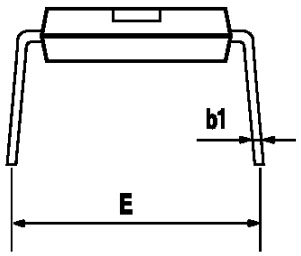
PACKAGE
N = Plastic DIP (48 Pins)
Q = Plastic J-Leaded Chip Carrier (52 Pins)

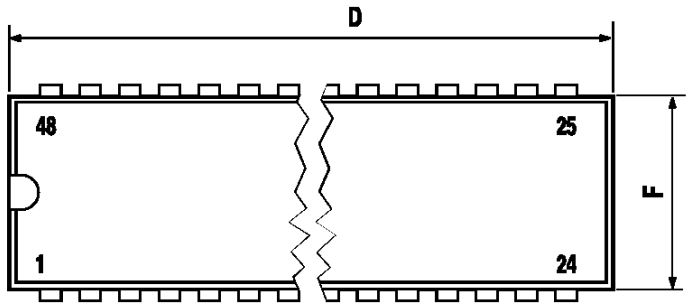
PART# PROTOCOL
50H27 = SS7 Layer 2 protocol

DIP48 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	







PLCC52 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060