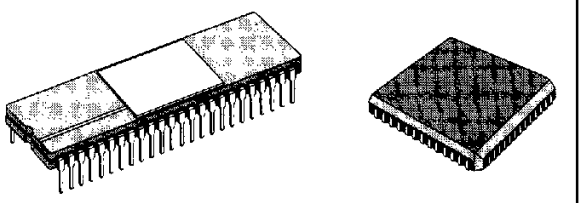
SGS-THOMSON MICROELECTRONICS

MK5025

CCITT X.25 LINK LEVEL CONTROLLER

PRELIMINARY DATA

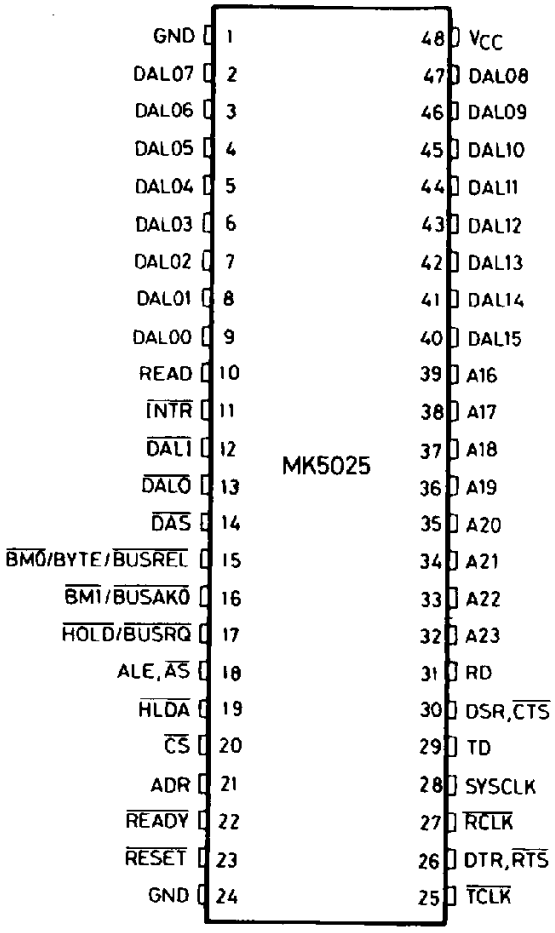
- CMOS
- FULLY COMPATIBLE WITH BOTH 8-BIT OR 16-BIT SYSTEMS
- SYSTEM CLOCK RATE TO 10MHz
- DATE RATE UP TO 7Mbps, WITH A 64-BYTE FIFO IN EACH DIRECTION
- COMPLETE DATA LINK LAYER IMPLEMENTATION
- COMPATIBLE WITH X.25 LAPB, ISDN LAPD, X.32, AND X.75 LINK LEVEL PROTOCOLS
- 48-PIN DIP NEARLY PIN-FOR-PIN COMPATIBLE WITH THE LANCE CHIP (MK7990)
- BUFFER MANAGEMENT INCLUDES :
  - initialization block
  - separate receive and transmit rings
  - variable descriptor ring and window size
- ON CHIP DMA CONTROL WITH PROGRAMMABLE BURST LENGTH
- SELECTABLE SINGLE OR EXTENDED CONTROL FIELD
- PROGRAMMABLE 1 BYTE OR 2 BYTES ADDRESS FIELD AND GLOBAL ADDRESS
- TRANSPARENT MODE WITH OR WITHOUT ADDRESS FILTERING ALLOWS DISABLING X.25 PROCESSING FOR CUSTOMIZED APPLICATIONS
- HANDLES ALL HDLC (ADCCP) FRAME FORMATTING :
  - zero bit insert and delete
  - FCS generation and detection
  - frame delimiters by flags
- FIVE PROGRAMMABLE TIMER/COUNTERS : T1, T3, TP, N1, N2
- HANDLES ALL ERROR RECOVERY, SEQUENCING, AND S AND U FRAME CONTROL
- SELECTABLE FCS OF 16 OR 32 BITS
- DATA LINK SERVICES :
  - compatible with ISO data link services
  - compatible with LAPD data link services
- TESTING FACILITIES :
  - built-in self test facility
  - 4 loopback modes
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE
- PROGRAMMABLE FOR FULL OR HALF DUPLEX OPERATION
- PROGRAMMABLE MINIMUM FRAME SPACING ON TRANSMIT (flags between frames)



CDIP48 **PLCC52**

(Order codes at the end of the datasheet)

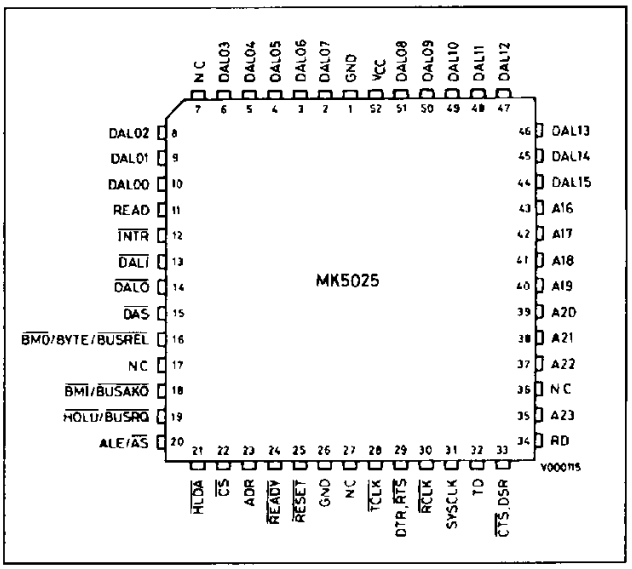
Figure 1 : MK5025 Dual in Line Pin Configuration.



GENERAL DESCRIPTION

The SGS-THOMSON X.25 Link Level Controller (MK5025) is a VLSI semiconductor device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, U (unnumbered) frame control, and S (supervisory) frame control. The MK5025 also supports X.32 (XID), X.75, and ISDN LAPD. The MK5025 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

Figure 2 : MK5025 Chip Carrier Pin Configuration.



PIN DESCRIPTIONS

DAL <07 : 00> (Input/Output ; 3-State). The time multiplexed Data/Address bus. During the address portion of the memory transfer, DAL <07 : 00> contains the lower 8 bits of the memory address. During the data portion of the memory address. During the data portion of a memory transfer, DAL <07 : 00> contains the read or write data, depending on the type of transfer.

READ (Input/Output ; 3-State). READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5025 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated by the MK5025 at all other times.

- MK5025 as a Bus Slave
  READ = HIGH - Data is placed on the DAL lines by the chip.
  READ = LOW - Data is taken off the DAL lines by the chip.
- MK5025 as a Bus Master
  READ = HIGH - Data is taken off the DAL lines by the chip.
  READ = LOW - Data is placed on the DAL lines by the chip.

$\overline{\text{INTR}}$ (Output ; Open Drain). INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set : MISS, MERR, ROR, TUR, RINT, TINT OR PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.

$\overline{\text{DALI}}$ (Output ; 3-State). DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by MK5025 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.

$\overline{\text{DALO}}$ (Output ; 3-State). DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by MK5025 when it driven the DAL lines during the data portion of a READ transfer or for the duration of a WRITE transfer.

$\overline{\text{DAS}}$ (Input/Output ; 3-State). DATA STROBE defines the data portion of a bus transaction. By definition data is stable and valid at the low to high transition of DAS. This signal is driven by the MK5025 while it is the BUS MASTER. During Bus Slave operations, this pin is used as an input. At all other times the signal is tristated.

BM0, BYTE, $\overline{\text{BUSREL}}$ (Input/Output ; 3-State). I/O pins 15 (16) and 16 (18) are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 (16) becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5025 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear the pin 15 (16) is the output BM0, and behaves as described below for pin 16 (18).

$\overline{\text{BM1}}$, $\overline{\text{BUSAKO}}$ (Output ; 3-State). Pin 15 (16) and 16 (18) are programmable through bit 00 of CSR4 (BCON).

If CSR4 <00> BCON = 0,
I/O Pin 15 (16) = $\overline{\text{BM0}}$ (Output ; 3-State)
I/O Pin 16 (18) = $\overline{\text{BM1}}$ (Output ; 3-State)

BYTE MASK <1 : 0> Indicates the byte(s) on the DAL to be read or written during this bus transition.

PIN DESCRIPTIONS (continued)

MK5025 drives these lines only as a Bus Master. MK5025 ignores the BM lines when it is a Bus Slave.

Byte selection is done as outlined in the following table :

BM1	BM0	
LOW	LOW	Entire Word
LOW	HIGH	Upper Byte (DAL <15 : 08>)
HIGH	LOW	Lower Byte (DAL <07 : 00>)
HIGH	HIGH	None

If CSR4 <00> BCON = 1,
I/O Pin 15 (16) = BYTE (Output ; 3-State)
I/O Pin 16 (18) = BUSAKO (Output)

Byte selection is done using the BYTE line and DAL <00> latched during the address portion of the bus transaction. MK5025 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table :

BYTE	DAL <00>	
LOW	LOW	Entire Word
LOW	HIGH	Illegal Condition
HIGH	LOW	Lower Byte
HIGH	HIGH	Upper Byte

BUSAKO is a bus request daisy chain output. If MK5025 is not requesting the bus and it receives HLDA, BUSAKO will be driven low. If MK5025 is requesting the bus when it receives HLDA, BUSAKO will remain high.

HOLD, BUSRQ (Input/Output ; Open Drain). Pin 17 (19) is configured through bit 0 of CSR4.

If CSR4 <00> BCON = 0
I/O Pin 17 (19) = HOLD

HOLD request is asserted by MK5025 when it requires a DMA cycle regardless of the previous state of the HOLD pin. HOLD is held low for the entire ensuing bus transaction.

If CSR4 <00> BCON = 1
I/O Pin 17 (19) = BUSRQ

BUSRQ is asserted by the MK5025 when it requires a DMA cycle if the prior state of the BUSRQ pin was high. BUSRQ is held low for the entire ensuring bus transaction.

ALE, AS. *Address Latch Enable, Address Strobe* (Output ; 3-State). The active level of Address Strobe is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by the MK5025 while it is the BUS MASTER. At all other times, the signal is tristated.

If CSR4 <00> ACON = 0
I/O PIN 18 (20) = ALE

Address Latch Enable is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion.

If CSR4 <00> ACON = 1,
I/O Pin 18 (20) = AS

As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register.

HLDA. *Hold Acknowledge* (Input). Hold Acknowledge is the response to HOLD. When HLDA is low in response to MK5025's assertion of HOLD, the MK5025 is the Bus Master. HLDA should be disasserted ONLY after HOLD has been released by MK5025.

CS. *Chip Select* (Input). Chip Select indicates, when low, that the MK5025 is the slave device for the data transfer. CS must be valid throughout the entire transaction.

ADR. *Address* (Input). Address selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when CS is low.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

READY (Input/Output ; Open Drain). When the MK5025 is a Bus Master, READY is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.

As a Bus Slave, the MK5025 asserts READY when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. READY is a response to DAS and it will be negated after DAS is negated.

PIN DESCRIPTIONS (continued)

RESET (Input). RESET is the Bus signal that will cause MK5025 to cease operation, clear its internal logic and enter an idle state with the STOP bit of CSR0 set.

TCLK. ***Transmit Clock*** (Input). A 1X clock input for transmitter timing. TD changes on the falling edge of TCLK. The frequency of TCLK may be up to 7Mbps.

DTR, RTS. Data Terminal Ready, Request to Send (Input/Output). Modem Control Pin. Pin 26 (29) is configurable through CSR5. This pin can be programmed to behave as output RTS or as programmable I/O in DTR. If configured as RTS, the MK5025 will assert this pin if it has data to send and throughout transmission of a frame.

RCLK. ***Receive Clock*** (Input). A 1X clock input for receiver timing. RD is sampled on the rising edge of RCLK. The frequency of RCLK may be up to 7MHz.

SYSCLK. ***System Clock*** (Input). Used for internal timing of the MK5025. SYSCLK should be a square wave, and be greater than 500KHz and less than 10MHz.

TD. ***Transmit Data*** (Output). Transmit serial data output.

DSR, CTS. ***Data Set Ready, Clear to Send*** (Input/Output). Modem Control Pin. Pin 30 (33) is configurable through CSR5. This pin can be programmed to behave as input CTS or as programmable I/O pin DSR. If configured as CTS, the MK5025 will transmit all 1's while CTS is high.

RD. ***Receive Data*** (Input). Received serial data input.

A <23 : 16> (Output ; 3-State). Address bits <23 : 16> used in conjunction with DAL <15 : 00> to produce a 24-bit address. MK5025 drives these lines only as a Bus Master.

DAL <15 : 08> (Input/Output ; 3-State). The time multiplexed Data/Address bus. For 16-bit operations, DAL <15 : 08> behaves similar to DAL <07 : 00> above for the high byte of data or the middle byte of the 24-bit address. For 8-bit operations,

DAL <15 : 08> behaves similar to A <23 : 16> for the middle byte of the 24-bit address only.

V_{SS}. Digital circuit ground pins.

V_{CC}. Main power supply pin (5V ± 5%).

OPERATIONAL DESCRIPTION

The SGS-THOMSON X.25 Link Controller (MK5025) device is a VLSI product intended for data communication applications requiring X.25 link level control (LAPB). The MK5025 will perform all frame formating, such as frame delimiting with flags, FCS generation and detection, as well as zero-bit insertion and delection for transparency. The MK5025 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple packets. Contained in the buffer management is an on-chip dual channel DMA : one channel for receive and one channel for transmit. The MK5025 handles all supervisory (S) and unnumbered (U) frames as shown in table 2 and table 3.

The MK5025 is intended to be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK5025 is shown in Figure 3.

The MK5025 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. An I/O acceleration processor can be used to off-load Network Level software from the Host. The I/O acceleration processor in Figure 3 is recommended, but not required.

All signal pins on the MK5025 independent of the physical interface. As shown in Figure 3, line drivers and receivers are used for electrical connection to the physical layer.

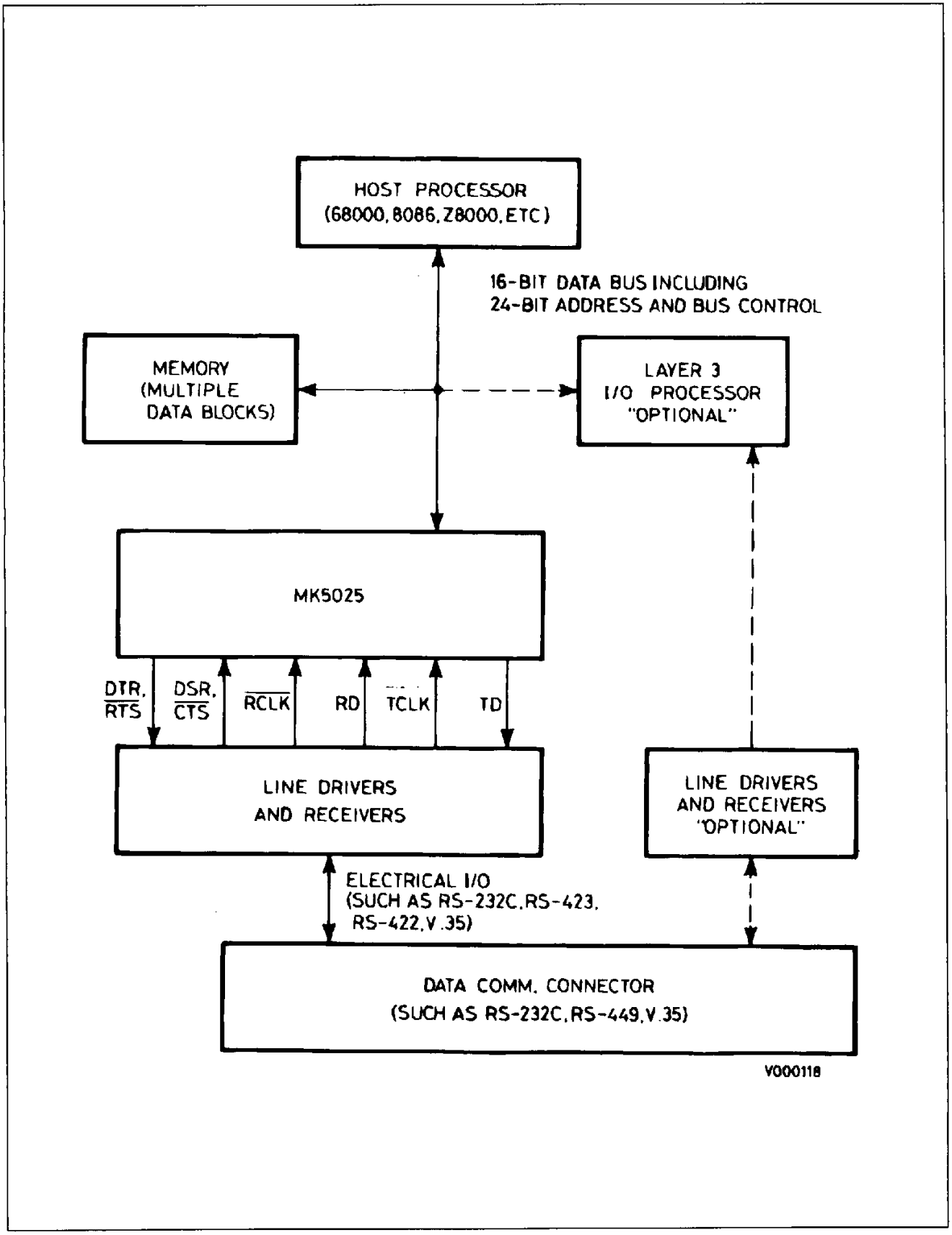
The MK5025 is mode up of functional blocks shown in Figure 4 and the MK5025 is made up of functional blocks shown in Figure 4 and described in the following paragraphs.

Microcontroller.

The microcontroller is the brain of the MK5025. It controls all of the other blocks and contains most of the protocol processing. All frame content processing as well as S and U frame processing and generation is performed by the microcontroller. All primitive processing and generation is also done here. The microcode ROM contains the control program for the microcontroller.

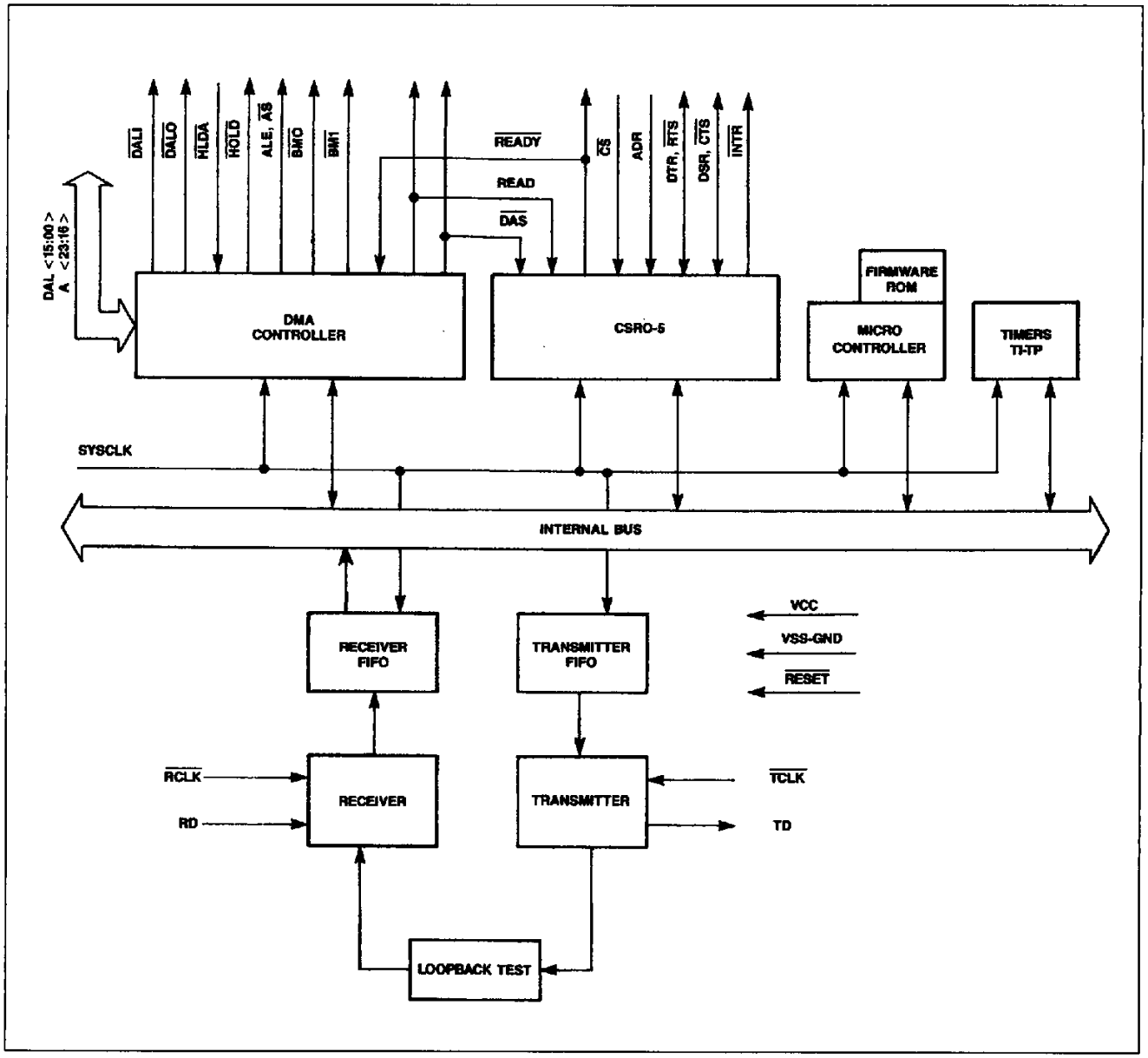
OPERATIONAL DESCRIPTION (continued)

Figure 3 : Possible System Configuration for the MK5025.



OPERATIONAL DESCRIPTION (continued)

Figure 4 : Simplified Block Diagram.



The MK5025 can interface with the host bus in two ways : either as bus master or as a bus peripheral. The MK5025 contains a dual channel DMA on chip to handle data transfers to and from the host memory. All access to the initialization block and descriptor rings is handled in this way. The address but is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations, this allows easy interfacing with both 8 and 16 bit processors. DMA transfers can be up to 1, 8 or an unlimited number of words per-transfer under program control. In bus slave mode the MK5025 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status, and more. Bus slave mode also allows both 8 and 16-bit accesses.

DMA Controller.

The MK5025 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK5025 requires access to the host memory it will negotiate

OPERATIONAL DESCRIPTION (continued)

for mastership of the bus. Upon gaining control of the bus the MK5025 will begin transferring data to or from memory. The MK5025 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case it will complete all bus transfers before releasing bus mastership back to the host. If, during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK5025 will release ownership of the bus immediately and the MERR bit will be set in CSRO. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode th limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode, it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed seperately for data and control information. Data information is defined as all contents of data buffers ; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see "Control and Status Register 4" description.

Serial Interface.

The MK5025 provides two seperate serial channels ; one for received data and one for transmitted data. These serial channels are completely seperate and may be run at different clock frequencies up to 7MHz. The receiver is responsible for recognizing frame boundaries, removal of inserted zeroes (for transparency), and checking the incoming FCS. Frames with incorrect FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring. The receiver also recognizes link idle and frame abort sequences. The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data. The transmitter generates flag sequences for interframe fill, at least two flags are transmitted between adjacent frames. The FCS calculations for both directions of serial data optionally follow either the 16-bit CRC-CCITT or the 32-bit CRC-32 algorithms. FCS generation and checking can also be optionally disabled if defined.

Receiver. Serial receive data comes into the Receiver (figure 4). The Receiver is responsible for :

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (Frame Check Sequence).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver-Over-Run.
7. Odd byte detection. If frames are received that have an odd number of bytes in the information field, the last byte of the frame is said to be an odd byte.
8. Detection of non-octet aligned frames, such frames are treated as invalid frames.

Transmitter. The Transmitter is responsible for :

1. Serialization of outgoing data.
2. Generating and appending the FCS.
3. Generation of interframe time-fill as either flags or idle.
4. Zero bit insertion for transparency.
5. Transmitter-Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS Control.

Frame Check Sequence. The FCS on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are :

- Transmitted Polarity : inverted
- Transmitted Order : High Order Bit First
- Pre-set Value : All 1's
- Polynominal 16 bit : X16 + X12 + X5 + 1
- Remainder 16 bit (if received correctly) :
  high order bit → 0001 1101 0000 1111
- Polynominal 32 bit :
  X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1
- Remainder 32 bit (if received correctly) :
  high order bit → 1100 0111 0000 0100
  1101 1101 0111 1011

OPERATIONAL DESCRIPTION (continued)

Receive FIFO. The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 2 bytes ; 18 or more bytes ; 34 or more bytes ; or 50 or more bytes. This programmability, along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK5025 must use the host bus. For more information, see Control and Status Register 4 description.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK5025 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

Transmit FIFO. The Transmit FIFO buffers the data to be transmitted by the MK5025. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to read data from the host's memory buffers in bursts ; making both the MK5025 and the host bus more efficient.

The transmit FIFO has a watermark scheme similar to the one described for the receive FIFO above. The transmit FIFO will not interrupt the microcontroller for service until it empties enough to reach the watermark level. The watermark can be programmed in CSR4 as: any space available, 18 bytes of space available, 34 bytes of space available, or 50 bytes of space available. The transmission of data however, will begin as soon as the FIFO has at least word of data

Bus Slave Circuitry

The MK5025 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in the Control and Status Registers section and the bus signal timing is described in figures 9 and 10.

Buffer Management

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in words (16 bits).

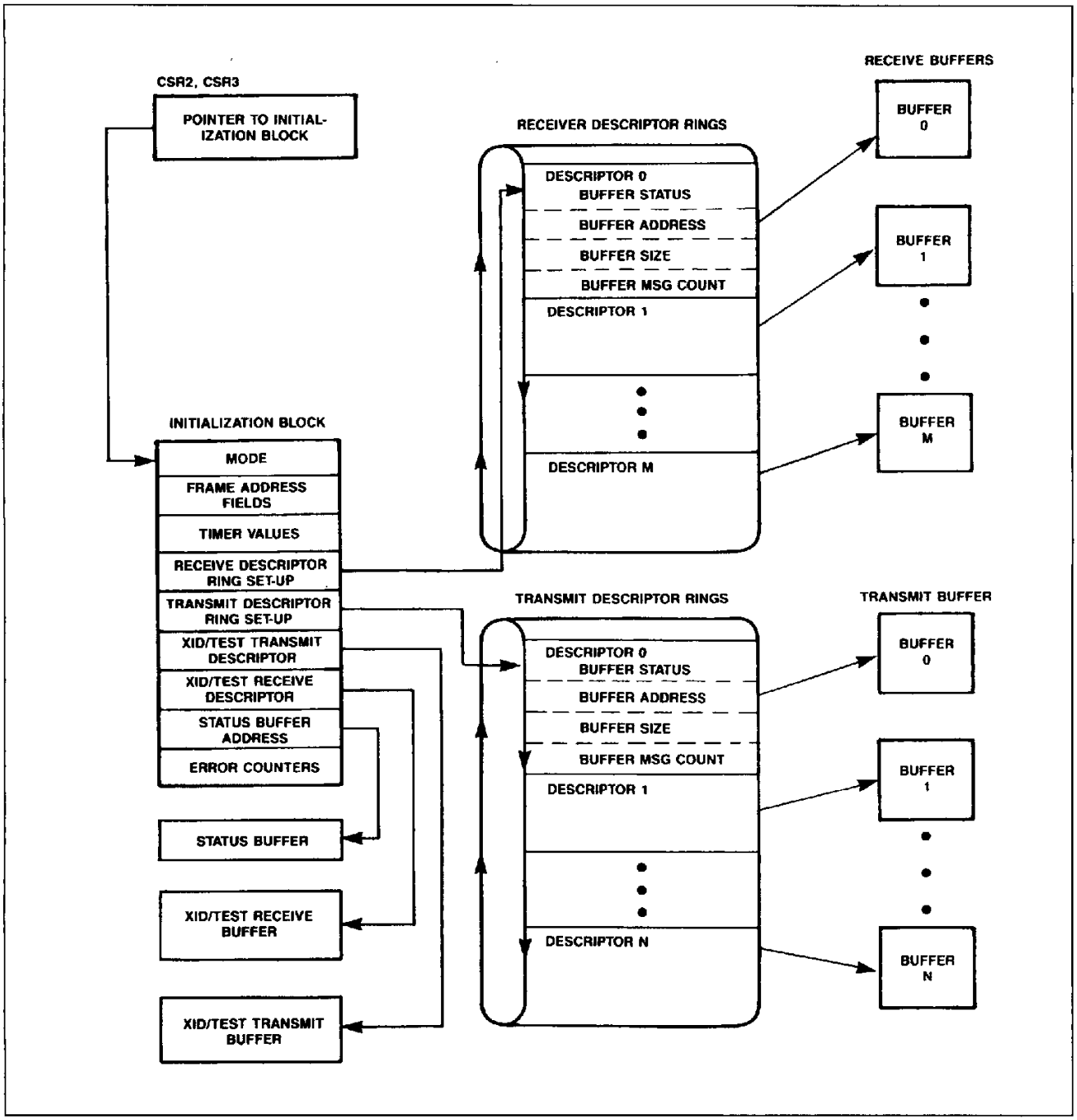
Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION Processor (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the .buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the Mk5025 does not own a receive buffer, it will not place received data in that buffer.

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer ; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc.

OPERATIONAL DESCRIPTION (continued)

Figure 5 : Buffer Management Organization.



The Initialization Block. Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 28 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST or I/O acceleration processor, and is accessed by MK5025 during initialization. The Initialization Block is comprised of :

A. Mode of Operation.

B. Frame Address Values.

C. Timer Preset Values.

D. Location and size of Receive and Transmit Descriptor Rings.

E. Location and size of XID/TEST Buffers.

F. Location of status buffer.

G. Error Counters.

OPERATIONAL DESCRIPTION (continued)

The Circular Queue. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the MK5025 does not own a receive buffer, it will not place received data in that buffer.

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the frames are too long for one buffer, the next buffer will be used after filling (or transmitting) the first buffer ; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc. The starting address for the Initialization, IADR, is defined in the CSR2 and CSR3 registers inside the MK5025.

Frame Format. The frame format used by the MK5025 is shown below. Each frame consists of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field (not in all frames), an FCS of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags is programmable through the Mode Register in the Initialization Block. Received frames may have only one flag between adjacent frames.

Transmitted First

The Command/Response Repertoire. The command/response repertoire of the MK5025 is shown in tables 2 and 3. This set conforms to the ISDN LAPD, which is a super-set of X.25 Link Level. The MK5025 will process the S and U frames shown in table 1 and will handle the A and C fields for all I and UI frames.

Table 1 : Frame Types Symbols Definitions.

Name	Definition
I	Information frame
UI	Unnumbered Information
RR	Receiver Ready
DISC	Disconnect
RNR	Receiver Not Ready
UA	Unnumbered Acknoledge
REJ	Reject
FRMR	Frame Reject
SABM	Set Asynchronous Balance Mode
DM	Disconnect Mode
XID	Exchange Identification
TEST	Link Test frame

OPERATIONAL DESCRIPTION (continued)

Table 2 : Command/Response Repertoire - Module 8 Operation.

Format	Command	Resp	Encoding							
			1	2	3	4	5	6	7	8
Information Transfer	I		0	←	N(S)	→	P	←	N(R)	→
Supervisory	RR	RR	1	0	0	0	P/F	←	N(R)	→
	RNR	RNR	1	0	1	0	P/F	←	N(R)	→
	REJ	REJ	1	0	0	1	P/F	←	N(R)	→
Unnumbered	SABM		1	1	1	1	PF	1	0	0
		DM	1	1	1	1	F	0	0	0
	XID (1)	XID (1)	1	1	1	1	P/F	1	0	1
	UI (1)	UI (1)	1	1	0	0	P/F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
	TEST (2)	TEST (2)	1	1	0	0	P/F	1	1	1

Table 3 : Command/Response Repertoire - Modulo 128 Operation.

Format	Command	Resp	Encoding									
			1	2	3	4	5	6	7	8	9	10-1
Information Trasfer	I		0	N(S)							P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SABME		1	1	1	1	P/F	1	1	0		
		DM	1	1	1	1	F	0	0	0		
	XID (1)	XID (1)	1	1	1	1	P/F	1	0	1		
	UI (1)	UI (1)	1	1	0	0	P/F	0	0	0		
	DISC		1	1	0	0	P	0	1	0		
		UA	1	1	0	0	F	1	1	0		
		FRMR	1	1	1	0	F	0	0	1		
	TEST (2)	TEST (2)	1	1	0	0	P/F	1	1	1		

Notes :
1. XID and UI frames can be individually enabled for compatibility with X.32 and LAPD respectively.
2. TEST frames are enabled with XID frames.
3. N(S) = Transmitter Send sequence number.
4. N(R) = Transmitter Receive sequence number.
5. P/F = Poll bit when issued as a command, Final bit when issued as a response.

Protocol. The MK5025 contains a full implementation of the 1984 CCITT X.25 data link layer. It allows both basic and extended control fields, variable window sizes, and user-defined counter and timer values. Extended addressing and UI frames are optionally available for use in ISDN LAPD applications. XID and TEST frames are available for use in X.32. The interface between the MK5025 and the host (layer 3) conforms to both the ISO data link services standard and the ISDN LAPD data link services standard.

PROGRAMMING SPECIFICATIONS

This section defines the Control and Status Registers and the memory data structures required to program the MK5025.

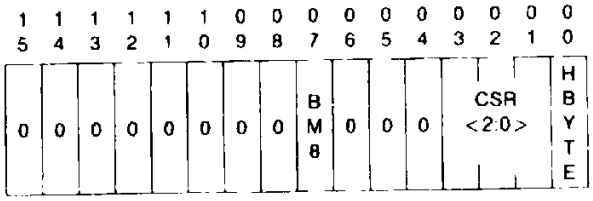
Control and Status Registers.

There are six Control and Status Registers (CSR's) resident within MK5025. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP). Thus the MK5025 needs only two address locations in the system memory or I/O map.

Accessing the Control and Status Registers. The CSR's are read (or written) in a two-step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

ADR	PORT
HIGH	Register Address Port (RAP)
LOW	Register Data Port (RDP)

Register Address Port (RAP)



Bit <15 : 08>. They are reserved and must be written as zeroes.

Bit 07, BM8. When set, places chip into 8-bit mode. CSR's, Init Block and data transfers are all 8-bit transfers, this provides compatibility with 8-bit microprocessors. When clear, all transfers are 16-bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is Read/Write and cleared on Bus Reset.

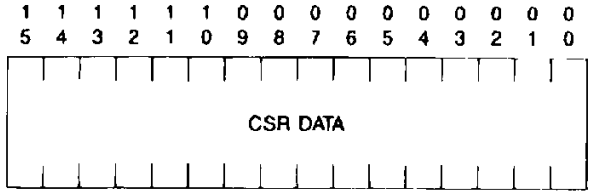
Bit <06 : 04>. They are reserved and must be written as zeroes.

Bit <03 : 01>, CSR <2 : 0>. CSR address select bits is Read/Write. Selects the CSR to be accessed through the RDP RAP is cleared by Bus Reset.

CSR<2 : 0>	CSR Selected
0	CSR0
1	CSR1
2	CSR2
3	CSR3
4	CSR4
5	CSR5

Bit 00, HBYTE. Determines which byte is addressed for 8-bit operation. If set, the high byte of the register referred to by CSR <2 : 0> is addressed, otherwise the low byte is addressed. This bit is only meaningful for 8-bit operation and must be written as zero if BM8 = 0. HBYTE is Read/Write and cleared on Bus Reset.

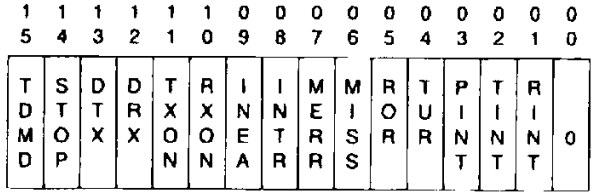
Register Data Port (RDP)



Bit <15 : 00>, CSR DATA. Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

Control and Status Register 0 (CSR0)

RAP <3 : 1> = 0



PROGRAMMING SPECIFICATIONS (continued)

Bit 15, TDMD. TRANSMIT DEMAND, when set, causes MK5025 to access the Transmit Descriptor Ring without waiting for the transmit polltime interval to elapse. TDMD need not be set to transmit a frame, it merely hastens MK5025's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and cleared by the MK5025 after it is used. It may read as a "1" for a short time after it is written because the MK5025 may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.

Bit 14, STOP. STOP, when set, indicates that MK5025 is operating in the STOPPED phase of operation. All external activity is disabled and internal logic is reset. MK5025 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.

Bit 13, DTX. Transmitter Ring Disable prevents the MK5025 from further access to the Transmitter Descriptor Ring. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. DTX is READ/WRITE. TXON acknowledges changes to DTX, see below.

Bit 12, DRX. Receiver Ring Disable prevents the MK5025 from further access to the Receiver Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. If DRX is set while a data link is established the MK5025 will go into the local busy condition and will send a RNR response frame to the remote station. Upon clearing DRX the MK5025 will send a RR response frame. DRX is READ/WRITE. RXON acknowledges changes to DRX, see below.

Bit 11, TXON. TRANSMITTER ON indicates that the transmitter ring access is enabled. TXON is set as the START primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by issuing a STOP primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY ; writing this bit has no effect.

Bit 10, RXON. RECEIVER ON indicates that the receiver ring access is enabled. RXON is set as the START primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a STOP primitive in CSR1, or by a Bus RESET. If RXON is clear, the host may modify the Receive Descriptor Ring entries regardless of the state of the OWNA bits. RXON is READ ONLY ; writing this bit has no effect.

Bit 09, INEA. INTERRUPT ENABLE allows the INTR I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 the INTR I/O pin will be low if CSR0 <08> INTR is set. If INEA = 0 the INTR I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE, set by writing a "1" into this bit and is cleared by writing a "0" into this bit or by Bus RESET or by issuing a STOP primitive.

Bit 08, INTR. INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occured ; MISS, MERR, RINT, TINT, PINT, TUR or ROR. If INEA = 1 and INTR = 1 the INTR I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a STOP primitive.

PROGRAMMING SPECIFICATIONS (continued)

Bit 07, MERR. MEMORY ERROR sets when MK5025 is the Bus Master and has not received READY within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.

Bit 06, MISS. MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer, indicating loss of a frame. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by the MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 05, ROR. RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. The frame being received is lost but is recoverable according to the Link Level protocol. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 04, TUR. TRANSMITTER UNDERRUN indicates that the MK5025 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by the MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 03, PINT. PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive or to indicate a User Primitive Error Condition. See CSR1<15> UERR. When PINT is set, an interrupt is generated if INEA = 1. PINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

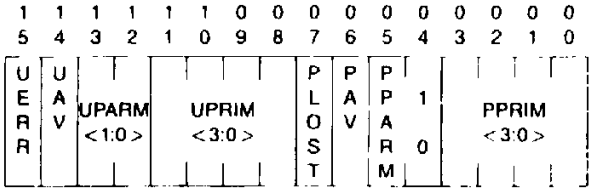
Bit 02, TINT. TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit descriptor Ring. This occurs when a transmitted frame has been acknowledged by the remote station. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 01, RINT. RECEIVER INTERRUPT is set after MK5025 updates an entry in the Receive Descriptor Ring. This occurs when the MK5025 has received a correct frame from the remote station. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.

Bit 00. Reserved. This bit is READ ONLY.

Control and Status Register 1 (CSR1)

RAP <3 : 1> = 1



PROGRAMMING SPECIFICATIONS (Continued)

Bit 15, UERR. USER PRIMITIVE ERROR is set by the MK5025 when a primitive issued by the user is in conflict with the current status of the link. UERR is READ/CLEAR ONLY and is set by MK5025 and cleared bywritig a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.

Bit 14, UAV. USER PRIMITIVE AVAILABLE is set by the user after a primitive has been placed in UPRIM. It is cleared by the MK5025 after the primitive has been processed. This bit is also cleared by a Bus RESET.

Bit < 13 : 12>, UPARM. UPARM is written by the host in conjunction with the user primitives in UPRIM. This user parameter field provides for the information to the MK5025 concerning the corresponding user primitive. For connect and reset primitives this field determines what the MK5025 will do with frames in the transmit descriptor ring that have been previously sent but not aknowledged. If UPARM = 0, these frames will be resent when the new link is established. If UPARM = 1, these frames are discarded by the MK5025 and their OWNA bits are cleared, releasing ownership back to the host. For all other primitives this field should be written with zeroes, unless otherwise indicated.

Bit < 11 : 08>, UPRIM. USER PRIMITIVE is written by the user to control the MK5025 link procedures. The following values are valid:

0 Stop - Instructs MK5025 to go into STPPED Mode. All link activity is terminated and the STOP bit is set. Transmitter outputs all "1"s. All DMA activity ceases.

1 Start-Instructs MK5025 to exit STOPPED Mode and enter the Disconnected Phase. Descriptor Rings are reset. Transmitter begins outputting flags. Issuring a Start primitive with UPARM = 1 will put the MK5025 directly into the Information Transfer phase, just as if it had received UA in response to SABM. Valid only in STOPPED Mode, or Transparent Mode.

2 Init Request - Instructs MK5025 to read the initialization block. Valid only in STOPPED Mode and Disconnected Phase. This should be performed prior to the start primitive after a bus reset or powerup.

3 Trans - Instructs MK5025 to enter the Transparent phase of operation. Data frames are transmitted and received out of the descriptor rings but no protocol processing is done. Address and Control Fields are not prepended to the frames, but FCS processing works normally. If the PROM bit is set in CSR2 then no address filtering is performed on received frames. Transparent Mode may be exited only with a stop primitive or by bus reset.

4 Status Request - Instructs MK5025 to write the current link status into the STATUS buffer. Valid only if INIT primitive has previously been issued.

5 Self - Test Request - Instructs MK5025 to perform a self test. Valid only in STOPPED Mode. See page 31/40 for self-test procedure.

6 Connect request - Instructs MK5025 to attempt to establish a logical link with the remote site. Valid only in Disconnected Phase.

7 Connect Response - Indicates willingness to establish a logical link with the remote site. Valid only in Disconnected Phase after receiving a Connect indication primitive.

PROGRAMMING SPECIFICATIONS (continued)

8 Reset Request - If a logical link has been established, instructs MK5025 to attempt to reset the current logical link with the remote site (sends SABM/E). In Transparent Mode or Disconnected Phase, instructs MK5025 to start the T1 timer.

9 Reset Response - If a logical link has been established, indicates willingness to reset current logical link with remote site (valid only after receiving a Reset Indication primitive.) In Transparent Mode or Disconnected Phase, instructs MK5025 to stop the T1 timer.

10 XID Request - Requests MK5025 to send an XID command to the remote site. Data in the XID/TEST Transmit buffer is used for the Data Field. Invalid in STOPPED Mode.

11 XID Response - Requests MK5025 to send an XID response to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Valid only after receiving an XID Indication primitive.

12 TEST Request - Requests MK5025 to send a TEST command to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Invalid in STOPPED Mode.

13 TEST Response - Requests MK5025 to send a TEST response to the remote site. Data in the XID/TEST transmit buffer is used for the data field. Valid only after receiving a TEST indication primitive.

14 Disconnect Request - Requests MK5025 to disconnect the current logical link. Invalid in STOPPED Mode. A DM response with the F bit clear will be sent if the link is currently disconnected.

Bit 07, PLOST. PROVIDER PRIMITIVE LOST is set by MK5025 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared and by a Bus RESET. Writing to this bit has no effect.

Bit 06, PAV. PROVIDER PRIMITIVE AVAILABLE is set by the MK5025 when a new provider primitive has been placed in PPRIM. PPRIM is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET.

Bit <05 : 04>, PPARM. PROVIDER PARAMETER provides additional information about the reason for the receipt of a disconnect, reset or error indication primitive. This field is undefined for other provider primitives. Parameters are as follows :

PPARM	Disconnect Indication	Disconnect Confirmation	Reset Indication	Error Indication
0	Remotely Initiated	UA or DM F = 1 Recvd	Remotely Initiated	Unsolicited DM/F = 0 Recvd
1	SABM Timeout	DISC Timeout		Timer Recovery Timeout
2	FRMR Sent then DISC or DM Received T3 Timeout		FRMR Sent then SABM/E Recvd	FRMR Received
3		T3 Timeout		Unsolicited UA or F bit Received

PROGRAMMING SPECIFICATIONS (continued)

Bit <03 : 00>, PPRIM. PROVIDER PRIMITIVE is written by MK5025 to inform the user of link control conditions. Valid Provider Primitives are as follows :

2 Init Confirmation - Indicates that the initialization has completed.

4 Error Indication - Indicates an error condition has occurred during the Information Transfer phase of operation that requires instruction by the Host for recovery. See PPARM for specific error conditions. Either a Reset Request or Disconnect Request primitive should be issued in UPRIM after receiving an Error Indication primitive.

5 Remote Busy Indication - Indicates change in Remote Busy status. PPARM = 0 indicates receipt of RNR - Remote Busy. PPARM = 1 indicates Remote no longer busy - RR received. This primitive is only issued if RBSY = 1. RBSY (bit 15 of IADR + 16) is set by the Host in the Init block.

6 Connect Indication - Indicates an attempt by the remote site to establish a logical link. Appropriate user responses are Connect Response or Disconnect Request.

7 Connect Confirmation - Indicates the success of a previous Connect Request by the user. A logical link is now established.

8 Reset Indication - If a logical link has been established, indicates an attempt by the remote site to reset the current logical link. Appropriate user responses are Reset Response or Disconnect Request. In Transparent Mode, or Disconnected Phase, indicates expiry of timer T1.

9 Reset Confirmation - Indicates the success of a previous Reset Request by the user. The current logical link has now been reset.

10 XID Indication - Indicates the receipt of an XID command. The Data Field of the XID command is located in the XID/TEST Receive Buffer.

11 XID Confirmation - Indicates the receipt of an XID response. The Data field of the XID response is located in the XID/TEST Receive Buffer.

12 TEST Indication - Indicates the receipt of a TEST command. The Data Field of the TEST command is located in the XID/TEST Receive buffer.

13 TEST Confirmation - Indicates the receipt of a TEST response. The Data field of the TEST response is located in the XID/TEST Receive Buffer.

14 Disconnect Indication - Indicates a request by the remote site to disconnect the current logical link or the refusal of a previous Connect or Reset Request. The chip is now in the Disconnected Phase.

15 Disconnect Confirmation - Indicates the completion of a previously requested link disconnection.

Control and Status Register 2 (CSR2)

RAP <3 : 1> = 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	FRMRD	T203E	X75E	PROM	UIE	XIDE	IADR<23:16>							

Bit <15 : 14>. Reserved, must be written as zeroes.

Bit 13, FRMRD. Setting this bit disables the sending of FRMR frames (used for LAPD applications) ; otherwise the MK5025 behaves as specified for X.25. This bit is READ/WRITE.

Bit 12, T203E. If this bit is set, the T3 timer is reconfigured to behave as specified for LAPD T203 timer ; otherwise it behaves as specified for X.25. This bit is READ/WRITE.

PROGRAMMING SPECIFICATIONS (continued)

Bit 11, X75E. X.75 mode is enabled if this bit is set to 1 ; otherwise X.25 mode is enabled. This bit is READ/WRITE.

Bit 10, PROM. Address filtering is disabled for transparent mode, if this bit is set. All uncorrupted incoming frames are placed in the Receive Descriptor Ring. This bit is READ/WRITE. Should be set only in Trans Mode.

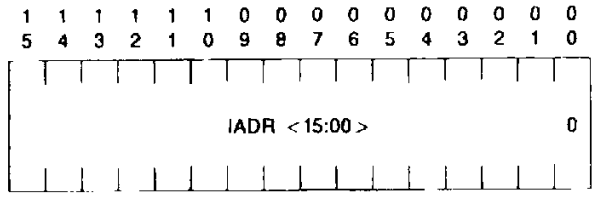
Bit 09, UIE. UI frames are recognized only if this bit is set. If UIE = 0 all received UI frames will not be recognized. This bit is READ/WRITE.

Bit 08, XIDE. XID frames are recognized only if this bit is set. If XIDE = 0 all received XID frames will not be recognized. This bit is READ/WRITE.

Bit <07 : 00>, IADR. The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

Control and Status Register 3 (CSR3)

RAP <3 : 1> = 3



BIT <15 : 00>, IADR. The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization Block must be on an even byte boundary.

Control and Status Register 4 (CRS4). CRS4 allows redefinition of the bus master interface.

RAP <3 : 1> = 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FWM <1:0>		BAEN	BUSR	BSWPC	BURST	1 : 0	BSWPD	ACON	BCON

Bit <15 : 10> Reserved, must be written as zeroes.

Bit <09 : 08>, FWM. These bits define the FIFO watermarks. FIFO watermarks prevent the MK5025 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive data, data will only be transferred to the data buffers after the FIFO has at least N 16-bit words or an end of frame has been reached. Conversely, for transmit data, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows :

FWM :0	N
11	1word
10*	9 words
01	17 words
00	25 words

* Suggested Setting

Bit 07, BAEN. This bit should be written as "0" for standard operation as described in the timing diagrams in figures 7 and 8 of this manual. If this bit is set, the upper 4 address bits (A <23 : 20>) will be available at the time HOLD is asserted, and are never tristated. This facilitates use in multiple bus systems to identify which bus is being requested.

Bit 06, BUSR. If this bit is set, pin 15 becomes input BUSREL. If this bit is clear pin 15 is either BM0 or BYTE depending on bit 00. For more information see the description for pin 15 earlier in this document. BUSR is READ/WRITE and cleared on Bus Reset.

Bit 05, BSWPC. This bit determines the byte ordering of all "non-data" DMA transfers. "Non-data" DMA transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows MK5025 to operate with

memory organizations that have bits <07 : 00> ar even addresses with bits <15 : 08> at odd addresses or vice versa.
With BSWPC = 1 :
Address
XX0 | 0 ••• 7 |
XX1 | 8 ••• 15 |
This memory organization is used with the LSI 11 and the 8086 microprocessors.
With BYTE SWAP = 0 :
Address
XX0 | 8 ••• 15 |
XX1 | 0 ••• 7 |
This memory organization is used with the 68000 and Z8000 microprocessors. BSWP is Read/Write and cleared by BUS RESET.

Bit <04 : 03>, BURST. This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on Bus RESET.

BURST <1 : 0>	8 bit Mode	16 bit Mode
00	2 bytes	1 word
10*	16 bytes	8 words
01	unlimited	unlimited

* Suggested Setting

Bit 02, BSWPD. This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.

Bit 01, ACON. ALE CONTROL defines the assertive state of Pin 18 when MK5025 is a Bus Master. ACON is READ/WRITE and cleared by Bus RESET.

ACON	Pin 18	Asserted
0	ALE	High
1	AS	Low

Bit 00, BCON. BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN 16	PIN 15	PIN 17
0	BM 1	BM 0	HOLD
1	BUSAKO	BYTE	BUSRQ

Control and Status Register 5 (CSR5).CSR5 facilitates control and monitoring of modem controls.

RAP <3 : 1> = 5

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	RTSEN	DTRD	DSRD	DTR	DSR

Bit <15 : 05>. Reserved, must be written as zeroes.

Bit 4, RTSEN. RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set pin 26 (DTR) becomes RTS and pin 30 (DSR) becomes CTS. RTS is driven low whenever the MK5025 has data to transmit and kept low during transmission. RTS will be driven high after the closing flag of a frame transmitted if either no other frames are in the FIFO or if the minimum frame spacing is higher than 2 (see Mode Register). The MK5025 will not begin transmission and TD will remain HIGH if CTS is high. Bit RTSEN should not be set when operating in Internal Loopback mode.

Bit 3, DTRD. DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR pin. If DTRD = 0, the DTR pin becomes an input pin and the DTR bit reflects the current value of the pin ; if DTRD = 1, the DTR pin is an output pin controlled by the DTR bit below.

Bit 2, DSRD. DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR pin. If DSRD = 0, the DSR pin becomes an input pin and the DSR bit reflects the current value of the pin ; if DSRD = 1, the DSR pin is an output pin controlled by the DSR bit below.

Bit 1, DTR. DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR pin.

Bit 0, DSR. DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR pin. If DSRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DSR pin.

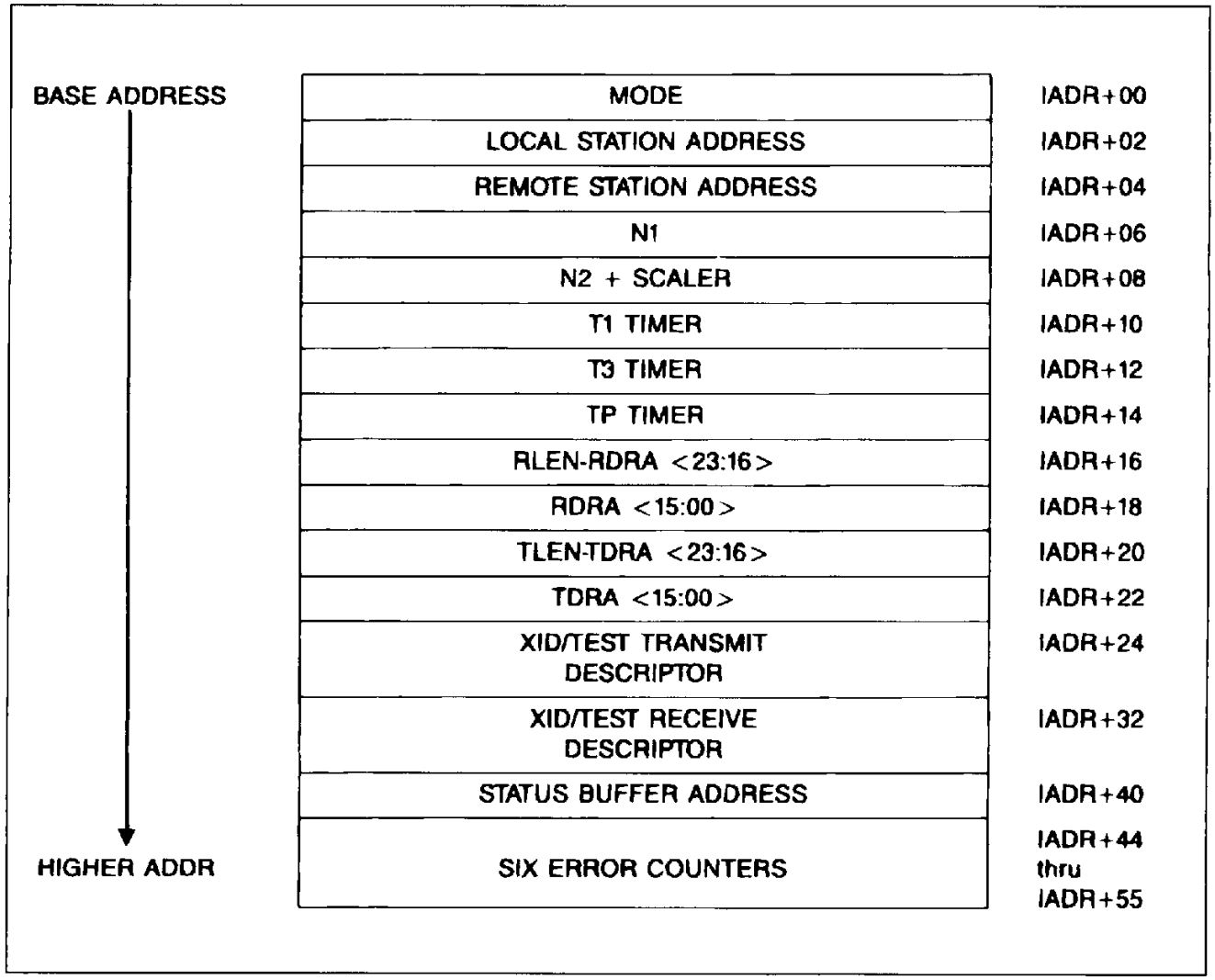
Initialization Block

MK5025 initialization includes the reading of the initialization block in memory to obtain the operating parameters.

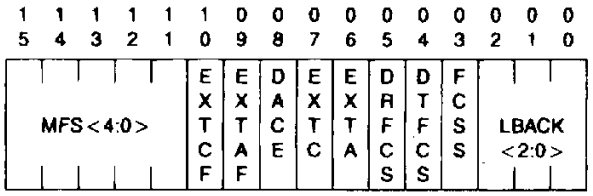
The Initialization Block is read by MK5025 when receiving an INIT primitive. During normal initialization the INIT should be sent prior to sending a START primitive. The user may re-issue the INIT primitive after a START, but received frames may be lost if care is not taken. An INIT cannot be issued while a link is connected ; MK5025 will reject such an attempt.

Except for the Error Counters and XID/TEST Descriptor OWNA bits, the MK5025 will not write into the Initialization Block.

Figure 6 : Initialization Block.



Mode Register. The Mode Register allows alteration of the MK5025's operating parameters.



Bit <15 : 11>, MFS <4 :0>. Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK5025. This only affects frames transmitted by the MK5025 and does not restrict the spacing of frames received by the MK5025. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after $\overline{CTS}$ is driven low (minus one for the trailing flag). See following table for encoding of this field.

Number of Flags	MFS <4:0>
1	1
2	0
4	2
6	4
8	9
10	18
12	5
14	11
16	22
18	12
20	25
22	19
24	7
26	15
28	31
30	30
32	28
34	24
36	17
38	3
40	6
42	13
44	27
46	23
48	14
50	29
52	26
54	21
56	10
58	20
60	8
62	16

Bit 10, EXTCF. Extended Control Force is useful only in transparent mode operation. If set along with EXTC, the receiver will assume the control field to be two octets long regardless of the first two bits of the control field. See EXTC below.

Bit 09, EXTAF. Extended Address Force is useful only in transparent mode operation. If set along with EXTA, the receiver will assume the address field to be two octets long regardless of the first bit of the address. See EXTA below.

Bit 08, DACE. Address and control field extraction are disabled when DACE is set. Address and control fields are treated as normal data. DACE must be written as "0" for normal operation in non-transparent mode.

Bit 07, EXTC. Extended Control Field is enabled when EXTC = 1. The control fields of all S and I frames become two octets in length, instead of one. The numbering for I frames becomes modulo 128, instead of modulo 8. The control field of U frames remains one octet in length.

Bit 06, EXTA. Extended address is enabled when EXTA = 1. The length of address fields is determined by the first bit of the address. If the first bit is set then the address field is 1 octet long otherwise it is 2 octets.

Bit 05, DRFCS. Disable Receiver FCS. When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct.

Bit 04, DTFCS. Disable Transmitter FCS. When DTFCS = 0, the transmitter will generate and append the FCS to each frame. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames.

Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.

Bit 03, FCSS. FCS Select. When FCSS = 1, a 16 bit FCS is selected otherwise a 32-bit FCS is used.

Bit <02 : 00>, LBACK. Loopback Control puts the MK5025 into one of several loopback configurations.

LBACK0. Normal operation. No loopback.

LBACK4. Simple loopback. Receive data and clock are driven internally by transmit data and clock.

LBACK5. Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.

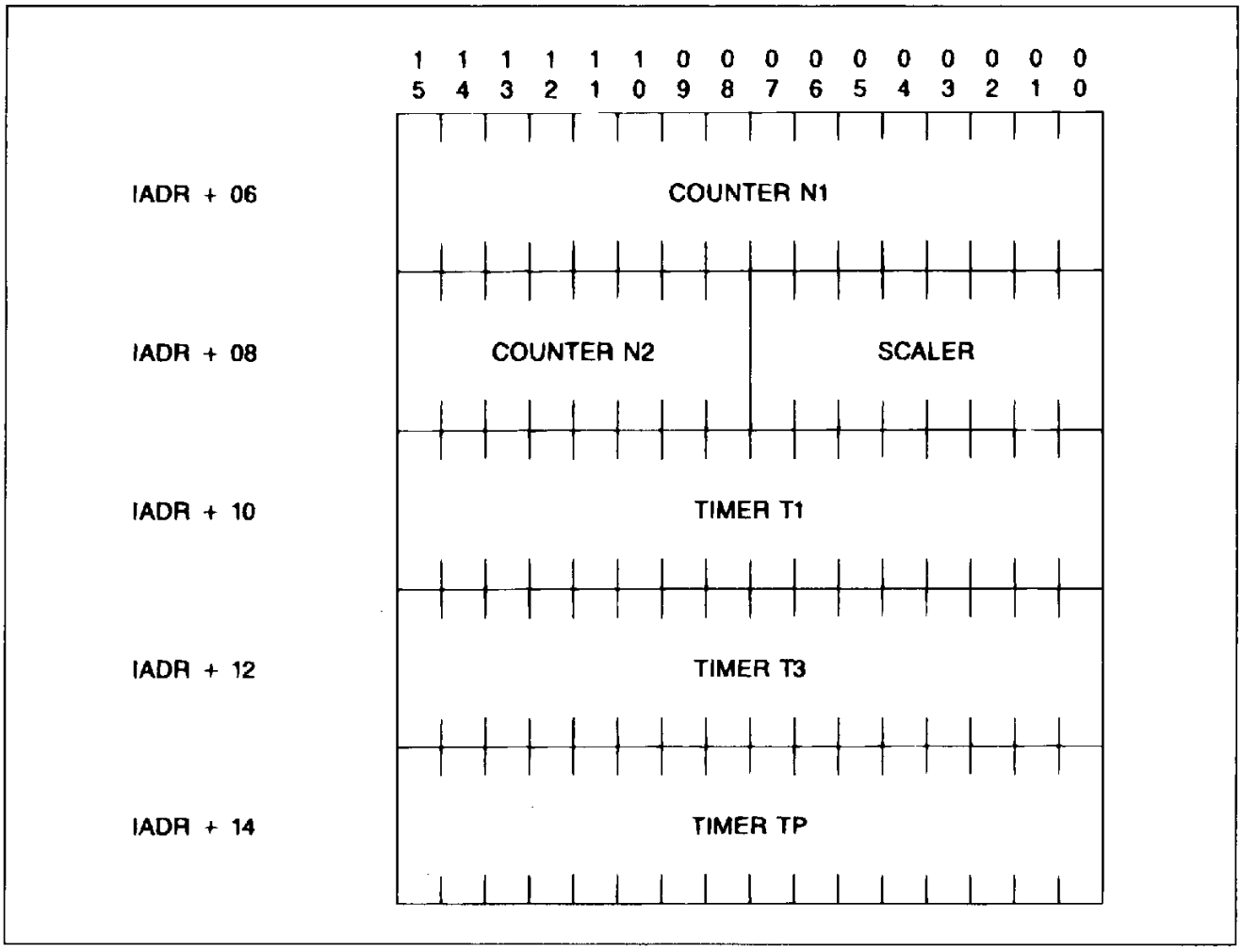
LBACK6. Silent loopback. Same as simple loopback with TD pin forced to all ones.

LBACK7. Silent Clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. TD pin is forced to all ones.

Station Addresses. The Local and Remote station addresses may be either one or two octets according to the EXTA control bit described in the MODE register. If extended address mode is selected bit 0 should be set to a zero for adherence to ADCCP/HDLC. If extended address mode is not selected, the command and response frame addresses should be located in the lower order byte of their respective fields. When operating in Loopback mode, Station addresses must be the same.

Timers. There are 5 independent counter-timers. The lower 8 bits of IADR + 08 are used as a scaler for T1, T3, and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is a 16 bit counter and is used to count the number of bytes in an I-frame. N2 is an 8 bit counter.

The Host will write the period of N1, N2, T1, T3, and TP into the Initialization Block.



N1. MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame received that exceeds this count will be discarded.

N2. MAXIMUM RETRANSMISSION COUNT. This field must contain the two's complement of one less than the maximum number of retransmissions that will be made following the expiration of T1.

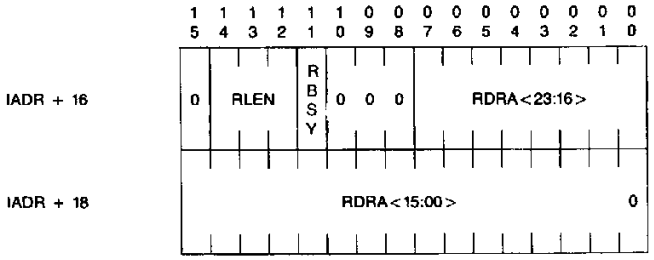
SCALER. TIMER PRESCALER. Timers T1, T3, and TP are scaled by this number. The prescaler incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. Note : a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8224 clock pulses).

T1. RETRANSMISSION TIMER. Link control frames will be retransmitted upon the expiration of the T1 timer if the appropriate response is not received. These frames will be retransmitted up to N2 (see above) times, at which time the link will be disconnected or reset by MK5025 according to the X.25 protocol. This field must contain the two's complement of the period of timer T1. The scaled (see SCALER) value of T1 should be made large enough to allow the remote station to receive the control frame and send its response.

T3. LINK IDLE TIMER. The link idle timer determines the amount of link idle time necessary to consider the link disconnected. This field must contain the two's complement of the period of timer T3. T3 is disabled (but not T203) if CSR5 RTSEN = 1 or if the MK5025 is in transparent mode.

TP. TRANSMIT POLLING TIMER. This scaled timer determines the lenght of time between transmit frame polls. Unless TDMD (see CSR0) is set or a frame is received on the link, no attempt to transmit a frame in the transmit descriptor ring is made until TP expires. At TP expiration all transmit frames in the transmit descriptor ring will be sent. This field must contain the two's complement of the period of timer TP.

Receive Descriptor Ring Pointer



Bit 15. Reserved, must be written as a zero.

Bit <14 : 12>, RLEN. RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.

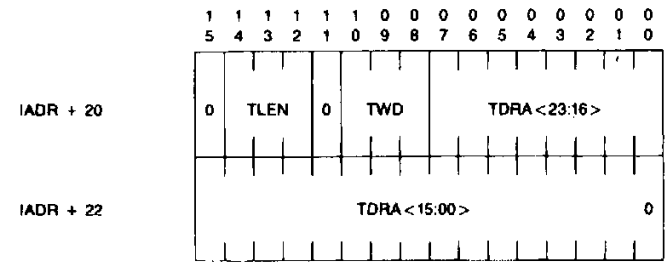
RLEN	Number of Entries
0	NA
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Bit 11 RBSY Setting this bit enables the generation of the Remote Busy Indication primitive (PPRIM = 5) whenever there is a change in the Remote Busy status.

Bit <10 : 08>. Reserved, must be written as zeroes.

Bit <07 : 00>/ <15 : 00>, RDRA. RECEIVE DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Receive Descriptor Ring. The Receive Ring must be aligned on a word boundary.

Transmit Descriptor Ring Pointer



Bit 15. Reserved, must be written as a zero.

Bit <14 : 12>, TLEN. TRANSIT RING LENGTH is the number of entires in the Transmit Ring expressed as a power of two.

Bit 11. Reserved, must be written as a zero.

Bit <10 : 08>, TWD. TRANSMIT WINDOW is the window size of the Transmitter as shown in the following table. TWD is the maximum number of I frames which may be transmitted without an acknowledgement. TWD is not allowed to be greater than 127.

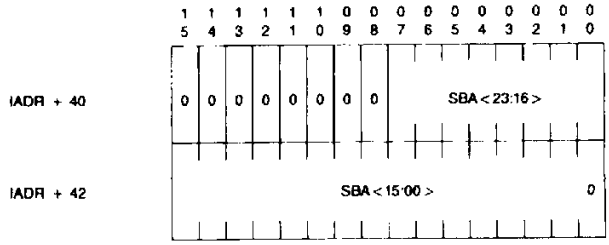
TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

TWD	Window Size	
	EXTC = 0	EXTC = 1
0	NA	1
1	1	3
2	2	7
3	3	15
4	4	31
5	5	63
6	6	127
7	7	127

Bit <07 : 00>/ <15 : 00>, TDRA. TRANSMIT DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Transmit Descriptor Ring. The Transmit Ring must be aligned on a word boundary.

XID/TEST Descriptors. The XID/TEST Descriptors contain pointers to the buffers used to receive and transmit XID and TEST frames, as well as the buffer lengths. The exact format of these descriptors can be seen below under Receive and Transmit Message Descriptor Entry descriptions. They are used the same as other descriptors except that no data chaining is allowed.

Status Buffer Address



Bit <15 : 08>. Reserved, must be written as zeroes.

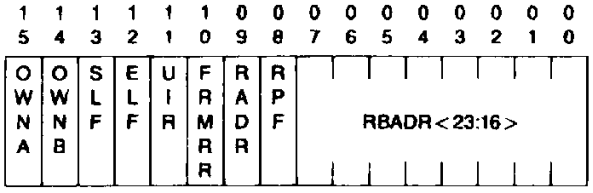
Bit <07 : 00>/ <15 : 00>, SBA. STATUS BUFFER ADDRESS points to a 7 word buffer into which link status information is placed upon the issuance of the STAT primitive by the HOST. The contents of the Status Buffer are described later in this document. The Status Buffer must begin on a word boundary.

Error Counters. Six locations in the initialization buffer are reserved for use as error counters which the MK5025 will increment. These are intended for use of the Host CPU for statistical analysis. The MK5025 will only increment the counters ; it is up to the user to clear and preset these counters. The error counters are :

MEMORY ADDRESS	ERROR COUNTER
IADR + 44	Bad frames received - Bad FCS - Non-Octet Aligned
IADR + 46	Number of FRMR frames received
IADR + 48	Number of T1 timeouts
IADR + 50	Number of REJ frames received
IADR + 52	Number of REJ frames transmitted
IADR + 54	Frames shorter than minimum length received

Receive and Transmit Descriptor Rings. Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

Receive Message Descriptor 0 (RMD0)



Bit 15, OWNA. When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided the received frame had a good FCS, N(r), and N(s). The Host sets the OWNA bit after emptying the buffer. Once the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

Bit 14, OWNB. This bit determines whether the HOST or the SLAVE PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.

Bit 13, SLF. Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the chip.
Note : *A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI or FRMR frame.*

Bit 12, ELF. End of Long Frame indicates that this the last buffer used by MK5025 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK5025.

Bit 11, UIR. UI Frame Received indicates that a UI frame has been received and is stored in this buffer.

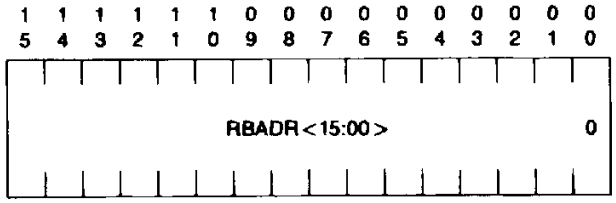
Bit 10, FRMRR. FRMR Received indicates that the I-field of a FRMR is stored in the buffer referenced by this Message Descriptor.

Bit 09, RADR. Valid only for frames received while in Transparent Mode with address filtering enabled. RADR indicates which of the 2 programmable addresses the frame matched. If set, the received address field matched the value in the Local Address field of the Initialization Block. Otherwise it matched the value in the Remote Address field.

Bit 08, RPF. Valid only for UI, XID and TEST frames. RPF equals the state of the P or F bit for the recvd frame.

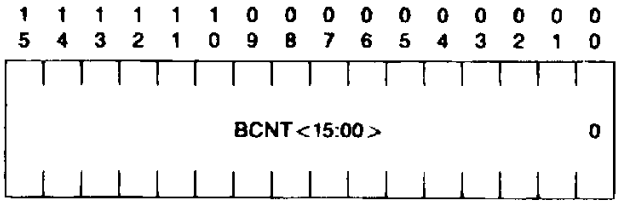
Bit <07 : 00>, RBADR. The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

Receive Message Descriptor 1 (RMD1)



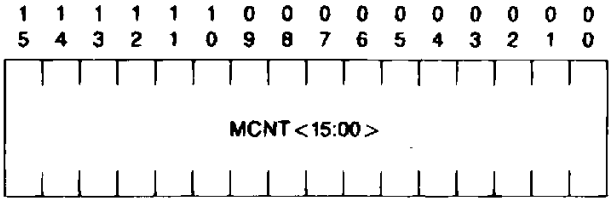
Bit <15 : 00>, RBADR. The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK5025. The receive buffers must be word aligned.

Receive Message Descriptor 2 (RMD2)



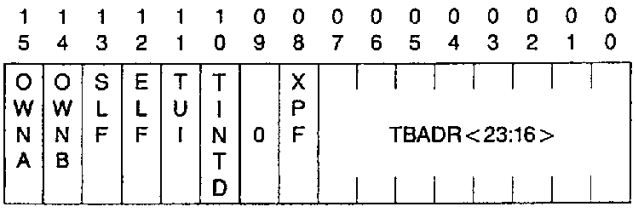
Bit <15 : 00>, BCNT. Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK5025. Buffer size must be even.

Receive Message Descriptor 3 (RMD3)



Bit <15 : 00>, MCNT. Message Byte Count is the length, in bytes, of the contents of the buffer expressed in two's complement. If ELF = 0, MCNT will equal the two's complement of BCNT since the MK5025 will fill a buffer before chaining to the next descriptor.

Transmit Message Descriptor 0 (TMD0)



Bit 15, OWNA. When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The host should set the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK5025 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the remote station. After the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

Bit 14, OWNB. This bit determines whether the HOST or the I/O ACCELERATION PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.

Bit 13, SLF. Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the Host.
Note : A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI frame or others.

Bit 12, ELF. End of Long Frame indicates that this the last buffer used by MK5025 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host.

Bit 11, TUI. Transmit a UI frame indicates that a UI frame is to be transmitted from the transmit buffer instead of a normal I frame. This bit must also be set for anything transmitted while the MK5025 is in Transparent Mode.

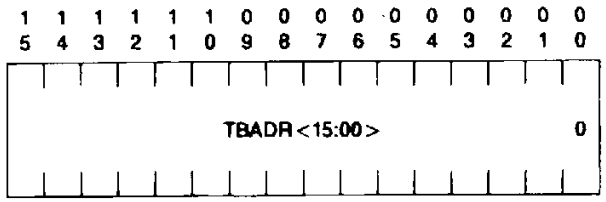
Bit 10, TINTD Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host. This allows users to limit the number of transmit interrupts.

Bit 09 Reserved, must be written as zeroes.

Bit 8, XPF. Transmit P/F bit instructs the MK5025 to send the corresponding frame with a particular value for the P/F bit. This bit should equal the desired value of the transmitted P/F bit. This bit is valid only for UI, XID and TEST frames and should be written with zero otherwise.

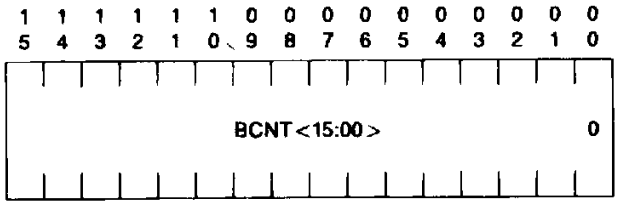
Bit <07 : 00>, TBADR. The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

Transmit Message Descriptor 1 (TMD1)



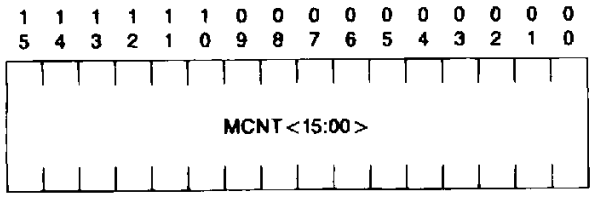
Bit <15 : 00>, TBADR. The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK5025. The least significant bit is zero since the descriptor must be word aligned.

Transmit Message Descriptor 2 (TMD2)



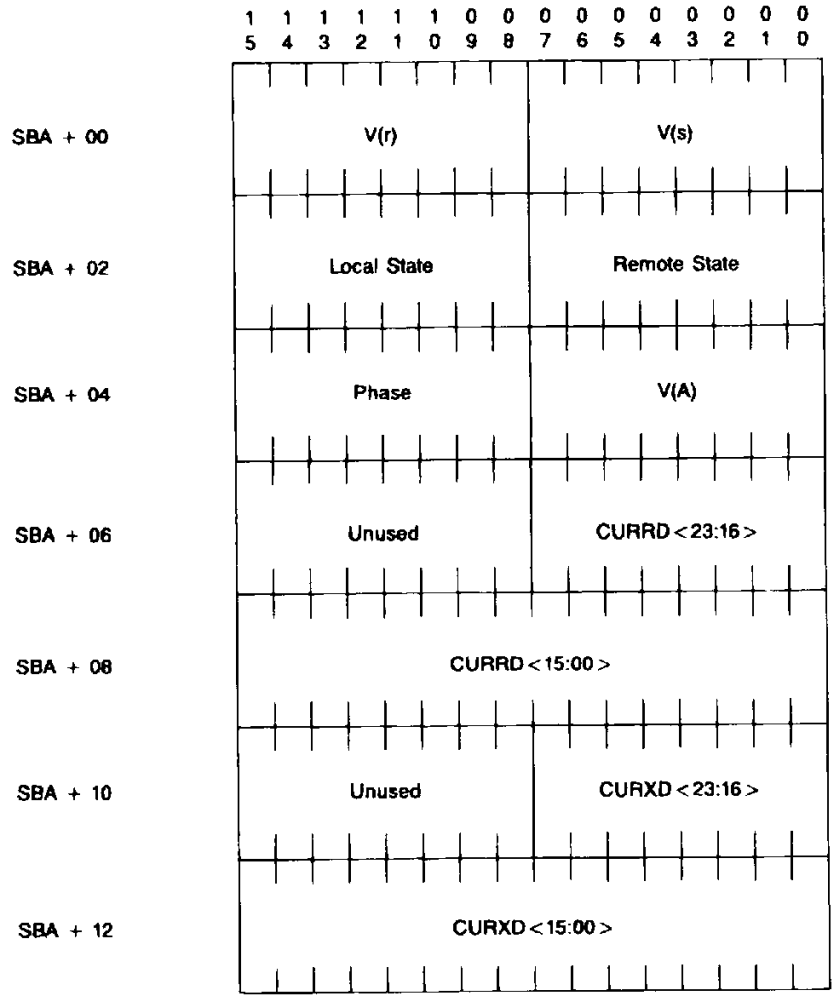
Bit <15 : 00>, BCNT. Buffer Byte Count is the usable length, in bytes, of the buffer pointed to by this descriptor in two's complement. This field is not used by the MK5025.

Transmit Message Descriptor 3 (TMD3)



Bit <15 : 00>, MCNT. Message byte count is the length, in bytes, of the contents of the buffer associated with this descriptor expressed as a two's complement.

Status Buffer



V(r). Current value of the Receive Count Variable. $0 \leq V(r) \leq 7$ for non-extended control ; $0 \leq V(r) \leq 127$ for extended control.

V(s). Current value of the Transmit Count Variable. $0 \Leftarrow V(s) \Leftarrow 7$ for non-extended control ; $0 \Leftarrow V(s) \Leftarrow 127$ for extended control.

Local State. Current state of local station.

Value	Description
0	Normal Data Transfer state
1	Local Busy state
2	REJ sent state
3	DISC sent state
4	Normal Disconnected state
5	SABM/E sent for link connection
6	FRMR sent state
7	SABM/E sent for link reset
8	Error Indication issued

Remote State. Current state of remote station.

Value	Description
0	Normal Data Transfer state
1	Remote Busy state

Phase. Current phase of operation.

Value	Description
– 1	Stopped Mode
0	Information Transfer phase
1	Disconnected phase
2	Resetting phase
3	Transparent Data Transfer phase

V(A). Current value of Transmit Acknowledge Count.. This field contains the value of the N(r) of the most recently received S or I frame. The modulo difference between V(A) and V(s) determines the number of outstanding I frames that have not been acknowledged by the remote station.

CURRD <23 : 00>. Current Receive Descriptor. This pointer indicates the position of the descriptor for the next receive buffer to be filled.

CURRXD <23 : 00>. Current Transmit Descriptor. This pointer indicates the position of the descriptor for the next transmit buffer to be transmitted.

Data Link Services

The MK5025 is consistent with the ISO Data Link Service Definition in providing services to the HOST. The following section is a brief description of this interface.

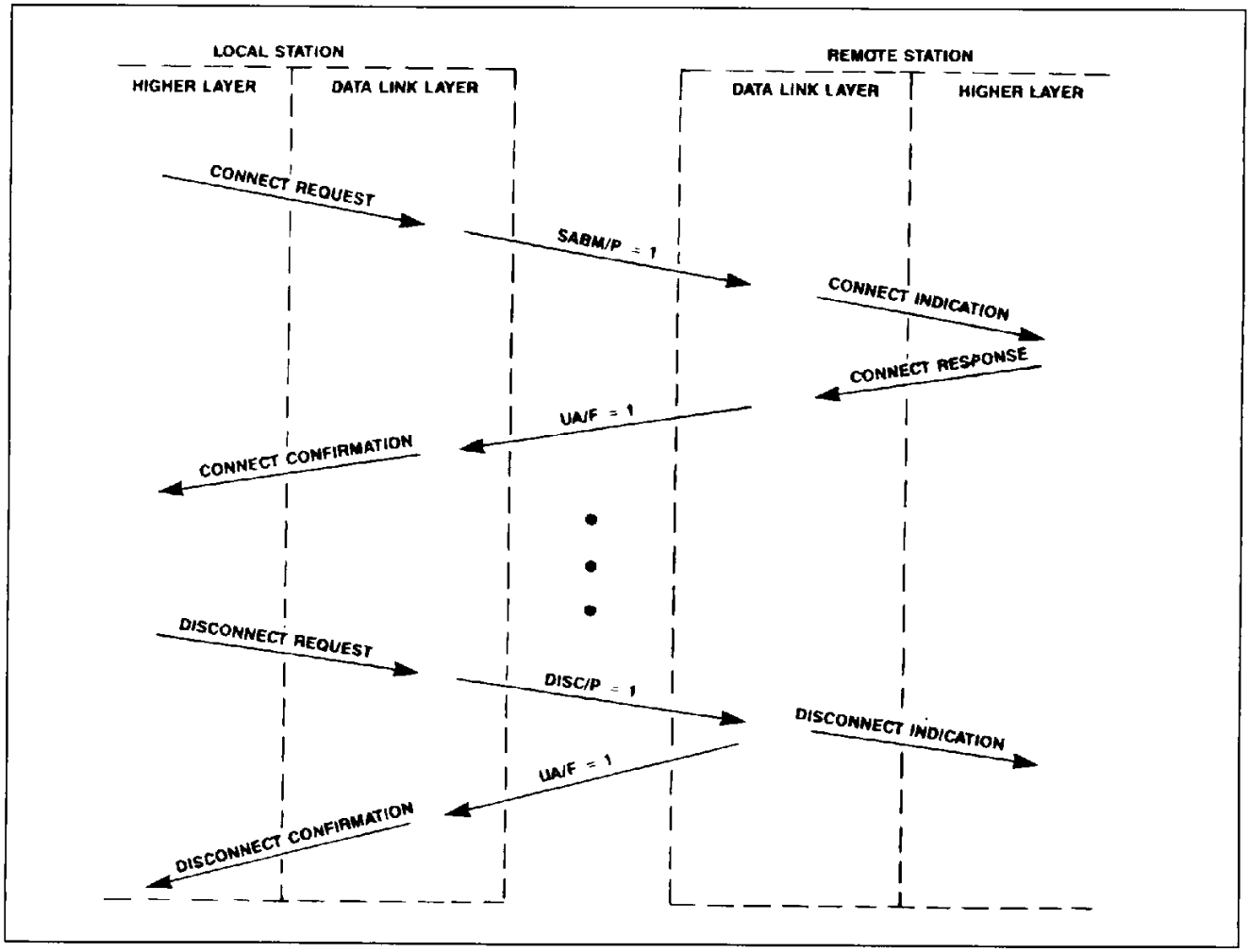
All link oriented services are provided through the exchange of Data Link Service Primitives. These primitives provide services to the HOST. Each primitive falls into one of the following categories :

1. Link Establishment (Connection)
2. Link Resetting
3. Link Disconnection
4. Data Transfer

A primitive is also one of the following types :

1. Request
2. Response
3. Indication
4. Confirmation

Figure 7 : Examples of Confirmed Data Link Services.



Requests and Responses are issued by the HOST and Indications and Confirmations are issued by the MK5025.

A Request will be issued by the HOST when a service is required. An Indication will be issued by the MK5025 when the remote system is attempting to change the data link status. A Response is issued by the HOST when receiving an indication for a confirmed service. A confirmation is issued by the MK5025 when the remote system has responded to a previously requested service.

In the MK5025, primitives are exchanged two ways : through the CSR1 and through the OWN bits in the descriptor rings. Connection, disconnection, and link reset primitives are exchanged through CSR1. Data transfer primitives are handled transparently by the OWN bit handshaking in the Descriptor Rings.

Nine additional primitives have been included in the MK5025 to handle services not mentioned in the ISO Data Link Service definition. These primitives include :

STOP - Disables the MK5025 from link operation. MK5025 transmits 1's.
INIT - Instructs the MK5025 to read the initialization block.
START - Enables the MK5025 for link operation. MK5025 starts sending flags.
TRANS - Enables the MK5025 for transparent operation. MK5025 starts sending flags.
STAT - Instructs the MK5025 to write chip status in the status buffer.
STEST - Instructs the MK5025 to perform an internal self test.
ERROR - Indicates the occurence of a link error requiring higher level action.
XID - Confirmed exchange of identification (optional).
TEST - Provides a full remote loopback test facility (optional).

For examples of the use of primitives, see the section on detailed programming procedures below.

Detailed Programming Procedures

Initialization. The following procedures should be followed to initialize the MK5025 :

1. Setup bus control information in CSR4.
2. Setup Initialization Block and Descriptor Rings and load the address of the initialization block in CSR's 2 and 3.
3. Issue the INIT primitive through CSR1 instructing the MK5025 to read the initialization block information.
4. Wait for INIT Confirmation primitive from the MK5025.
5. Issue the START Primitive through CSR1 to enable the MK5025 for link operation.
6. Enable interrupts in CSR0 if desired.

Active Link Setup. The following procedures should be followed to actively establish a link :

1. Issue the Connect Request primitive through CSR1. The MK5025 will attempt to establish a logical link.
2. Wait for a Connect Confirm primitive from the MK5025.
3. If a Connect Confirm primitive is received, a link has been established.
4. If a Disconnect Indication primitive is received, the MK5025 has been unable to establish a link. The reason will be in the PPARM field of CSR1.

Passive Link Setup. The following procedures should be followed to passively establish a link :

1. Issue a Disconnect Request primitive. A DM frame with F bit clear will be sent to the remote station requesting link setup. This step is optional.
2. Wait for a Connect Indication primitive from the MK5025.
3. If a Connect Indication primitive is received, issue a Connect Response primitive to indicate willingness to establish the link. The link is now established.
4. If no Connect Indication primitive is received, the remote site is not trying to actively setup a link.

Refusing Link Setup. The following procedure should be followed when refusing link establishment :

1. A Connect Indication will be received indicating a request by the remote station to establish a link.
2. Issue a Disconnect Request to refuse the link establishment request.

Sending Data. The following procedure should be followed to send a data frame :

1. Wait for OWNA bit of current transmit descriptor to be cleared, if not already.
2. Fill buffer associated with current transmit descriptor with data to be sent, or set descriptor buffer address to any already filled buffer.
3. Repeat steps 1 and 2 for next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.
5. Go on to next descriptor, these OWNA bits will be cleared when the data has been sucessfully sent and acknowledged. In Transparent Mode, OWNA bits are cleared immediately after frame transmission.

Receiving Data. The following procedure should be followed when receiving a data frame :

1. Make sure that the OWNA bit of the current receive descriptor is clear.
2. Read data out of buffer associated with current receive descriptor.
3. Set the OWNA bit of current descriptor.
4. If ELF bit of current descriptor is clear, go on to next descriptor and repeat above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

Link Disconnection. The following procedure should be followed to disconnect an established link :

1. Issue the Disconnect Request primitive to the MK5025. The MK5025 will disconnect the link.
2. A Disconnect Confirmation will be issued after successful disconnection.

Link Reset. The following procedure should be followed to reset an established link :

1. Issue a Reset Request primitive to the MK5025.
2. Wait for a Reset Confirm primitive from the MK5025.
3. If a Reset Confirm primitive is received, the link has been reset.
4. If a Disconnect Indication is received, the MK5025 was unable to reset and has disconnected. The reason for failure is in the PPARM field of CSR1. Link connection procedures must now be performed to re-establish the link.

Receiving Link Reset. The following procedure should be followed when receiving a request for link reset :

1. A Reset Indication will be received from the MK5025 indicating the remote station has requested a link resetting.
2. If able to reset, issue a reset response to indicate willingness to reset the link.
3. If unable to reset, issue a Disconnect Request to disconnect the link.

Receiving FRMR Frame. The following procedure should be followed when receiving a FRMR :

1. An Error Indication will be received from MK5025 indicating an error condition. PPARM will indicate a FRMR frame has been received. The I-field of the FRMR has been placed in the next Receive Descriptor.
2. If able to reset, issue a Reset Request to MK5025 and wait for either a Reset Indication or a Disconnect Indication as described above for Link Reset.
3. If unable to reset, issue a Disconnect Request to disconnect the current link. Link setup procedures should now be performed to re-establish a link.

Exchanging Identification. The following procedure should be followed to exchange identification with the remote :

1. XIDE in CSR3 must be set prior to any identification exchange.
2. Place identification information in the XID/TEST Transmit Buffer.
3. Issue an XID Request primitive.
4. If an XID Confirm primitive is received, the identication exchange has been performed and the remote response is located in the XID/TEST receive buffer.
5. If a Disconnect Indication is received, the identification exchange was unsuccessful.

Receiving an Identification Request. The following procedure should be performed when receiving a request for identification :

1. An XID Indication primitive will be received from the MK5025 to indicate the request for identification. The remote identification information will be located in the XID/TEST receive buffer.
2. To respond, place identification information in the XID/TEST send buffer and issue an XID Response primitive.
3. To refuse, issue a Disconnect Request primitive.

Note : *An XID Indication will only be issued if the XIDE bit in CSR3 has been set. Otherwise, all identification requests will automatically be refused and XID frames will not be recognized.*

Disabling the MK5025. The following procedure should be followed to disable the MK5025 :

1. Issue the STOP primitive. This will disable the MK5025 from receiving or transmitting. The TD pin will be held high while the MK5025 is in stopped mode. The STOP bit in CSR0 will be set and interrupts disabled. If a link is currently established, data may be lost.

Re-enabling the MK5025. The same procedure should be followed for re-enabling the MK5025 as was used to initialize upon power-up. If the Initialization Block and the hardware configuration have not changed then steps 1 and 2 may be omitted.

MK5025 Internal Self Test. The MK5025 contains an easy to use internal built-in self test designed to test, with a high fault coverage, all of the major blocks of the device except for the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute internal self test :

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK5025.
5. After the PAV bit is set, read CSR1. The success or failure of the test is indicated in the PPRIM and PPARM fields as follows :

PPARM	PPRIM	RESULT
0	0	Passed self test
1	1	Failed the reset test of the self test
1	2	Failed self test in the micro controller RAM
1	3	Failed self test in the ALU
1	4	Failed self test in the timers
1	5	Failed self test in the transmitter and/or receiver
1	6	Failed self test in the CSRs and/or bus master
Otherwise		failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHz), the MK5025 is unable to respond to the Self Test Request and will not complete it successfully.

If the self test passes, then it may be immediately re-executed by clearing the PAV bit in CSR1 and then proceding from step 3, otherwise re-execution should proceed from step 1.

MK5025 Software Identification. The MK502X family of devices provide a means of identifing the device type by using the following procedure.

After completing steps 1 and 2 of above listed procedure for Self Test, issue the Self Test Request primitive (UPRIM = 5) with UPARM = 3. The chip will then return a PPRIM of 5 (7 for the MK5027, 9 for the MK5029, etc.) to identify the device type.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	− 0.5 to V_{CC} + 0.5	V
T_A	Ambient Operating Temperature Under Bias	− 25 to + 100	°C
T_{stg}	Ambient Storage Temperature	− 65 to + 150	°C
P_D	Total Device Power Dissipation	0.5	W

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified)

Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IL}		− 0.5		+ 0.8	V
V_{IH}		+ 2.0		V_{CC}+0.5	V
V_{OL}	@ I_{OL} = 3.2mA			+ 0.5	V
V_{OH}	@ I_{OH} = − 0.4mA	+ 2.4			V
I_{IL}	@ V_{in} = 0.4 to V_{CC}			± 10	µA
I_{CC}	T_{SCT} = 100ns		50		mA

CAPACITANCE (Frequency = 1MHz)

Symbol	Conditions	Min.	Max.	Unit
C_{IN}			10	pF
C_{OUT}			10	pF
C_{IO}			20	pF

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified).

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
1	SYSCLK	T_{SCT}	SYSCLK period		100		2000
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$		0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	C_L = 50pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$	C_L = 50pF	5		

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified)

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ Period		140		
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ High Time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ Low Time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise Time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall Time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD Data Rise Time		0		8
19	RD	T_{RDF}	RD Data Fall Time		0		8
20	RD	T_{RDH}	RD Hold Time after Rising Edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup Time Prior to Rising Edge of $\overline{RCLK}$		30		
22	A/ADL	T_{DOFF}	Bus Master Driver Disable after Rising Edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master Driver Enable after Falling Edge of $\overline{HLDA}$	T_{SCT} = 100nS	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to Falling Edge of $\overline{HLDA}$ from Falling Edge of $\overline{HOLD}$ (bus master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ Pulse Width		30		
26	A/DAL	T_{CYCLE}	Read/write, Address/data Cycle Time	T_{SCT} = 100nS	600		
27	A	T_{XAS}	Address Setup Time to Falling Edge of ALE		100		
28	A	T_{XAH}	Address Hold Time after the Rising Edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address Setup Time to the Falling Edge of ALE		75		
30	DAL	T_{AH}	Address Hold Time after the Falling Edge of ALE		20		
31	DAL	T_{RDAS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus maaster read)		55		
32	DAL	T_{RDAH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0		
33	DAL	T_{DDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master write)		0		
34	DAL	T_{WDS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus master write)		250		
35	DAL	TWDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus mater write)		35		
36	DAL	TSRDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave read)	T_{SCT} = 100nS	0		35
37	DAL	TSWDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave write)		0		
38	DAL	TSWDS	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave write)		0		
39	ALE	TALEW	ALE width high		110		

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified).

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
40	$\overline{ALE}$	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	DAS width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD} = 300nS T_{SCT} = 100nS	120		200
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of $\overline{ALE}$ (Bus master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
51	$\overline{DALO}$	T_{WDIS}	Delay from rising edge of $\overline{DAS}$ to the rising edge of DALO (bus master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
54	ADR	T_{SAH}	$\overline{ADR}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle (600nS)	T_{SCT} = 100nS			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)	T_{SCT} = 100nS	0		35
60	READ	T_{SRH}	$\overline{READ}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
61	$\overline{READ}$	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (bus slave read)	T_{SCT} = 100nS		200	

Figure 8 : Output Load Diagram.

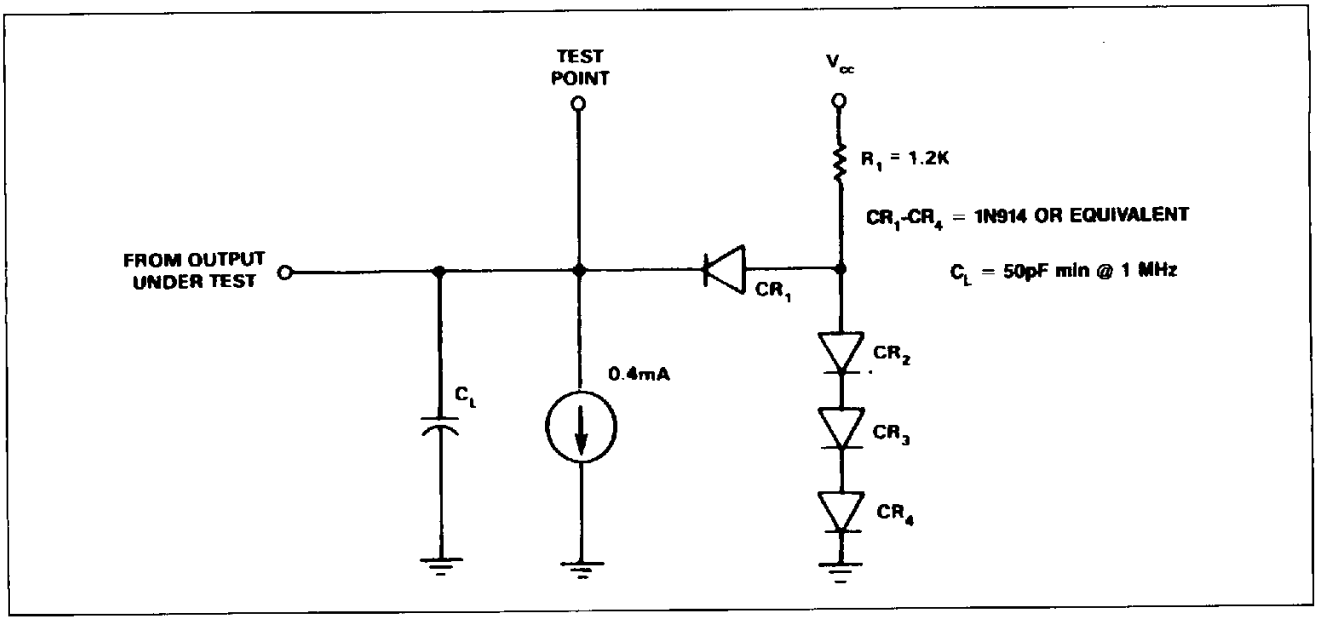
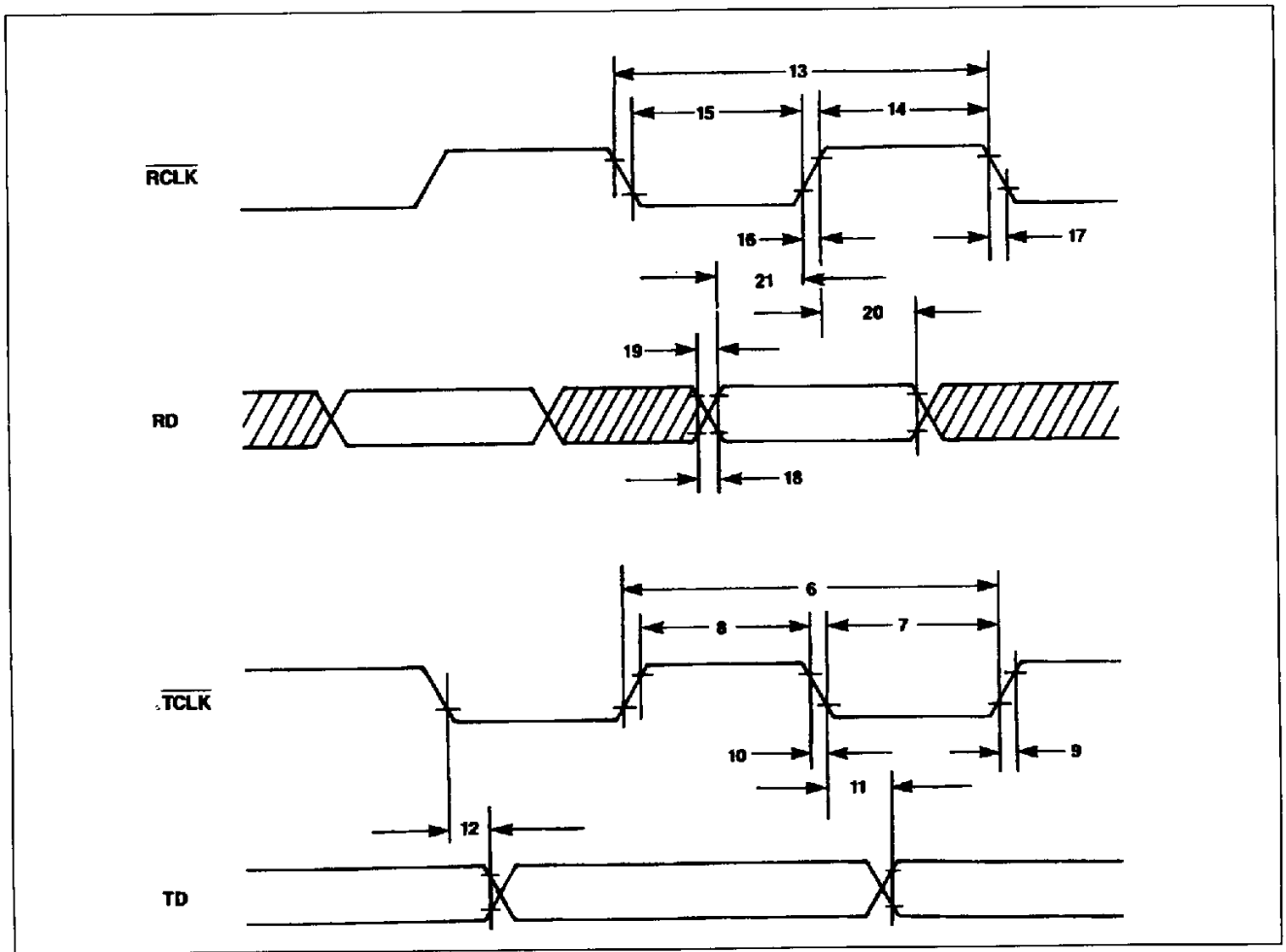


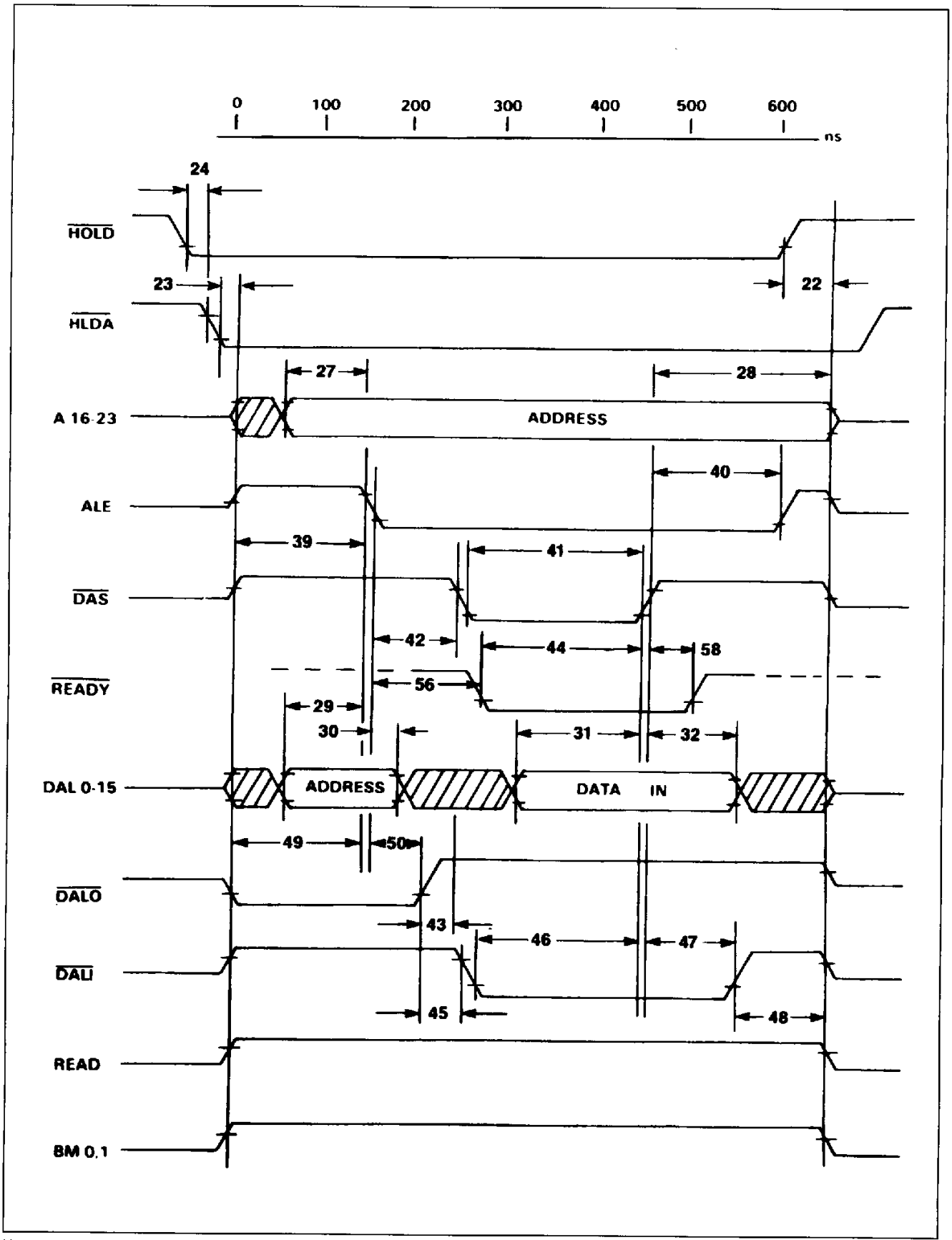
Figure 9 : Serial Link Timing Diagram.



Note : Timing Measurements are made at the following voltages, unless otherwise specified :

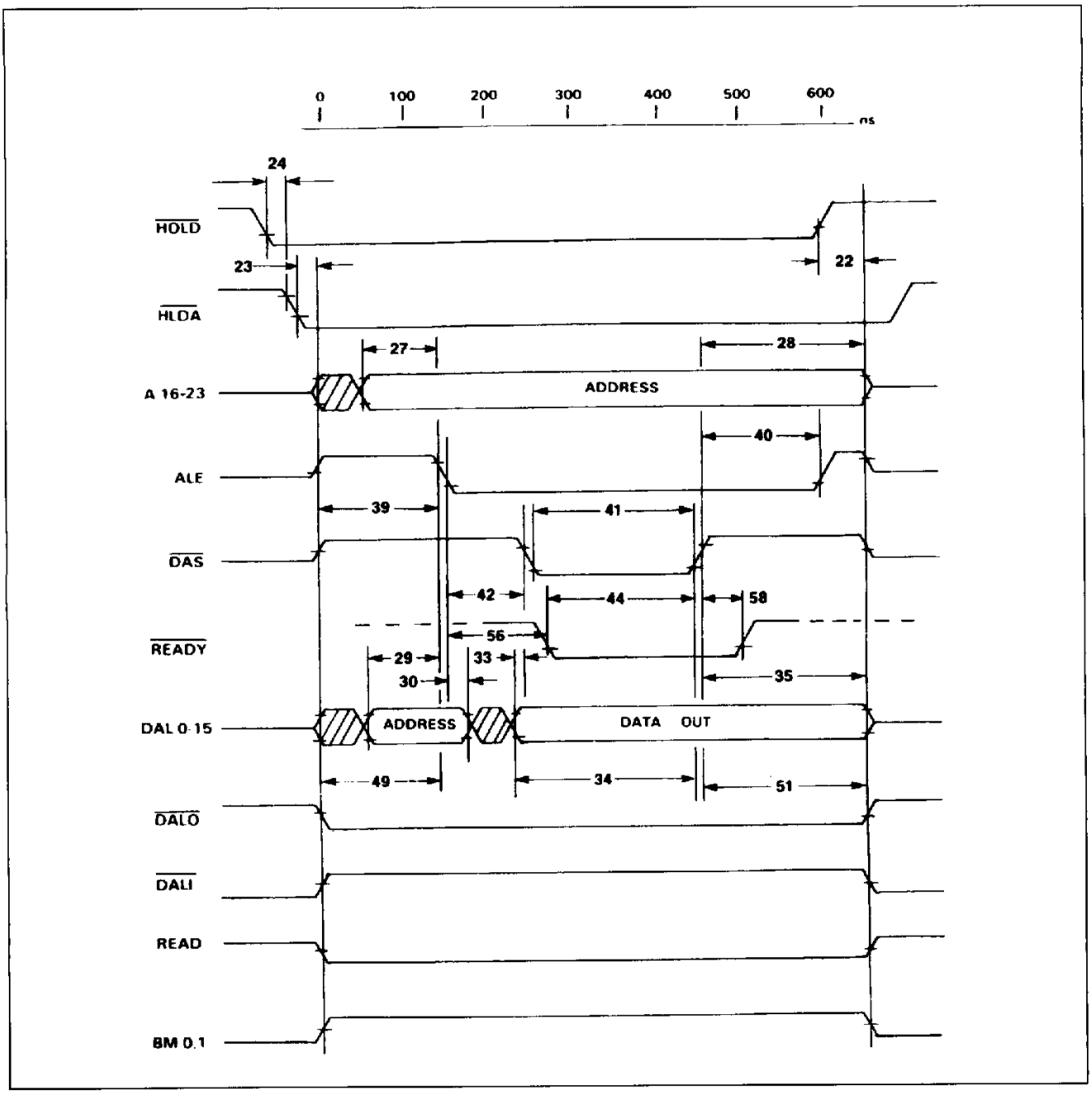
	"1"	"0"
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	90% V_{OH}	10% V_{OL}

Figure 10 : Bus Master Timing Diagram (Read).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

Figure 11 : Bus Master Timing Diagram (Write).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

Figure 12: MK5025 Bus Slave Timing Diagram (Read).

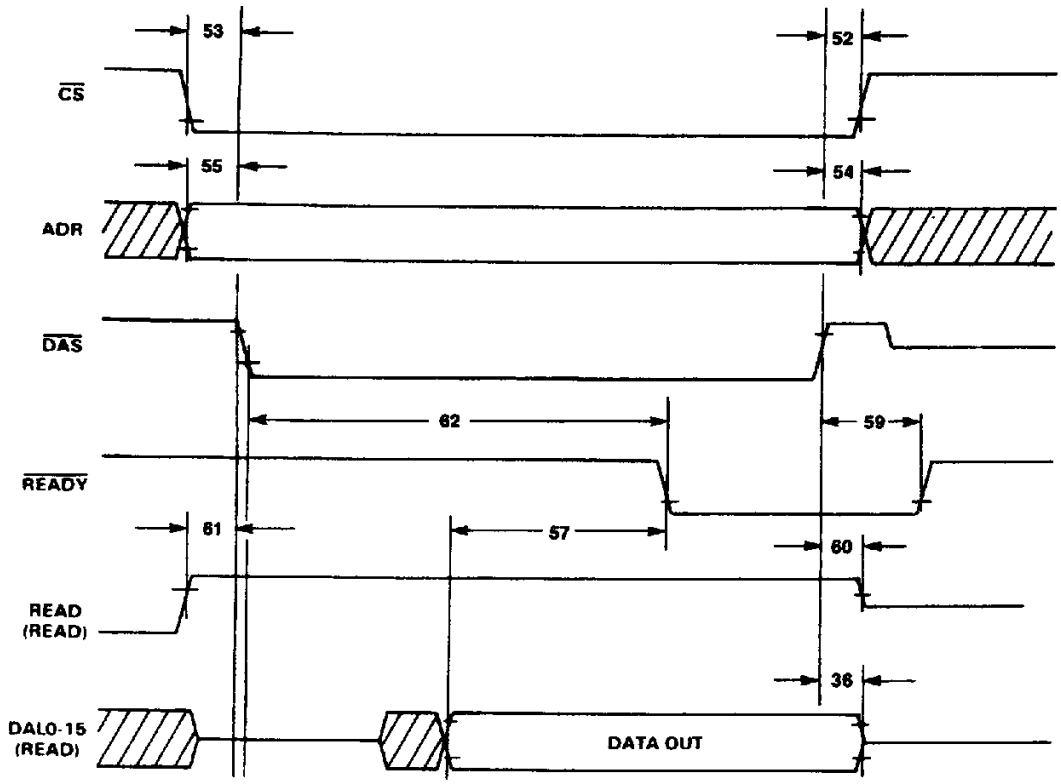
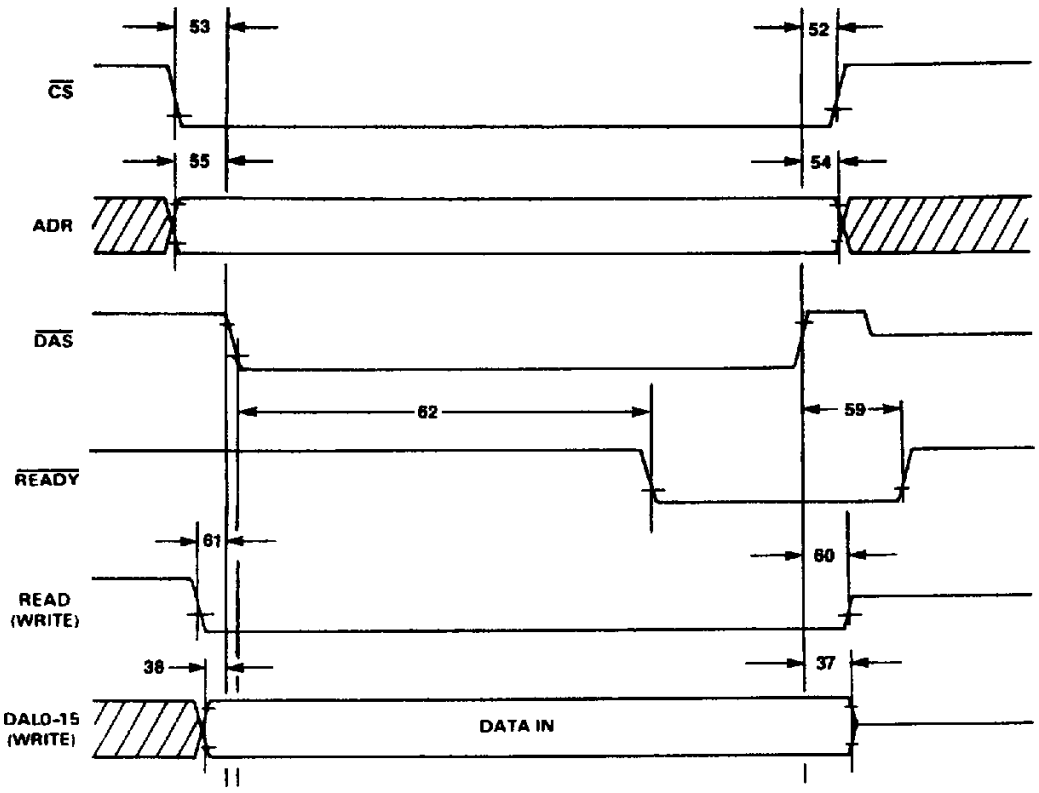


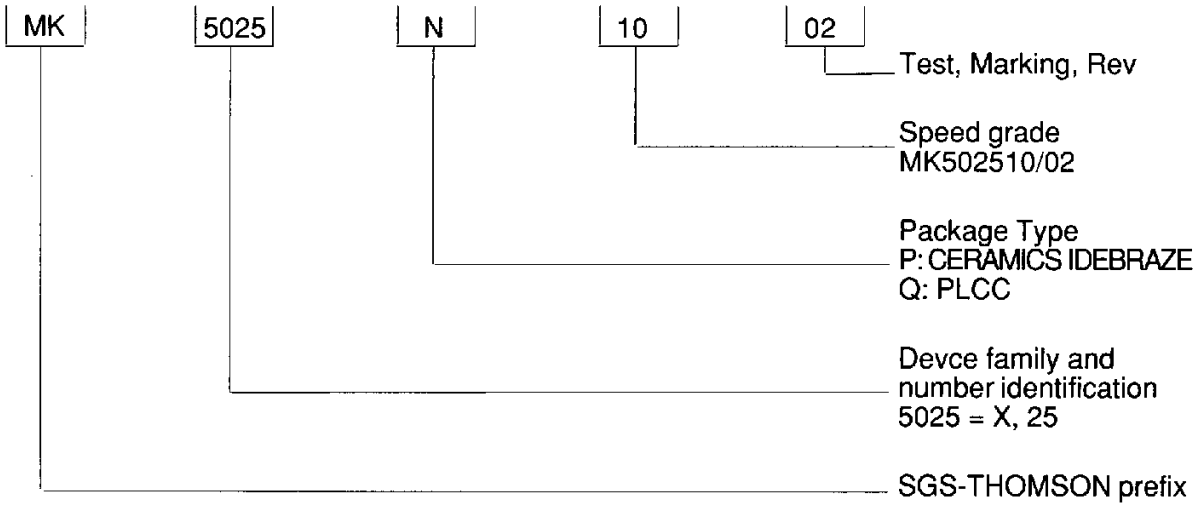
Figure 13: MK5025 Bus Slave Timing Diagram (Write).



ORDER CODES

Part Number	Description I/O	Data Rate	Clock Frequency	Temperature Range	Package Type
MK5025P-10/02	X, 25	7MB/s	10MHz	0°C to 70°C	CDIP48 600-MIL
MK5025Q-10/02		7MB/s	10MHz	0°C to 70°C	PLCC52

Note: CDIP = Ceramic Multilayer DIP, PLCC = Plastic leaded Chip carrier, PDIP = Plastic DIP.



MK5021Q10/0 Serial COM Controller, Frame Relay
MK5027P10/0 CCS#7
MK5027Q10/0 CCS#7