MOSTEK

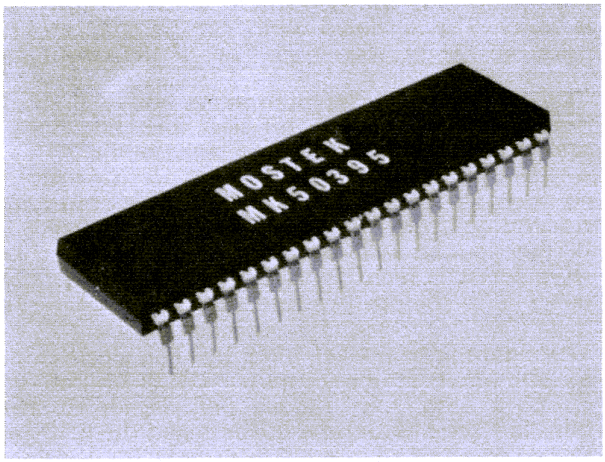
SIX DECADE COUNTER / DISPLAY DECODER

MK50395N / MK50396N / MK50397N

December 1976

FEATURES

- ☐ Single power supply
- ☐ Schmitt-Trigger on the count-input
- ☐ Six decades of synchronous up/down counting
- ☐ Look-ahead carry or borrow
- ☐ Loadable counter
- ☐ Loadable compare-register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal scan oscillator
- ☐ Direct LED segment drive
- ☐ Interfaces directly with CMOS logic
- ☐ Leading zero blanking
- ☐ MK 50396 programmed to count time: 99 hrs. 59 min. 59 sec.
- ☐ MK 50397 programmed to count time: 59 min. 59 sec. 99/100 sec.



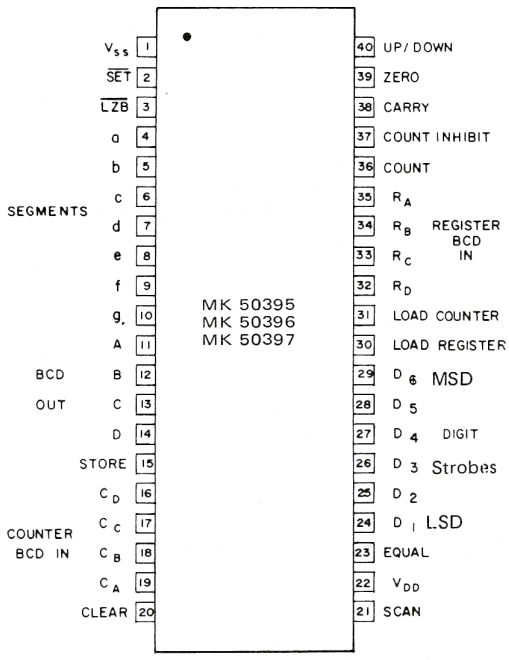
DESCRIPTION

The MK 50395 is an ion-implanted, P-channel MOS six-decade synchronous up/down-counter/display driver with compare-register and storage-latches. The counter as well as the register can be loaded digit-by-digit with BCD data. The counter has an asynchronous-clear function.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be driven by an external signal. The six-decade register is constantly compared to the state of the six-decade counter and when both the register and the counter have the same content, an EQUAL signal is generated. The contents of the counter can be transferred into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7-segment format to the output. The seven-segment decoder incorporates a leading-zero blanking circuit which can be disabled by an external signal. This device is intended to interface directly with the standard CMOS logic families.

The MK 50396 and MK 50397 operate identically to the MK 50395 except that two digits in each were reprogrammed to provide divide by six circuitry instead of divide by ten. The MK 50396 is well suited for industrial timer applications while the MK 50397 is best suited for stop watch or real time computer clock applications.

PIN CONNECTION



OPERATIONS:

SIX DECADE COUNTER, LATCH

The six decade counter is synchronously incremented or decremented on the positive edge of the count input signal. A Schmitt trigger on this input provides hysteresis for protection against both a noisy environment and double triggering due to a slow rising edge at the count input.

The count inhibit can be changed in coincidence with the positive transition of the count input; the count input is inhibited when the count inhibit is high.

The counter will increment when up/down input is high (V_{SS}) and will decrement when up/down input is low. The up/down input can be changed .75 μs prior to the positive transition of the count input.

The clear input is asynchronous and will reset all decades to zero when brought high but does not affect the six digit latch or the scan counter.

As long as store input is low, data is continuously transferred from the counter to the display. Data in the counter will be latched and displayed when store input is high. Store can be changed in coincidence with the positive transition of the count input.

The counter is loaded digit by digit corresponding to the digit strobe outputs. BCD thumb wheel switches with four diodes per decade connected between the digit strobe outputs and the BCD inputs is one method to supply BCD data for loading the counter decades.

The load counter pulse must be at V_{SS} 2 microseconds prior to the positive transition of the digit strobe of the digit to be loaded. The load counter pulse may be removed after the positive transition of the digit strobe since the chip internally latches this signal. The BCD data to be loaded must be valid through the negative transition of the digit strobe.

INPUTS, OUTPUTS

The seven segment outputs are open drain capable of sourcing 10mA average current per segment over one digit cycle. Segments are on when at V_{SS}. The Carry, Equal, Zero, BCD and digit strobe outputs are push pull and are on when at V_{SS}. All inputs except Counter BCD, Register BCD, and SCAN inputs are high impedance CMOS compatible.

Three basic outputs originate from the counter: zero output, equal output, and carry output. Each output goes high on the positive (V_{SS}) going edge of the count input under the following conditions:

Zero output goes high for one count period when all decades contain zero. During a load counter operation the zero output is inhibited.

Equal output goes high for one count period when the contents of the counter and compare register are equal. The equal output is inhibited by a load counter or load register operation, which lasts until the next interdigit blanking period following a negative transition of Load Counter or Load Register.

The carry output goes high with the leading edge of the count input at the count of 000000 when counting up or at 999999* when counting down and goes low with the negative going edge of the same count input.

A count frequency of 1 MHz can be achieved if the equal output, zero output and carry output are not used. These outputs do not respond at this frequency due to their output delay illustrated on the timing diagram.

SIX DECADE COMPARE REGISTER

The register is loaded identically to the load counter paragraph described previously. The register may be loaded independently of the counter, however, the clear input will not remove the register contents. Contents of the register are not displayed by the BCD or seven segment outputs.

BCD & SEVEN SEGMENT OUTPUTS

BCD or seven segment outputs are available. Digit strobes are decoded internally by a divide by six Johnson counter. This counter scans from MSD to LSD. By bringing the $\overline{SET}$ input low, this counter will be forced to the MSD decade count. During this time the segment outputs are blanked to protect against display burn out.

BCD outputs are valid for MSD when $\overline{SET}$ is low. Applying V_{SS} to $\overline{SET}$ allows normal scan to resume. Digit 6 output is active (V_{SS}) until the next scan clock pulse bring up digit 5 output.

The segment outputs and digit strobes are blanked during the interdigit blanking time. Leading zero blanking affects only the segment outputs. This option is disabled by bringing the $\overline{LZB}$ input high. Typically the interdigit blanking time is 5 to 25 microseconds when using the internal scan oscillator.

BCD output data changes at the beginning of the interdigit blanking time. Therefore the BCD output data is valid when the positive transition of a digit output occurs.

SCAN OSCILLATOR

The MK 50395 has an internal scan oscillator. The frequency of the scan oscillator is determined by an external capacitor between V_{SS} or V_{DD} and scan input. The wave form present on the scan oscillator input is triangular in the self oscillate mode.

An external oscillator may also be used to drive the scan input. In either case, external capacitors of 150pF each will be required from V_{SS} to Counter BCD inputs and register BCD inputs. This will allow asynchronous loading of the BCD inputs.

In the internal drive mode the interdigit blanking time will be the sum of the negative dwell period of the external oscillator and the normal self oscillate blanking time. (5 → 25 μsec). Display brightness can be controlled by the duty cycle of the external scan oscillator.

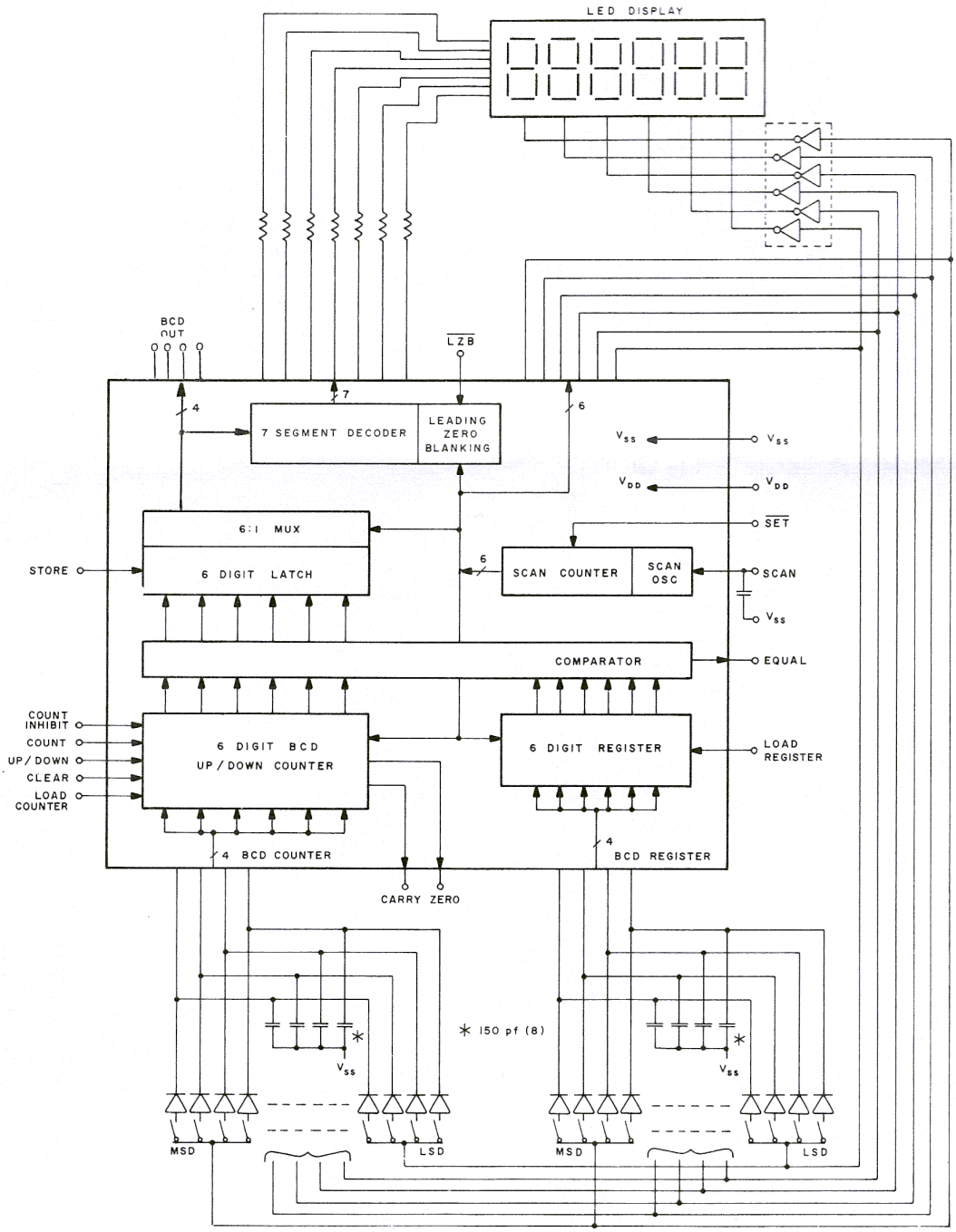
*Carry occurs at 99 59 59 for the MK 50396 and 59 59 99 for the MK 50397

If external capacitors on the BCD inputs are undesirable, it will be necessary to synchronize the negative going edge of the load register and/or load counter command to coincide with the positive going edge of the scan input signal. Also the V_{SS} range should be limited from 10.8 to 13.2 volts.

Typically, the scan oscillator will oscillate at the following frequencies with these nominal capacitor valves from V_{SS} to scan input.

	Min	Max
820pF	1.4KHz	4.8 KHz
470pF	2.0KHz	6.8KHz
120pF	7.0KHz	20KHz

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . +0.3V to −20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . -40°C to +100°C

MAXIMUM OPERATING CONDITIONS

	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Operating Temperature	0	70	C	
V_{SS}	Supply Voltage (V_{DD} = 0V)	10	15	V	1
I_{SS}	Supply Current		30	mA	2
B_V	Break Down Voltage (Segment only @ 10 μA)		V_{SS} − 26	V	
P_D	Power Dissipation		670	mW	3

ELECTRICAL CHARACTERISTICS

(V_{DD} = 0V, V_{SS} = + 10.0V to + 15.0, 0°C ≤ T_A ≤ 70°C)

Static Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IL}	Input Low Voltage, "0"	V_{DD}	$0.2V_{SS}$	V	
V_{IH}	Input High Voltage, "1"	V_{SS}−1	V_{SS}	V	4
V_{OL}	Output Voltage "0" @ 30μA		$0.2V_{SS}$	V	5
V_{OH}	Output Voltage "1" @ 1.5 mA	$0.8V_{SS}$		V	5
I_{OH}	Output Current "1"				
	digit strobes	3.0		mA	6
	segment outputs	10.0		mA	7
I_{SCAN}	Scan Input Pullup Current @ 0V		5.5	mA	
I_{SCAN}	Scan Input Pulldown Current @ 15V	2	40	μA	
$I_{\overline{SET}}$	$\overline{SET}$ Input Pullup Current @ 0V	5	60	μA	

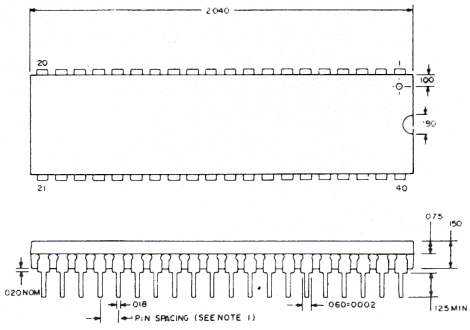
NOTES:
1. With 150 pF capacitor to V_{SS} from counter BCD and register BCD inputs.
2. I_{SS} with inputs and outputs open at 0°C. 28mA at 25°C and 25mA at 70°C. This does not include segment current. Total power per segment must be limited not to exceed power dissipation of package. (Θ_{JA} = 100 C/Watt)
3. All outputs loaded
4. MIN V_{IH} from R_A R_B R_C R_D C_A C_B C_C C_D inputs is V_{SS} −2.5V. Those inputs have internal pulldown reisitors to V_{DD}.
5. This applied to the push pull CMOS compatible outputs. Does not include digit strobes on segment outputs.
6. For V_{OUT} = V_{SS} −2.0 volts. Average value over one digit cycle.
7. For V_{OUT} = V_{SS} −3.0 volts. Average value over one digit cycle.

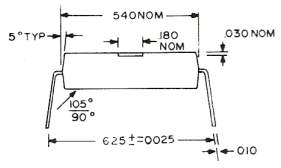
Dynamic Operating Conditions

	PARAMETER	MIN	MAX	UNITS	NOTES
f_{CI}	Count Input Frequency	0	1.00	MHz	8,9
f_{SI}	Scan Input Frequency	0	20	KHz	
t_{CPW}	Count Pulse Width	400		ns	10
t_{SPW}	Store Pulse Width	2.0		μs	
t_{SS}	Store Setup Time	0		μs	11
t_{CIS}	Count Inhibit Setup Time	0		μs	11
t_{UDS}	Up/Down Setup Time	−.75		μs	11
t_{CPW}	Clear Pulse Width	2.0		μs	11
t_{CS}	Clear Setup Time	− 0.5		μs	11
t_{OA}	Zero Access Time		3.0	μs	11
t_{OH}	Zero Hold Time		1.5	μs	11
t_{CA}	Carry Access Time		1.5	μs	11
t_{CH}	Carry Hold Time		0.9	μs	12
t_{EA}	Equal Access Time		2.0	μs	11
t_{EH}	Equal Hold Time		1.5	μs	11
t_L	Load Time	1/6 f_{SI}			

NOTES:
8. Measured at 50% duty cycle.
9. If carry, equal, or zero outputs are used, the count frequency will be limited by their respective output times.
10. The count pulse width must be greater than the carry access; time when using the carry output.
11. The positive edge of the count input is the t = 0 reference.
12. Measured from negative edge of count input.

PACKAGE DESCRIPTION 40-pin Dual In-Line Plastic

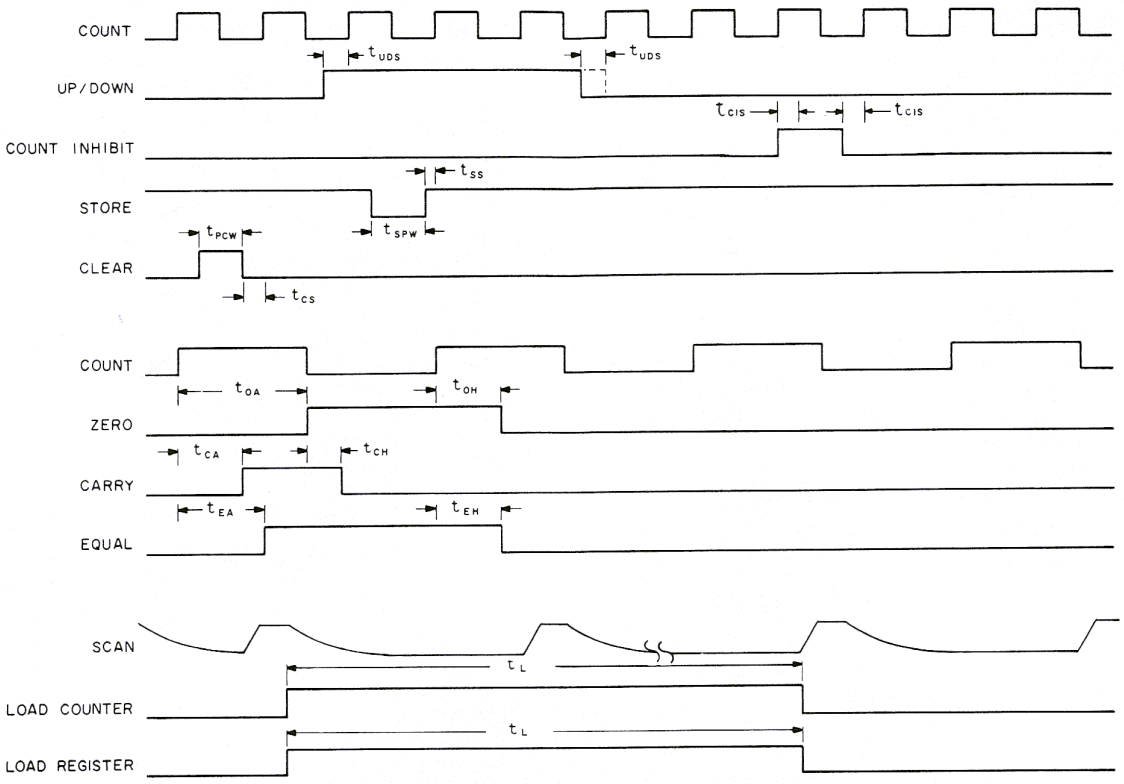




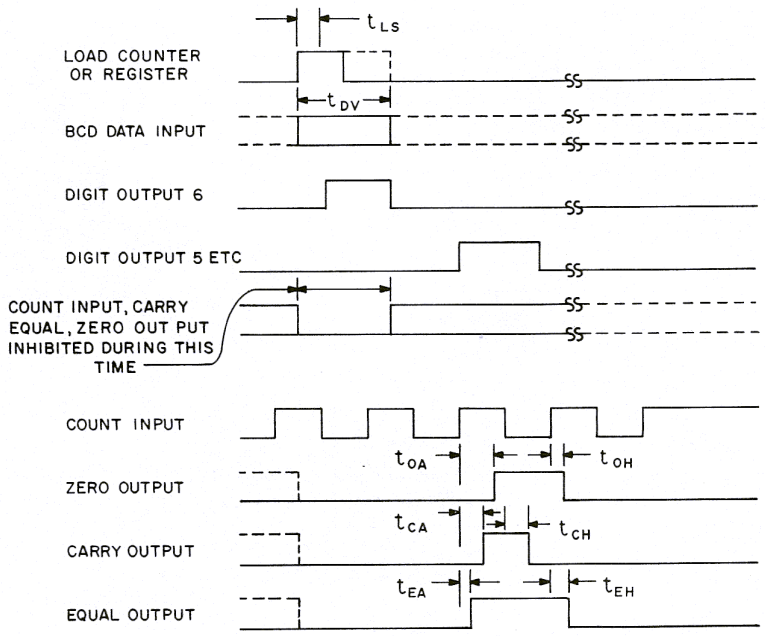
NOTE:

1. The true position pin spacing is 0.100 between center lines. Each pin centerline is located within± 0100 of its true longitudinal position relative to pins 1 and 40.

TIMING



LOADING COUNTER, REGISTER (1 DIGIT)



t_{LS} 2.0 μsec min NOTE: REF TO POSITIVE TRANSISTION OF DIGIT OUTPUT

t_{DV} 2.0 μsec min NOTE: REF TO NEGATIVE EDGE OF DIGIT OUTPUT

NOTE:

The inhibit function of the zero or equal outputs does not end when the Load Counter input goes to a "0" unless that transition occurs during interdigit blanking period at least 2.0 μsec prior to a positive transition of a digit output. This same timing restriction hold for Equal and Load Register.

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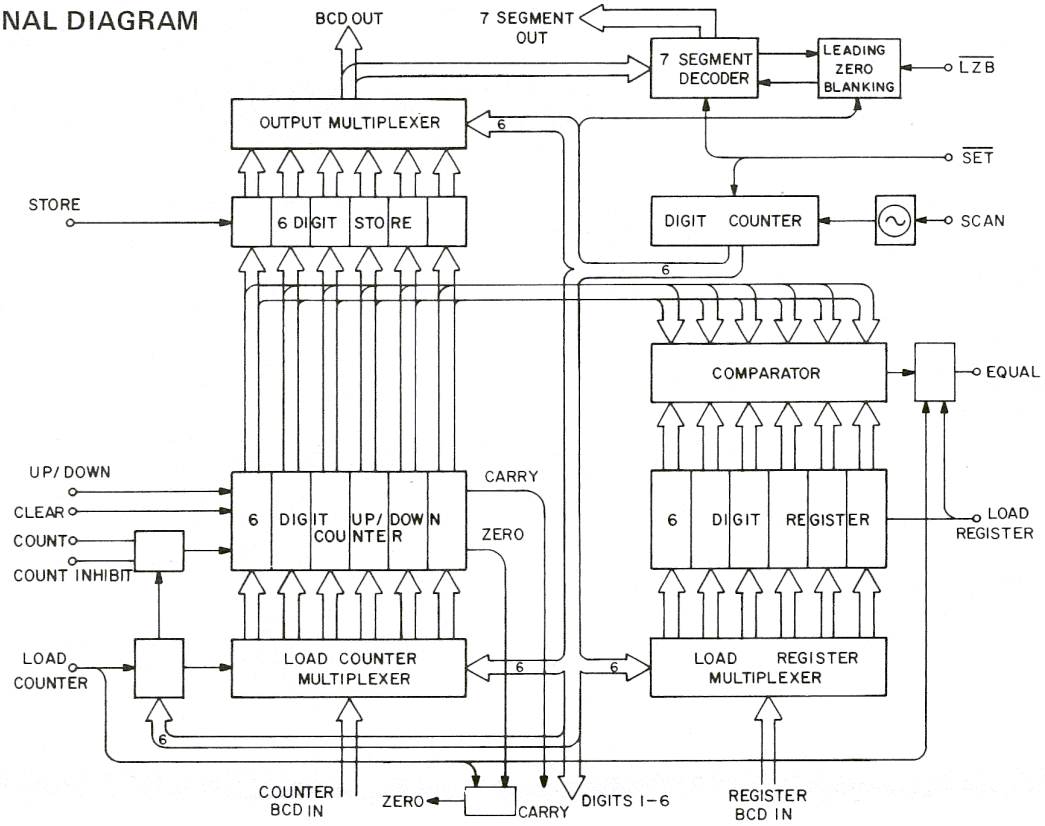
Application Information Using Mostek's Six-Decade Counter/Display Totalizer

FUNCTIONAL DIAGRAM



The MOSTEK MK 50395 has been developed, after careful counter application analysis, as a counting system for most needs. The functional diagram shows that the system consists of six, synchronous, up down decade counters with a data store and an auxiliary storage register that may be compared with the counter value. The circuit is relatively insensitive to power supply variation, and can interface with CMOS logic using power supplies in the 10 to 15 volt range. Counting speeds up to 1.0 MHz are permissable and the circuits are readily cascaded.

Positive logic, i.e., logic 1 is the more positive level in the following description:

THE COUNTER

The positive going edges of a pulse train at the COUNT input (pin 36) are standardized by an internal monostable to a fixed pulse width thereby giving only a minimum value to the time for which the input pulse must stay high. This pulse is applied synchronously to the six decades and if the UP/DOWN input is a logic 1 the counters will be incremented, if at logic 0 then the counters will be decremented. At any time the value in the counter will be set back to zero if the CLEAR COUNTER input goes to a logic 1 for 2 μs or longer. This resetting action occurs whether or not there is a counting input pulse train by forcing the counters directly to 0.

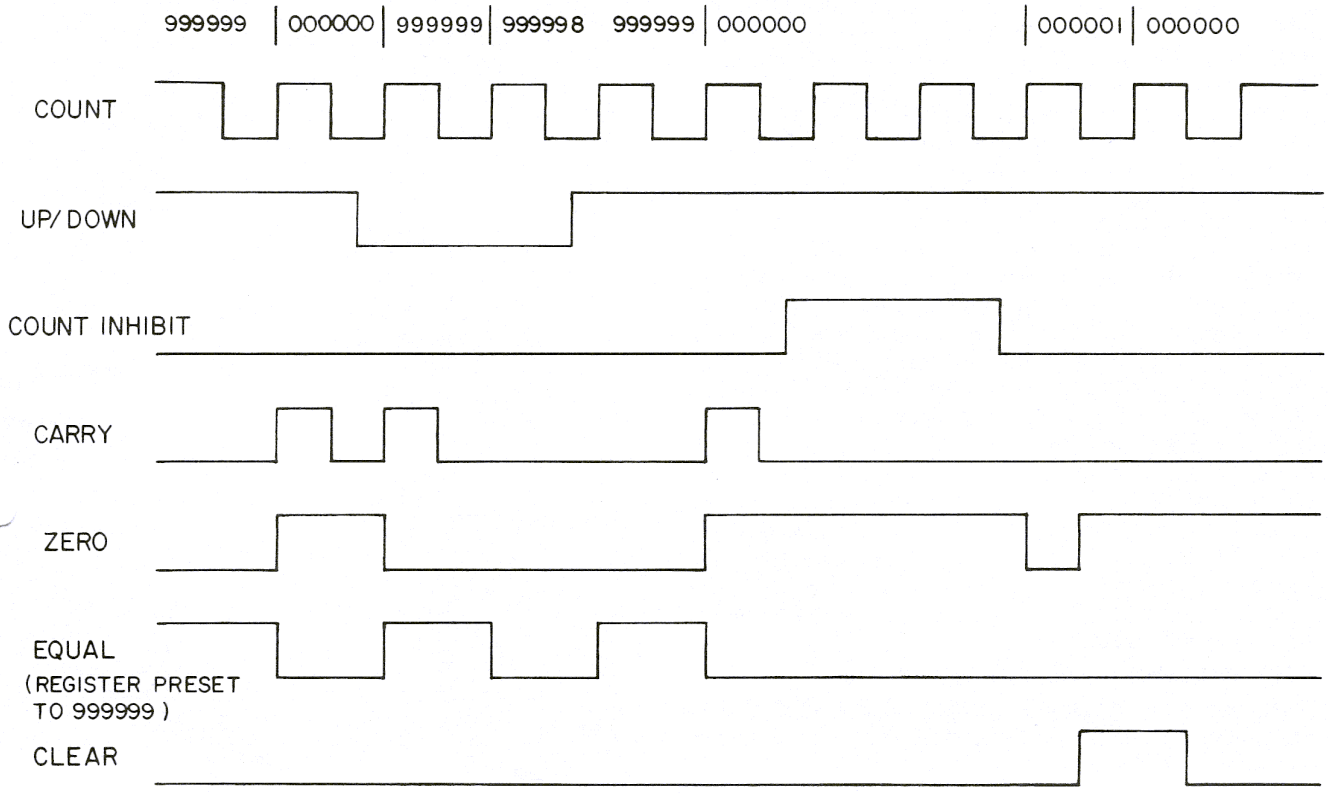
In addition to resetting it is also possible to preset any desired value into the counter. This is done sequentially decade by decade, under control of the LOAD COUNTER command in the following manner. If load counter is taken to logic one a minimum of 2 microseconds prior to the positive transistion of the digit output of the digit being loaded, the chip will latch this command and the BCD data presented to the counter will be loaded upon the negative transistion of the digit strobe. It is thus possible to load each of the 6 counters individually if required. While the counter is being loaded the counting input is inhibited. Internally the load counter command is synchronized to the scan oscillator. Thus if load counter is brought to a logic zero in the middle of a digit strobe, the counter will remain inhibited until the next interdigit blanking time. A separate COUNT INHIBIT control is provided to stop the applied count inputs from being accepted while this signal is a logic 1.

The counter section has two control outputs, a CARRY from the most significant decade and a ZERO SIGNAL that indicates when the counter contents are zero. These signals are suppressed during LOAD COUNTER operations to avoid a spurious output being given during a counter presetting operation.

COMPARISON AND REGISTER

The six digit storage register may be preset to any value by bringing the LOAD REGISTER signal to logic 1. The presetting sequence is exactly the same

UP/DOWN COUNT TIMING

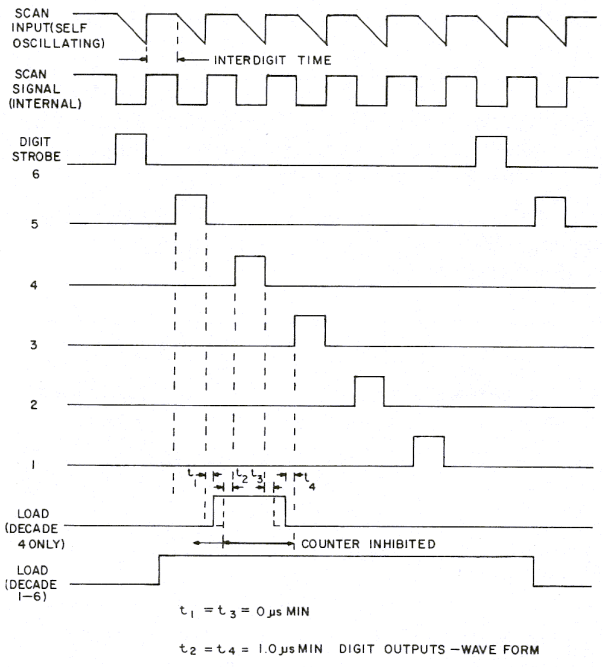


as for counter. The value on the REGISTER BCD INPUTS being loaded decade by decade by the six digit signals in the order "most significant" (digit 6) to "least significant" (digit 1). The outputs of this register are compared continuously with the value currently in the counter, this comparison is made in parallel and not decade by decade. When the two values are the same an EQUAL signal is given, however, during presetting of either the counter or the register, the CARRY, ZERO and EQUAL signals are inhibited so that no false, intermediate comparison result is given. Since the counter and the register have separate BCD inputs both may be preset simultaneously if desired. The value held in the register can only be altered by the BCD inputs. The Count Input is not inhibited during load register operations.

DIGIT SCANNING AND OUTPUT FUNCTIONS

The digit scan counter is timed from an internal oscillator which may be driven externally from the SCAN input. A capacitor attached from V_{SS} to this pin will determine the scan frequency when an external logic drive to this pin is not used. Internal circuitry gives a fixed delay to the DIGIT OUTPUT signal to ensure that there is a gap between each digit strobe, thus a "ghosting" effect in a displayed output due to the storage time of external display driver transistors is eliminated. This is the interdigit blanking time. Typically this time can range from 3 to 10 microseconds.

LOAD COUNTER, REGISTER TIMING



$\overline{\text{SET}}$ input is used to force the digit strobe counter to the digit 6 position for purposes of synchronizing the counter output. The digit counter outputs are gated by the interdigit blanking period and appear as DIGIT STROBE OUTPUTS. The counter outputs are not directly multiplexed but are buffered by a 6 digit latch controlled by the STORE command. The outputs of the latch go directly to the output multiplexer, thus when the STORE signal is at logic 0 the counter contents are directly available but as soon as STORE goes to logic 1 the value present as the signal changed is retained and subsequent changes in counter value are ignored. The contents of the store are read out, digit by digit — the scan counter again performs this function in the order most significant to least significant— and appear on BCD OUT pins. The four bits in each BCD digit are encoded simultaneously to seven segment code and appear as SEGMENTS OUT and can be used to drive a suitable 7 segment display. The $\overline{\text{SET}}$ operation will also turn off these seven outputs, blanking the display, as well as setting the digit counter to digit 6. This is to preven possible destruction of an LED type display when $\overline{\text{SET}}$ is a prolonged signal. Frequently it is required to display only significant numbers, in which case taking the $\overline{\text{LZB}}$ control to a logic 0 will blank the leading zeros in the seven segment output.

INTERFACING WITH THE MK 50395

The wide range of power supply, 10.0 — 15.0, makes the counting system particularly suitable for interfacing with CMOS logic.

A. Segment output — these transistors can source 10 mA from the V_{SS} supply, there is no internal pull down to V_{DD} when the transistor is turned off. These transistors are capable of driving small LED displays directly via series resistors.

B. Digit outputs — a push pull configuration is used here as the most suitable arrangement for driving both external logic and display drivers. These outputs supply 3.0 mA max from V_{SS} and sink 30 μA to V_{DD}.

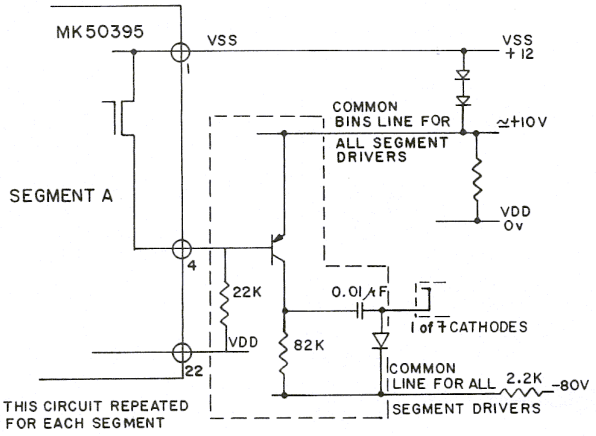
When higher power displays are used the segment outputs should be buffered by an emitter follower in order to provide the extra current.

The BCD OUTPUTS, EQUAL, ZERO and CARRY are also push-pull. Output drive capabilities are listed in the following table:

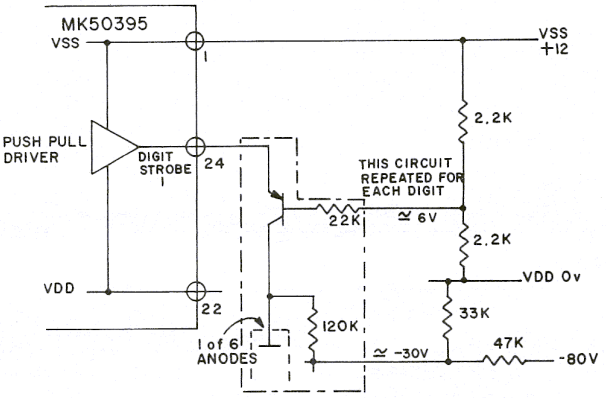
	VOL	VOH
Segment Output (Pins 4-10)		V_{SS}–3V at 10mA (average over one digit strobe cycle)
Digit Outputs (Pins 24-29)	V_{DD} at no load .2 V_{SS} at 30 μA	V_{SS}–2V at 3.0mA
Equal/Zero/Carry (Pins 23,39,38)	V_{DD} at no load .2 V_{SS} at 30 μA	V_{SS} –2V at 1.5mA

The following inputs, COUNT, STORE, UP/DOWN, COUNT INHIBIT, CLEAR, $\overline{\text{LZB}}$, LOAD REGISTER have no internal current sources and must therefore be driven from sources that give correct logic 1 and 0

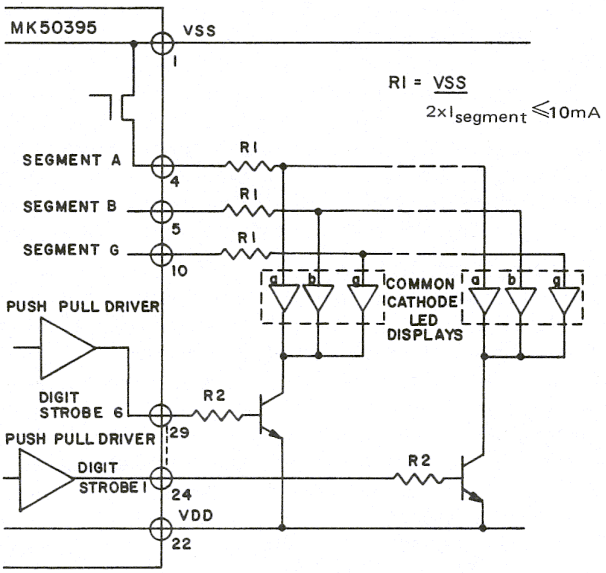
SEGMENT DRIVER



DIGIT DRIVER



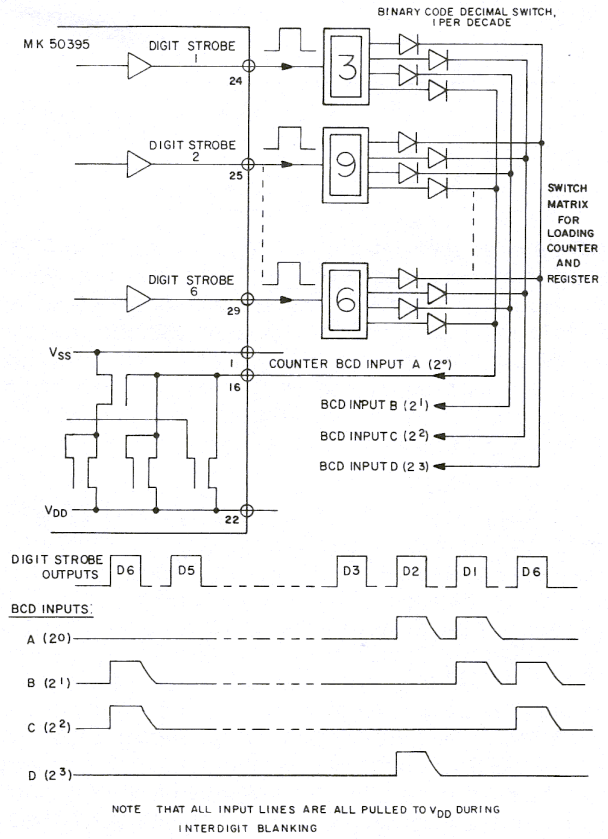
DRIVING LED DISPLAYS DIRECTLY



levels – open collector circuits, or switches without pull down resistors for example, may not be used. If any of the above functions are not required then those pins should be tied to the appropriate supply, that is to V_{SS} for logic 1 and V_{DD} for logic 0. SET has an internal transistor that pulls the pin to V_{SS} if unconnected thus the driving circuit should be able to sink this current, approximately 60 μA, when pulling the input to logic 0. The COUNTER BCD and REGISTER BCD inputs have two internal transistors one static and one switched as a precharge, that pull to V_{DD}. The static current is $< 350\ \mu A$ to V_{DD} when the input is taken to V_{SS}, the dynamic current from V_{SS} is 1 mA while the transistor is on. The dynamic precharge ensures that even with the large capacitive loading and leakage current of a switch matrix at these pins, the correct data will be entered at the maximum digit scan frequency.

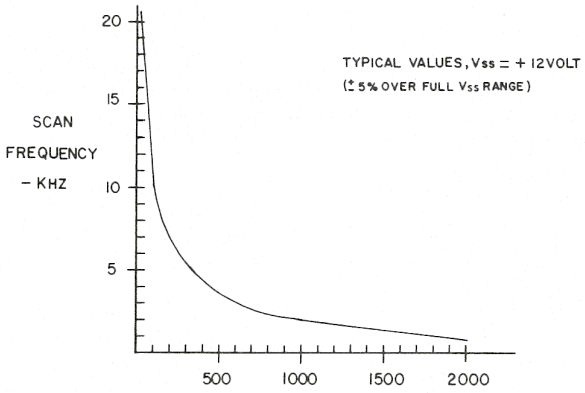
An example of a switch matrix input illustrates this operation. Six binary coded decimal switches are used, one for each decade, the switches being enabled by the corresponding DIGIT STROBE output, with the paralleled switch outputs connected to the COUNTER (or REGISTER) BCD inputs. The DIGIT STROBE outputs are separated by the interdigit blanking time and it is only during this time that the precharge transistors at the BCD inputs are all pulled to logic 0 (V_{DD}). After this blanking time the next DIGIT STROBE output will in its turn switch to logic 1 (only one out of six is ever on) and pull those BCD inputs selected by the switch and diode matrix to logic 1. This value is loaded into the corresponding register or counter stage, i.e. the switch matrix driven by DIGIT STROBE 6 will be loaded into MSB of the register or counter. As the DIGIT STROBE switches back to logic 0 the next interdigit blanking time begins and the inputs are all pulled back to logic 0 again by the internal precharge. It is possible for the DIGIT STROBE outputs to drive both the switch matrix and a display. If the COUNTER & REGISTER BCD inputs are connected in parallel they may still be driven driectly from the DIGIT STROBE outputs.

BCD SWITCH MATRIX



NOTE THAT ALL INPUT LINES ARE ALL PULLED TO V_{DD} DURING INTERDIGIT BLANKING

SCAN FREQUENCY VS EXTERNAL



When the scan oscillator is free running the SCAN input may use an external capacitor to set the scanning frequency to a particular value. The signal seen at the pin is a ramp determined by the capacitance, followed by a period clamped at V_{SS}. This period clamped at V_{SS} is determined by the internal oscillator and is the interdigit blanking period. During this time the DIGIT STROBE outputs are all turned off. When the SCAN input is driven externally this fixed interdigit period remains plus the time at which the synchronizing signal is at logic 0. To make the interdigit blanking time independent of the external synchronizing signal requires only the addition of a resistor and capacitor.

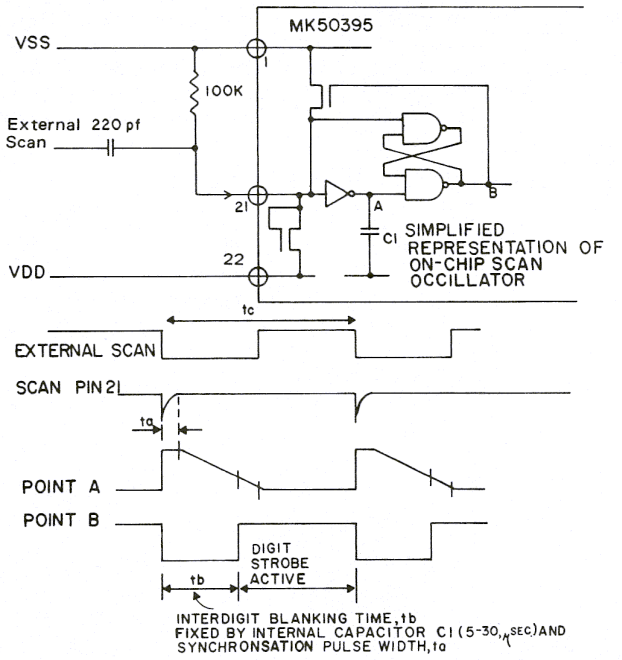
Time A is the interdigit blanking time, time B should be greater than 2 μs – a range of 2 – 5 μs is suitable and time C may be from infinity to 30 μs. If time C is made too short then the interdigit blanking circuit never resets itself and will stay at logic 0 and no DIGIT STROBE outputs will appear.

TYPICAL MK 50395 APPLICATIONS

BATCH CONTROL

In many situations involving the metering of material, whether as a liquid, individual items or revolutions of a spindle, a two step operation is required for better efficiency. The flow is started at the maximum speed and at a preset point before the end of the operation a signal is required to slow down and eventually stop the equipment. Such applications could be as diverse as filling sacks with cement or controlling the turns on a transformer bobbin. A block diagram of such a system is presented. Pressing the start switch allows the input to the D flip flop to go to logic 1. This is clocked by the DIGIT STROBE 6 so that a synchronous signal at least one complete scan counter cycle

EXTERNAL DRIVE TO SCAN INPUT



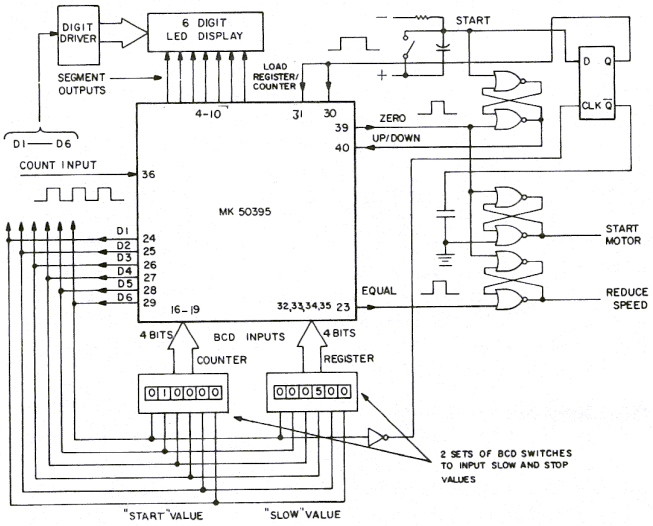
long is obtained. This signal is used as LOAD COUNTER and LOAD REGISTER, the two controls being tied in parallel for simultaneous loading. It does not matter how long the load signal is as long as it is at least one scan cycle long and changes synchronously with the scan signal. The two values representing total quantity and "slow down" quantity are set on the digit switches and these values are loaded at the beginning of each cycle. Once the counter register loading is complete a start signal is generated to set the equipment in operation. The train of pulses representing the measured quantity is counted, the UP/DOWN control is in the down mode. Thus with two quantities at, let us say, 10 000 and 500 the counter starts off with 10 000 loaded and counts toward zero. When the counter reaches 500 an EQUAL signal is generated and this sets the signal controlling the brake. A further 500 pulses and the counter reaches zero, an output on the ZERO pin resets the start flip flop and the equipment is brought to reset awaiting a new start signal. In such an operation the display outputs would probably not be used.

This application can be extended by using the ZERO output to control the UP/DOWN input. The operation is identical but the start signal also sets a latch into the count down state. As ZERO is detected this latch is reset so that the counter mode is now up. Even with a braking facility there may be an "overrun" and the value now held in the counter and displayed is the extra quantity. The operator may now decide if this extra quantity is within the tolerance allowed for the job and to take whatever action is necessary.

POSITIONAL MEASUREMENT

Positional measurement can readily be made using this circuit, the six decades gives considerable accuracy

BATCH CONTROL



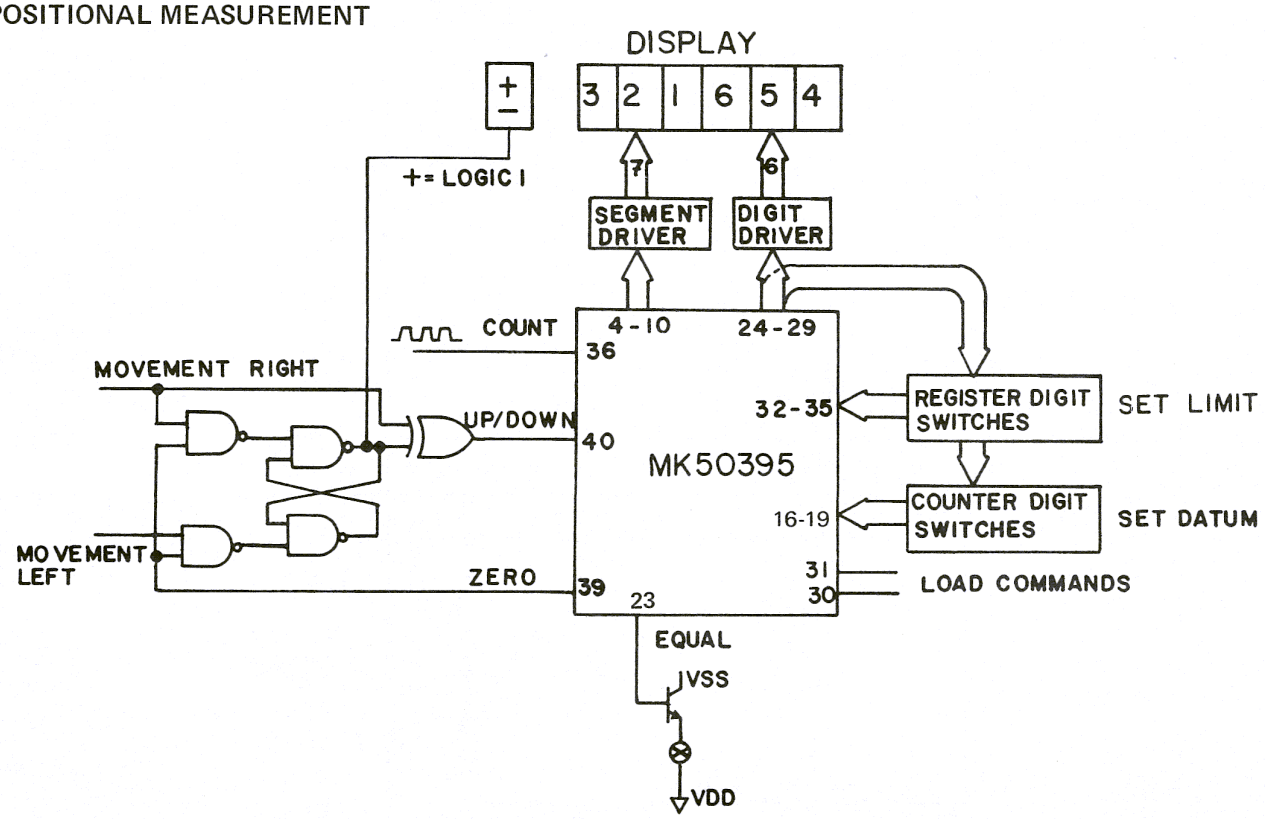
in one package. The two quadrature signals from a graticule type displacement measurement system must be converted to count impulses and an UP/DOWN signal. If the measurement zero datum is in the middle of the measurement area then the following counting conditions arise:

Direction of Movement	Displayed sign + or — of Datum	Count direction	
RIGHT	—	DOWN	ZERO DATUM CROSSED
RIGHT	+	UP	
LEFT	+	DOWN	ZERO DATUM CROSSED
LEFT	—	UP	

Each time the zero datum is reached and each time the direction of movement is changed then the count direction must be changed. The value displayed thus represents the position either side of the zero datum. The storage register may be used as a means of limiting the travel of the measurement piece, if a value equal to the limit is loaded into the register the EQUAL output may be used to give a warning that the limit is reached.

It will have been noted from the delay of EQUAL and ZERO to the COUNT edge (Fig. 2) that ZERO has as much longer propagation delay than the EQUAL output. In the event that the register is not used it may be loaded with zeros — by giving a LOAD REGISTER command with the BCD inputs as zero — and the EQUAL output then used as zero detect. This has the advantage of increasing the system speed for although the counter can accept inputs up to 1.0 MHz the propagation delay of the outputs is too long to allow a control signal to be changed between clock pulses at this counting rate. In this example UP/DOWN has to be controlled and using the faster output enables

POSITIONAL MEASUREMENT



a higher counting speed to be used if necessary in this case approximately 600 KHz instead of 300 KHz.

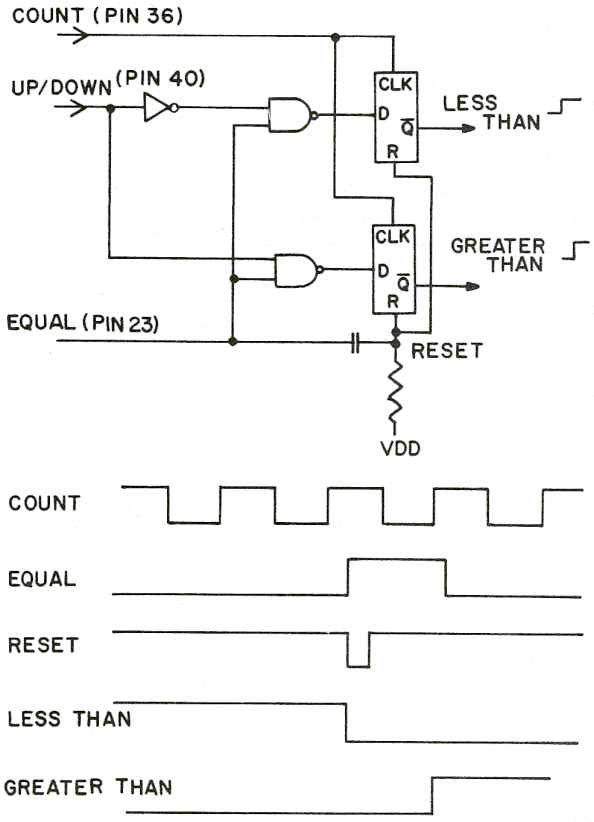
GREATER THAN – LESS THAN DETECTION

The availability of an EQUAL output facilitates the generation of greater than and less than signals, the only requirement is the circuit is set into the correct initial state. When the counter has the same value as the register the generation of the "greater/less than" signal depends on the direction of count, i.e. from this EQUAL condition count up gives "greater than" and count down gives "less than". EQUAL is gated with UP and with DOWN and these are connected to the D inputs of two D flip flops that are both clocked by the counting pulse. As EQUAL is reached the two flip flops are reset but the next count pulse after the EQUAL condition will set one or other of the flip flop and thereby provide the appropriate signal.

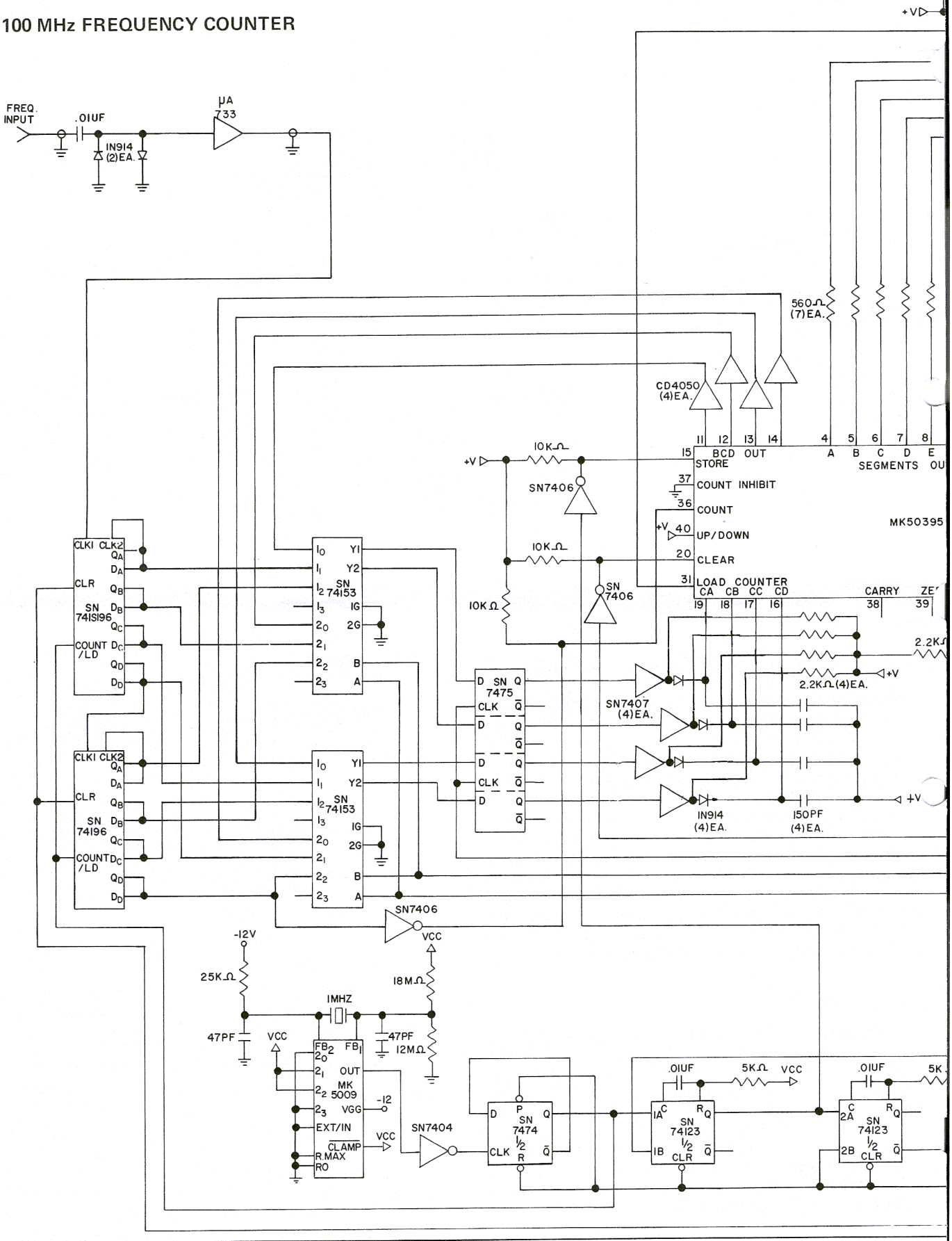
AUTOMATIC STOP

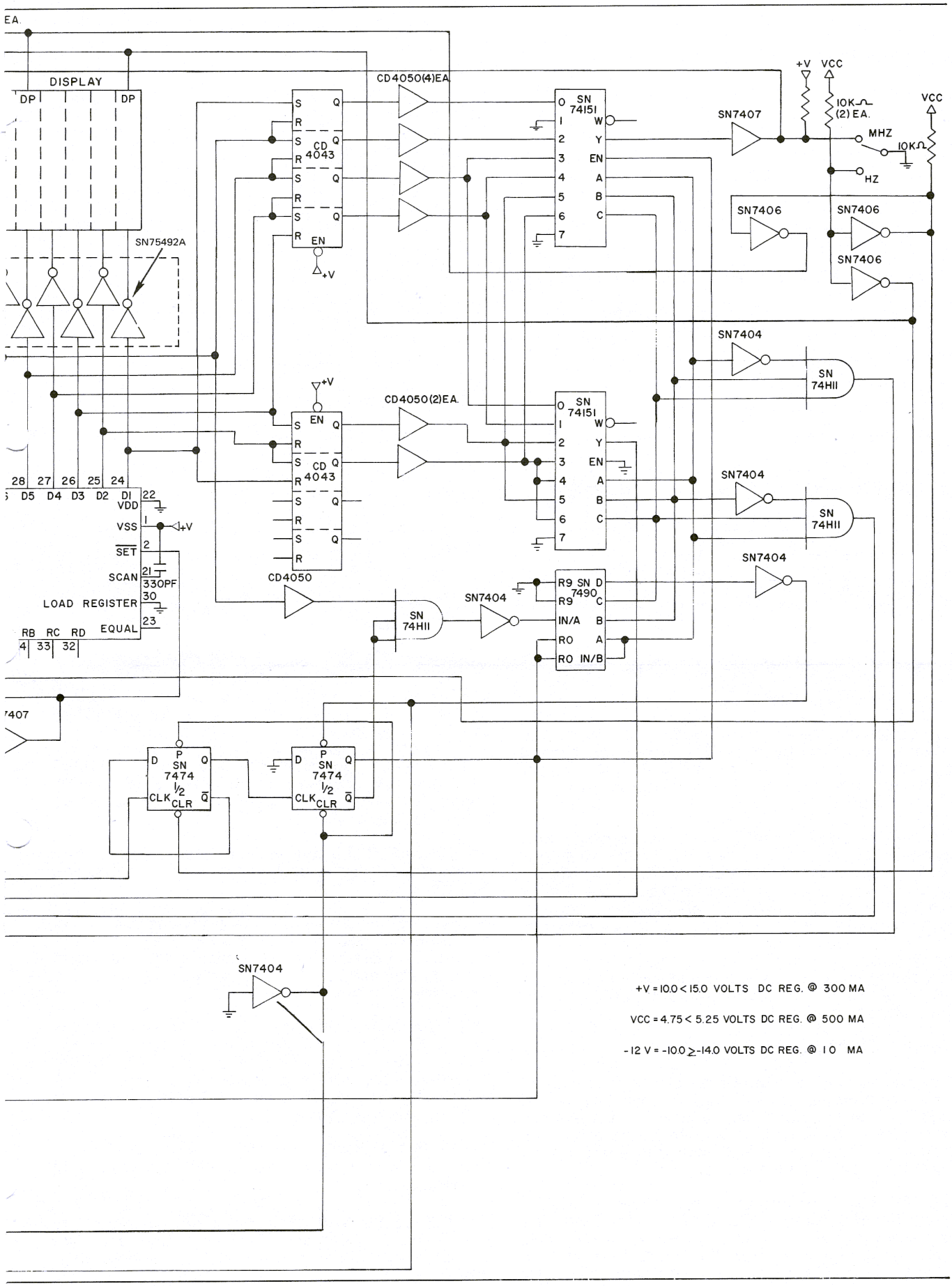
The COUNT INHIBIT input may be used to stop the counter automatically when the EQUAL or ZERO outputs are connected directly to this input. As EQUAL, for example, goes to a logic 1, then further counting is inhibited when this signal is connected directly to COUNT INHIBIT. Since no more count inputs are accepted the EQUAL value remains and blocks the counting action. The operation of CLEAR, LOAD REGISTER or LOAD COUNTER can be used to start the system counting again.

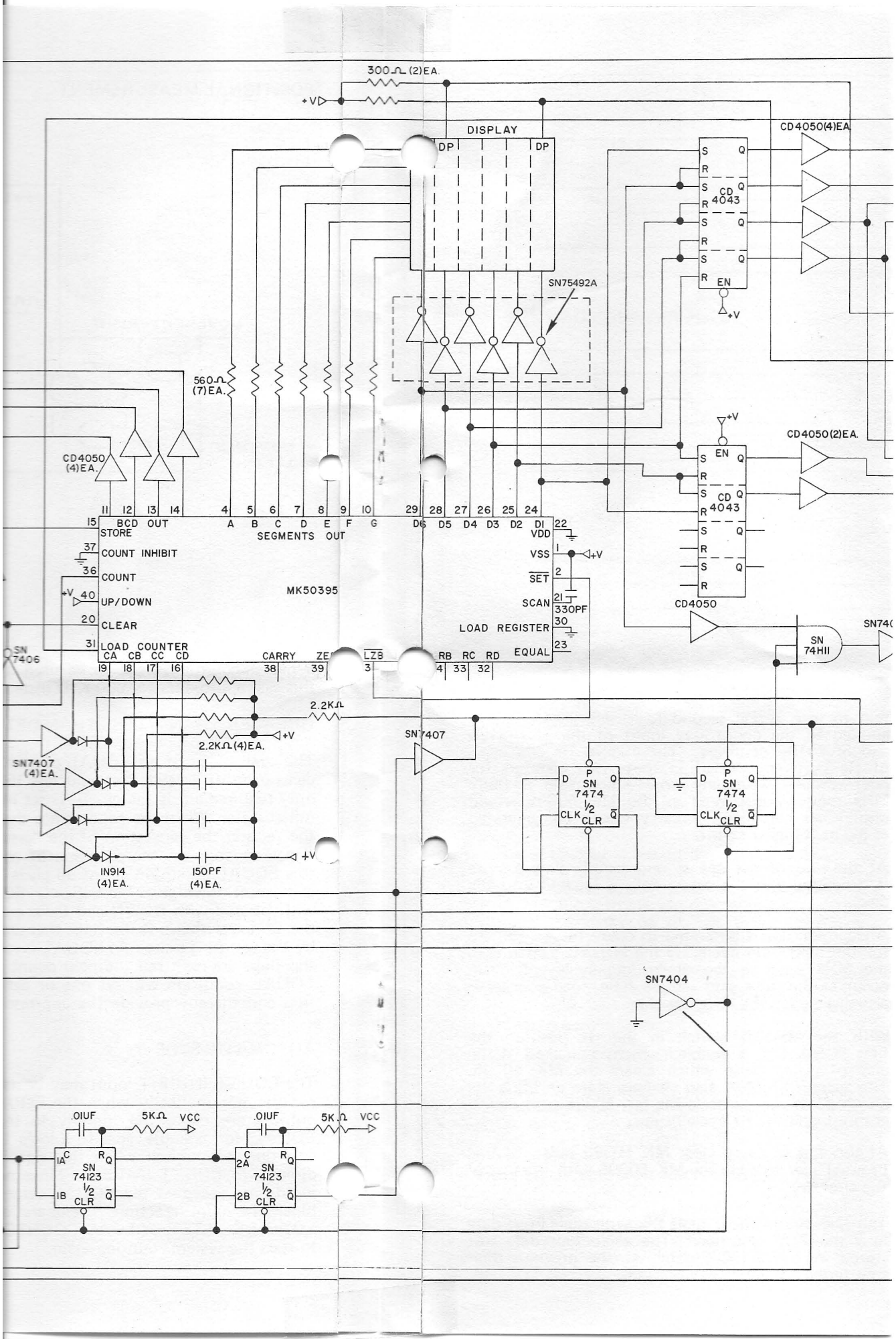
LESS THAN GREATER THAN



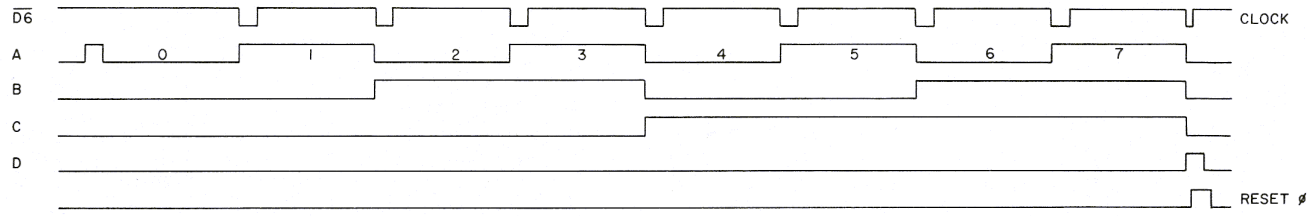
100 MHz FREQUENCY COUNTER



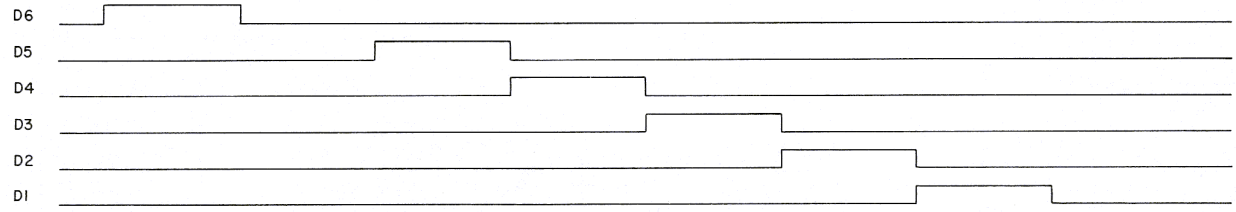




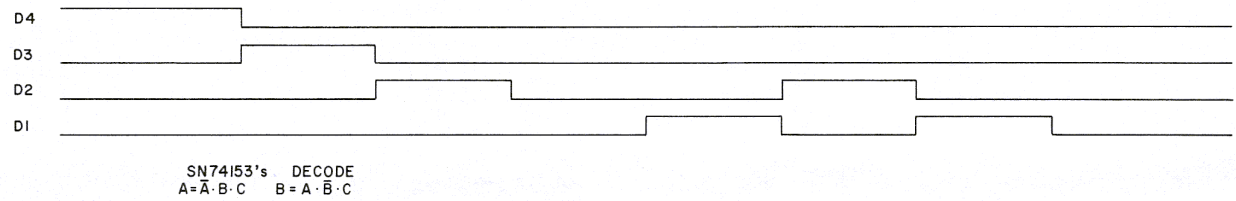
SN 7490 TIMING



SN 74151 LOAD COUNTER PULSE TRAIN OUTPUT



SN 74151 OUTPUT TO BCD LATCH ENABLE



MORE APPLICATIONS

The following applications resulted from an ad contest sponsored by Mostek. These applications represent a cross section of uses for the MK 50395 family and are intended as a guide for applying the counter circuit.

The type of display is left to the user to design into his particular application. The MK 50395 series was designed to allow direct drive of efficient display systems. If the current requirements of a display exceed the specifications of MK 50395 series external segment drive circuitry will be required.

Power supply; voltage range, wattage, filtering, and decoupling must be observed in all applications. The MK 50395 series was designed to keep power supply restrictions to a minimum.

100 MHz FREQUENCY COUNTER

In most counter applications the problems associated with prescaling result in a loss of resolution, or the need for longer count sample times. This application allows the MK 50395 with some associated circuitry to count at a 100 MHz with a one second gate time achieving one Hz resolution.

The MK 50395 counts the input frequency after a divide by 100 using a SN74S196 and a SN74196. Frequency sample time is achieved by a one MHz crystal in conjunction with the MK 5009 time base in the 10^6 configuration, followed by a divide by two to give a one second logic one level. This is applied to the count/load input of the SN74S196 and SN74196 counters. The 10's of Hz and one's of Hz data is retained in these two counters for later display. Actually only a count of 99.9999 MHz may be displayed as the MK 50395 would display all zeros and a carry would be generated at the next higher count.

At the end of the one second sample time a store is generated and the count data is latched into the display.

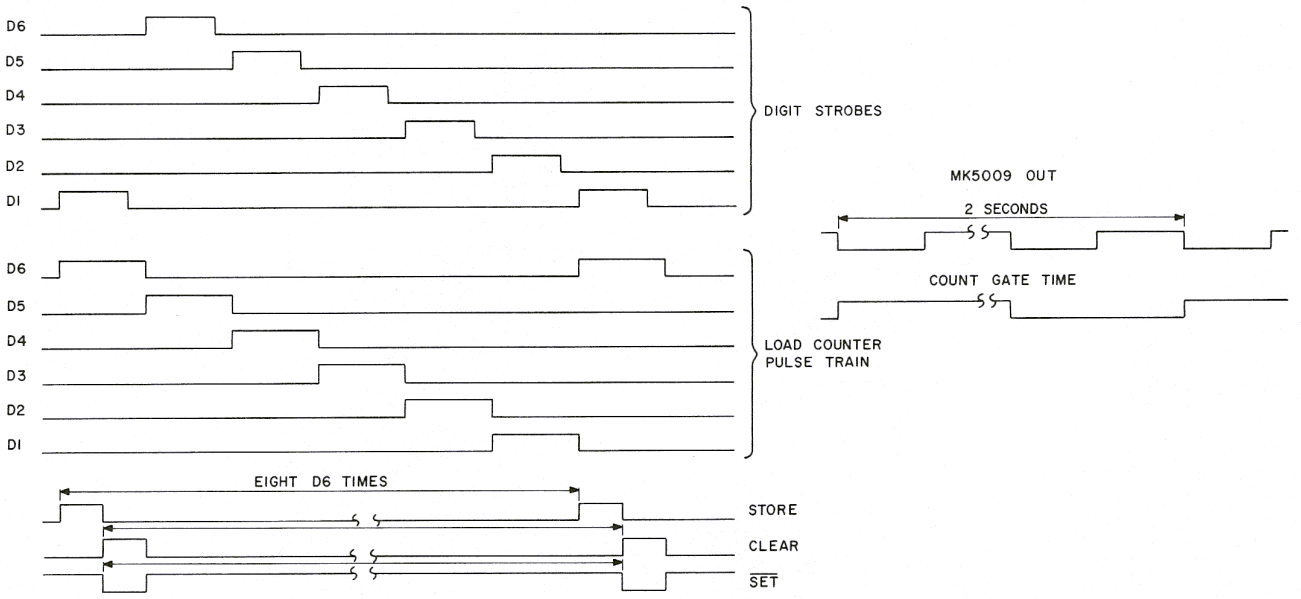
A clear counter is generated to ready the MK 50395 for the next data cycle. If the MHz-Hz switch is in the MHz position the preceeding cycle will again occur at the next gate sample time, load counter is also disabled in the MHz position.

With the MHz-Hz switch in the Hz position the first ½ SN7474 is enabled which is clocked at the end of every pulse which clears the MK 50395. The second SN7474 also changes state enabling the SN74151 which controls the MK 50395 load counter input, and the Hz cycle begins.

At the end of every clear MK 50395 pulse, $\overline{SET}$ is brought low to sync the MK 50395 with the rest of the circuitry.

The MK 50395 loads digit Six with digit Four data into the BCD counter. The digit four data was stored in the SN7475 latch at the previous digit four time.

TIMING DIAGRAM



The SN7490 is advanced one count at the digit six time at the start of the sequence.

Latch Digit Four Data,
Load Into Counter Digit Six

Latch Digit Three Data,
Load Into Counter Digit Five

Latch Digit Two Data,
Load Into Counter Digit Four

Latch Digit One Data,
Load Into Counter Digit Three

At this time the output of the SN7490 is decoded to select via the SN74153's first digit two data, then digit one data is selected which at the end of sample time was stored in the SN74196 and SN74S196. So the sequence is continued.

Latch Digit Two Data
Load Into Counter Digit Two

Latch Digit One Data
Load Into Counter Digit One

At the beginning of the eight count of the SN7490 several things take place. The MK 50395 is furnished with a store pulse to display the shifted data. A clear is applied to the MK 50395 to ready it for a new cycle.

The divide by two action of the first ½ SN7474 allows the second clear clock to have no effect at the second clear pulse. The SN74S196 and SN74196 are cleared. The second ½ SN7474 is preset which disables the load counter SN74151. The SN7490 is reset to zero.

To improve front end sensitivity a suitable wide band amplifier may be used. A typical device would be a μA 733. Timing diagrams for the MK 50395 and the associated circuitry are provided to further describe the various functions.

DARKROOM TIMER – A TYPICAL APPLICATION

A darkroom timer capable of being set for time periods from 99 minutes and 59 seconds is illustrated, The time interval to be set is entered into the BCD thumbwheel switches. Upon pressing the start button, the time indicated on the thumbwheel switches causes the counter to be loaded identically. Diode CR1, loads the register for a prewarning signal (8 seconds in diagram) prior to the end of the time interval so the operator can be altered to the fact, the time interval is about over.

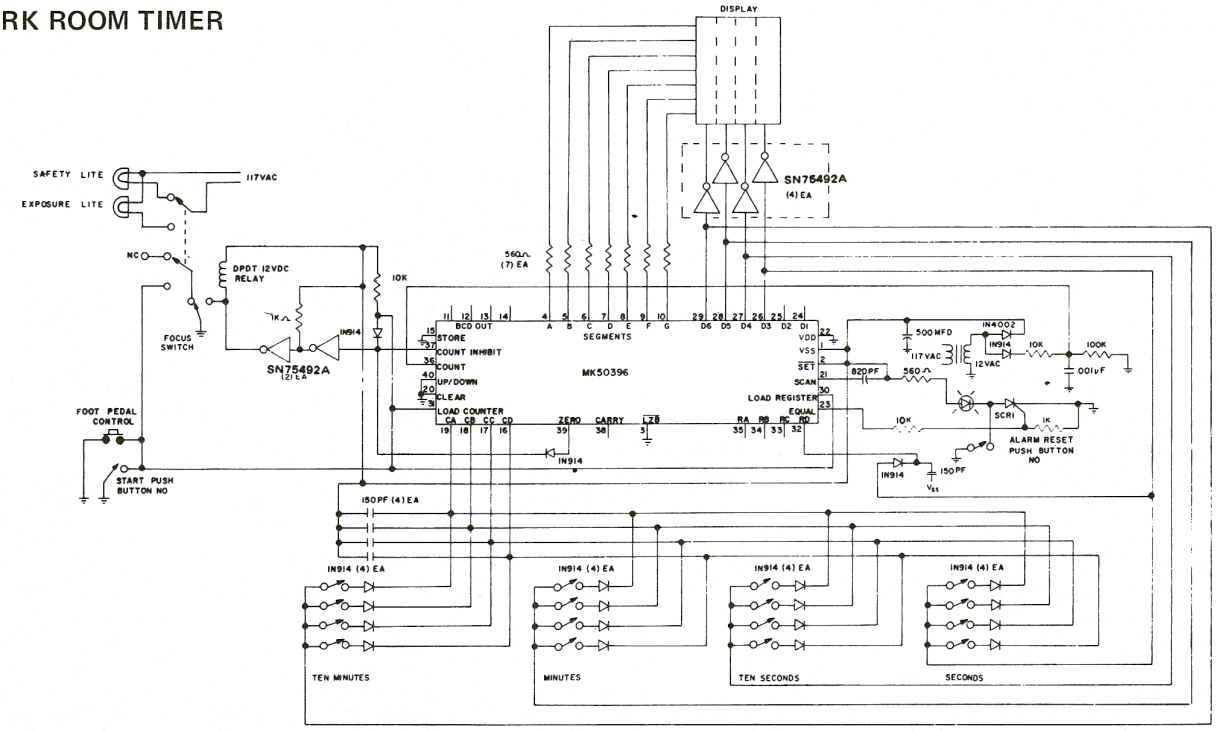
Resistor network R_1, R_2 lowers the 60Hz line voltage so that the positive peak does not exceed V_{SS}, otherwise damage to the circuit could occur. The counter input is driven directly from the 60Hz line frequency and the two LSD are not monitored by the display since they perform a divide function in this application. The LED display will present the time remaining since the counter is in the count down mode. If an illegal entry is made such as Binary 12, (1100), the display will show "E" in the digits containing an illegal entry. The counter will eventually "count out" the "E", but, of course, the time interval will not be useful. Also, it is possible to load illegal time such as 75 seconds. This illegal time will result in an error in timing.

SEQUENCE OF EVENTS

Assume a time interval of 1 minute, 45 seconds has been selected and programmed into the thumbwheel switches.

1. Pressing the start button completes loading 1 minute 45 seconds into the counter. The register is loaded with eight second prewarning signal. The relay is activated which allows the count down sequence to begin. (The display will immediately

DARK ROOM TIMER



show 1:44, because the ÷ 60 stage will be counting down the 60Hz input.) The relay also turns off the safety light and turns on the exposure light.

2. When eight seconds to time out occurs, the equal outputs goes to V_{SS} momentarily, turning on SCR_1 which lights a LED warning light that indicates the time interval is about over.

3. When the counter hits zero time, the zero output inhibits any further count input. The zero output also provides bias to turn on amplifier A_1 to turn off relay driver amplifier A_2, so the safety light will come on as the exposure light turns off.

4. The reset switch is used to turn off the SCR for the next time sequence.

DIGITAL TUNING INDICATOR

The MK 50395 is used to count and display frequencies of the FM frequency bands.

The frequency being sampled is buffered to TTL logic levels, then divided by 100 with a SN74S112 JK flip flop, a SN74S196 and a SN7490. Transistor Q_1 then shifts the TTL logic levels to MOS logic levels.

The CMOS RC time base oscillates at 1KHz and is then divided by two to produce the necessary 500Hz time base.

At the end of the count sample time, a store is generated to latch the data into the display. Also the CD 4013 which controls the load counter input of the MK 50395 is preset, allowing the proper values to be loaded into the MK 50395 counter.

The placement of the diodes which determine the value to be loaded in the MK 50395 counter is dependent on the frequency of the local oscillator and whether high side or low side injection is used in the receiver.

In a typical FM receiver with High side injection a dial setting of 88.7 MHz means the local oscillator output would be 99.4MHz. To offset the 10.7MHz (88.7 + 10.7) the counter would be preloaded to 999893 (000000 minus 107). This effectively subtracts the 10.7MHz thus displaying the dial frequency. After each sample time the MK 50395 counter is reloaded readying it for the next count cycle. For low side injection receivers the preset would be 107 (00000 plus 107). This effectively adds 10.7MHz to the count. The decimal point of Digit two may be wired to +V through a resistor to produce the decimal in the FM mode.

To calibrate the time base an oscilloscope or frequency counter may be used, however careful adjustment at the low and high end of the counter display would be sufficient.

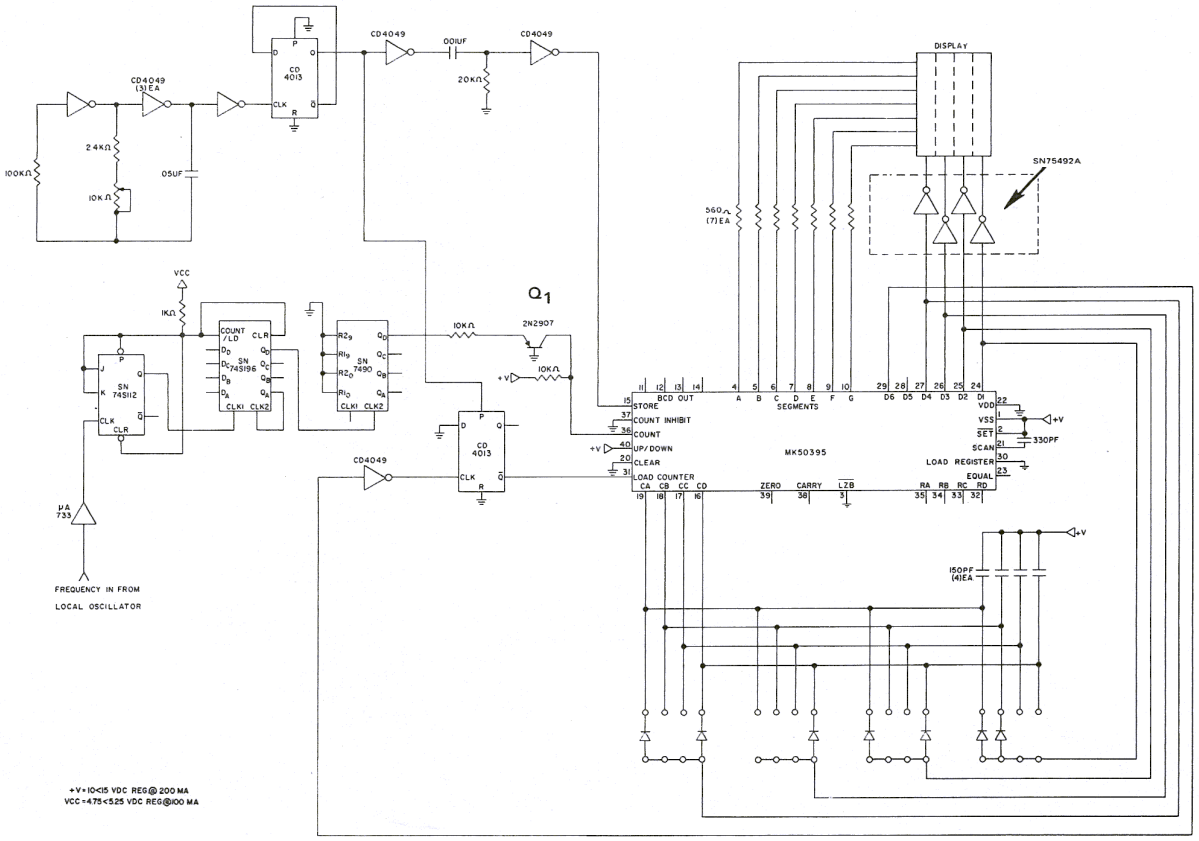
N PULSER

The N Pulser was designed to gate a specific number of pulses, its design uses a minimum of external circuitry.

The number of pulses to be gated are entered into the thumbwheel switches, this value is loaded into the BCD Register with the load register button. When the MK 50395 counter reaches this value the MK 50395 equal output goes high. The pulse string is then interrupted.

To control frequencies above 500KHz a suitable prescaler could be used at the MK 50395 count input, and compensated by the value entered into

DIGITAL TUNING INDICATOR

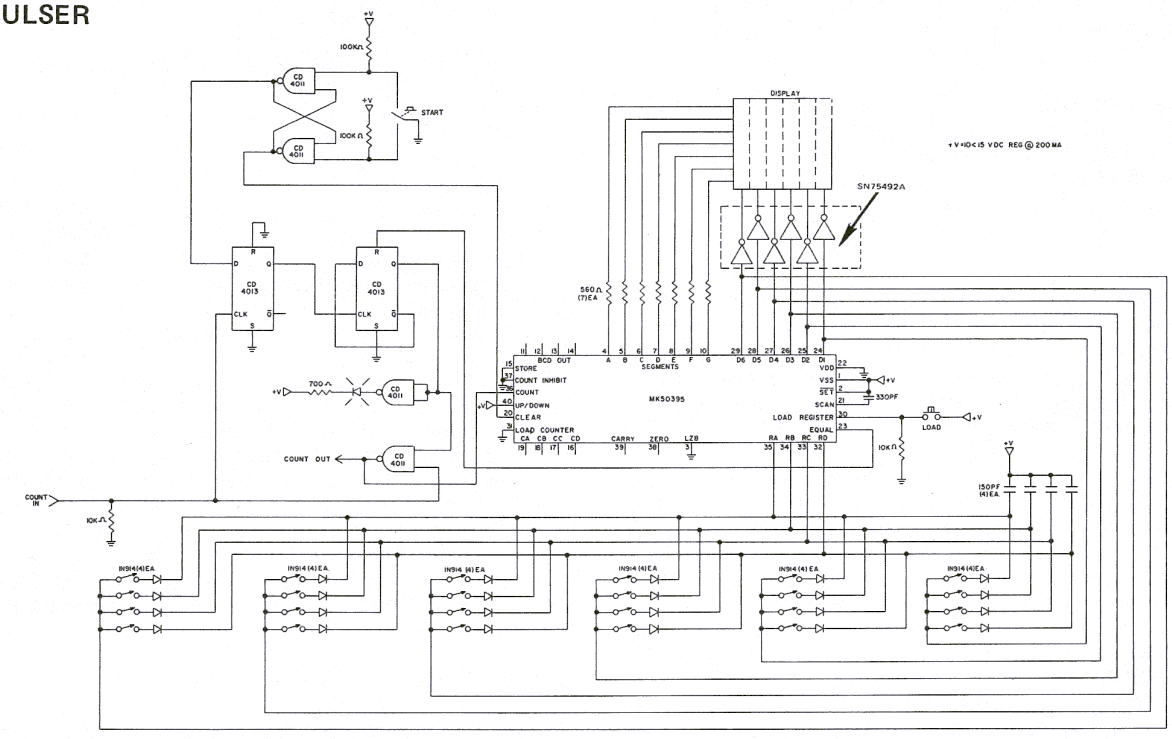


the MK 50395 BCD Register. Pulses in and pulses out must be CMOS compatible, or suitable level shifters would be required.

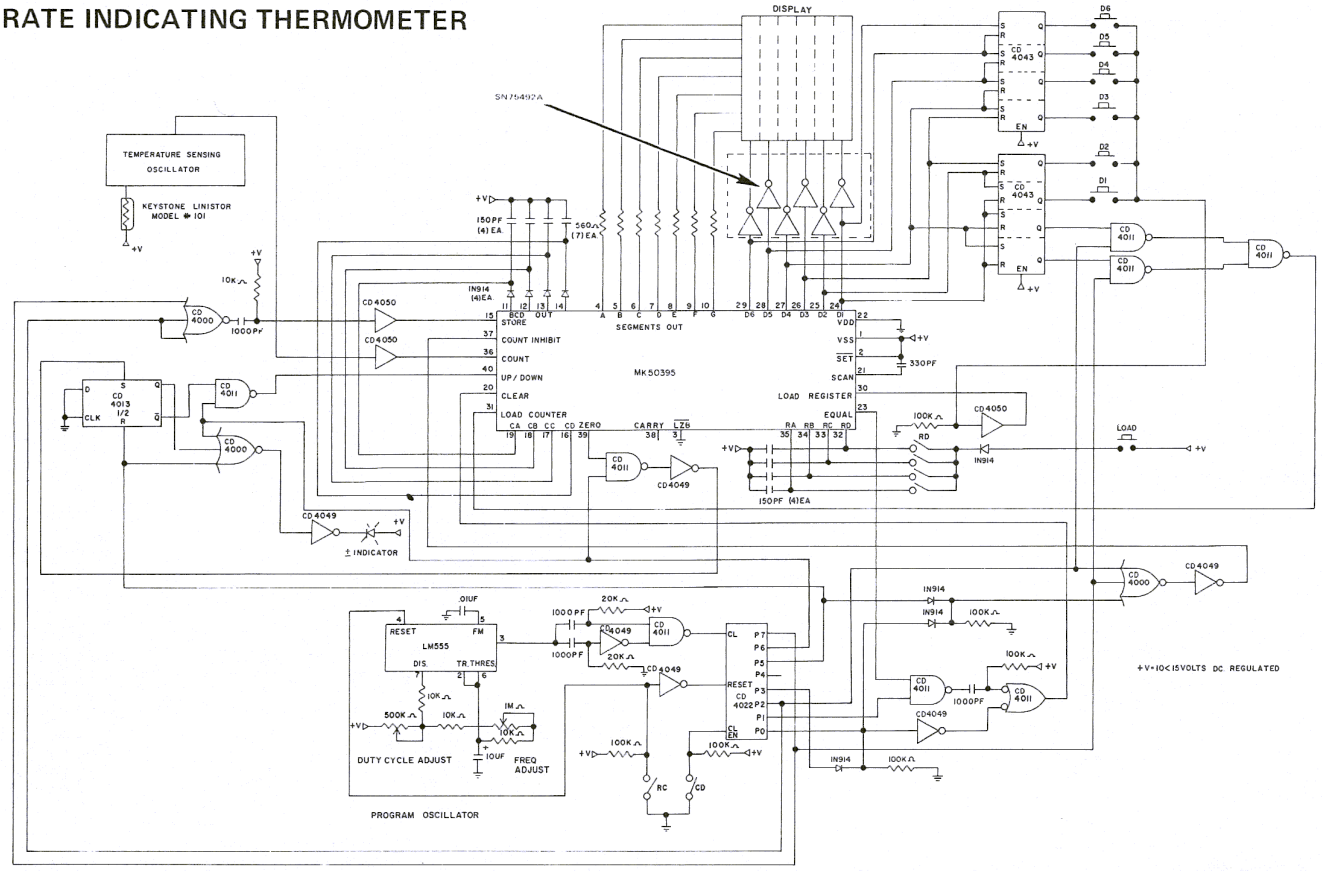
CONTINUOUS RATE INDICATING THERMOMETER

The MK 50395 displays the result of a program of eight periods (P0 through P7) under control of a

N PULSER



RATE INDICATING THERMOMETER



program counter (CD4022) which is driven by a program oscillator having independent controls for its frequency and its duty cycle. The output of the program oscillator is differentiated to supply a clock pulse to the program counter for each half cycle of the program oscillator. The program counter has eight decoded outputs which are used to time the program periods P0 through P7.

A voltage controlled oscillator in conjunction with a thermistor converts temperature into frequency. After the initial calibration it is desireable that the VC0 be stable to maintain accuracy of temperature change indications, which occur during P4 and P6 times.

During P0, the P0 output of the program counter is high and the counter of the MK 50395 is reset. During P1, the MK 50395 counter is incremented at the rate of the pulses furnished by the temperature sensitive oscillator. When the counter reaches equality with the register, the counter is reset to zero and continues counting until the end of P1.

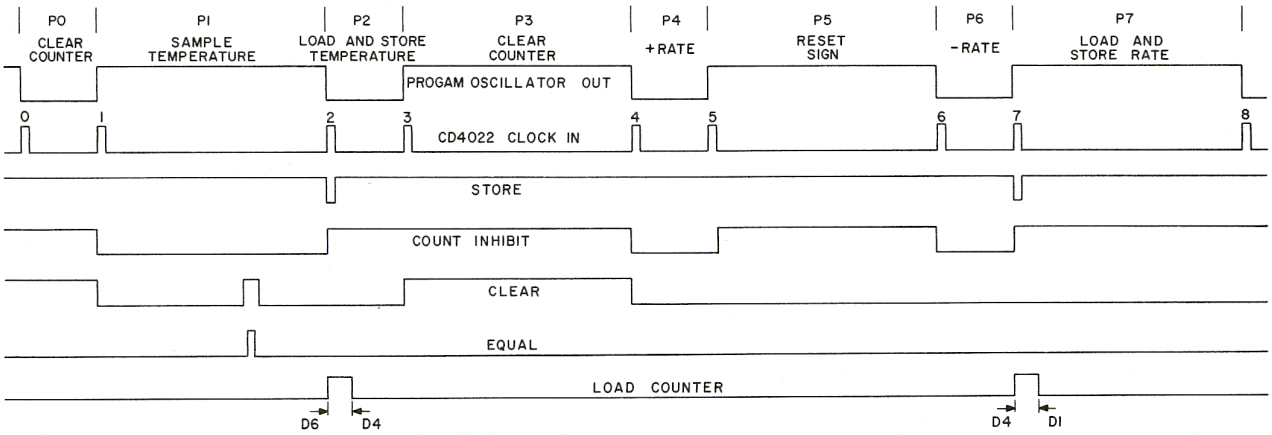
The length of the positive-going half-cycles of the program oscillator (during P1, P3, P5 and P7) is selected so that during the period P1, the number of cycles of the temperature sensitive oscillator (which are counted) changes with temperature at the rate of one thousand cycles per degree (either F. or C). For example, if the frequency of the temperature sensitive oscillator is 75KHz at 70°F and changes at the rate of 1000 Hz per degree change of temperature, the positive going half-cycle of the program oscillator is selected to equal 1.0 seconds, to vary the count of the 50395 counter (at the end of P1) by 1000 counts per degree. The register is preloaded with a quantity to calibrate temperature. In the above example, the register is preloaded with the quantity 80,000 so that the counter stands at 70,000 (150,000–80,000) at the end of P1 indicating a temperature of 70°F. Only the three most significant digits of the MK 50395 counter are displayed for temperature, and the display indicates the temperature in degrees, 70, 71, etc. The leading zero is blanked.

The three most significant digits of the counter indication are set into the MK 50395 latch during P2, but not before the three least significant digits of the counter are loaded to a quantity equal to that stored in the three least significant digits stored in the latch. These counter digits are set by bringing the load counter pin 31 high at the end of digit 4 thru digit 1 time and then bringing the store pin 15 low after the leading edge of D3, D2, and D1 with a delay. The four BCD output pins 11-14 are connected directly to the four counter inputs pins 16-19. In this way the three least significant digits are retained in the latch and the three most significant digits of the latch are set to the current temperature. The three least significant digits in the latch store the current rate of change of temperature which is calculated during subsequent periods of the program.

During P3, the MK 50395 counter is reset.

During P4, the MK 50395 counter is again ready to

THERMOMETER TIMING



count the pulses produced by the temperature sense oscillator for an entire period, during which the content of the register is ignored.

During P5, the sign flip-flop is reset, so that the MK 50395 counter, counts down during the following period. During P6, the MK 50395 is again ready to count up the temperature sensitive oscillator for one half cycle, and count down from the state arrived at at the end of P4. If the temperature has not changed in the interval between P4 and P6, the MK 50395 counter will stand at zero at the end of P6. If the temperature has decreased since P4, the counter will stand at some number which is proportional to the rate of change in temperature.

If the temperature has increased between P4 and P6, the MK 50395 counter is counted down to zero before the end of P6. When this occurs the sign flip-flop is set, and the level at pin 40 goes high, changing the mode of counting from down to up. At the end of P6, the MK 50395 counter stores a quantity which is proportional to the rate of change of temperature. If the sign flip-flop remains reset after P6, it provides a signal to the negative sign display associated with the rate display.

The durations of the periods of the negative going half cycle of the program oscillator are chosen so that the rate identifying contents of the MK 50395 counter are in units of degrees per hour. Since the change of temperature is less than 1000 per hour, only the lowest three bits of the counter contains significant information, with the three higher orders standing at zero. During P7, the current temperature data from the three highest digits of the latch are set into the counter by bringing the load counter pin 31 high from the leading edge of D1, thru D4. The contents of the counter are then stored in the latch by bringing pin 15 up, after a delay. The program counter is reset to zero at P0 and the entire program is repeated successively. Display of temperature and rate of change is continuous, with the negative sign blanked during P5 and P6.

The temperature calibration data is entered into the register by operation of several manual switches. The CD4043 latches allow the digits of the BCD Register to be loaded individually and not alter the data in other digits.

Switches CD and RC are provided for disabling the program counter and for resetting the program counter (and the program oscillator.)

To load the BCD register close the reset counter (CD) switch, select the desired BCD data with the register data switches, depress the desired digit switch, and the load data switch at the same time. After all digits have been properly loaded check operation to assure the proper data has been loaded.

The period of the positive-going half-cycle of the program oscillator is chosen to allow calibration of the temperature. The period of the negative-going half-cycle of the program oscillator (P0, P2, P4, and P6) is chosen independently of the positive-going half-cycle to allow calibration of the rate of change.

Where the period of the positive-going half-cycle is P (in seconds), the period of the negative-going half-cycle is chosen equal to $\frac{p2}{3.6\text{-}P}$ or the frequency of the program oscillator is chosen equal to $\frac{3.6\text{-}P}{3.6\ P}$

This allows calibration for both temperature and rate of change without any restriction on the temperature sensitive oscillator.

The timing diagram above indicates the relative contents of the MK 50395 counter during the eight program periods.

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