

# SC14046B

## Phase Locked Loop

The SC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA<sub>in</sub> and PCB<sub>in</sub>. Input PCA<sub>in</sub> can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1<sub>out</sub>, and maintains 90° phase shift at the center frequency between PCA<sub>in</sub> and PCB<sub>in</sub> signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, PC2<sub>out</sub> and LD, and maintains a 0° phase shift between PCA<sub>in</sub> and PCB<sub>in</sub> signals (duty cycle is immaterial). The linear VCO produces an output signal VCO<sub>out</sub> whose frequency is determined by the voltage of input VCO<sub>in</sub> and the capacitor and resistors connected to pins C1<sub>A</sub>, C1<sub>B</sub>, R1, and R2. The source-follower output SF<sub>out</sub> with an external resistor is used where the VCO<sub>in</sub> signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

### Features

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive OR Gate and is Duty Cycle Limited
- Phase Comparator 2 Switches on Rising Edges and is not Duty Cycle Limited
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub>	Input Voltage Range (All Inputs)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 1)	500	mW
T <sub>A</sub>	Operating Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating:

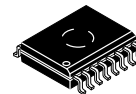
Plastic "DW" Packages: - 7.0 mW/°C From 65°C To 125°C



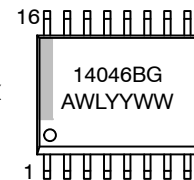
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM



SOIC-16  
DW SUFFIX  
CASE 751G



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

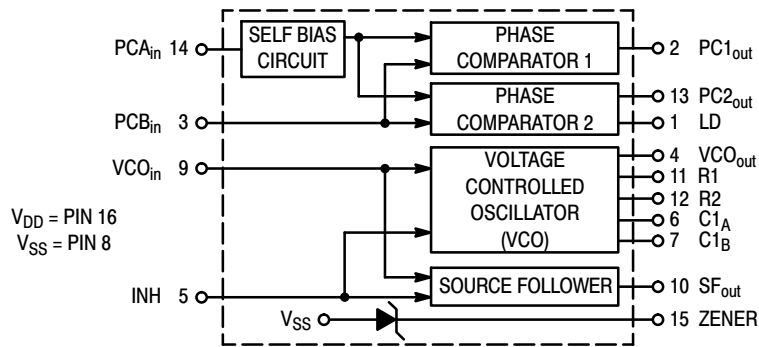
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

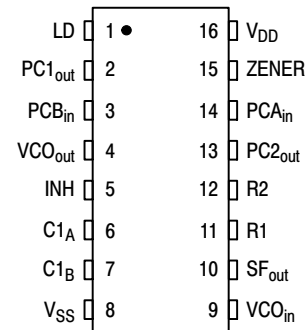
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# SC14046B

## BLOCK DIAGRAM



## PIN ASSIGNMENT



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55° C		25° C			125° C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
	"1" Level V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- - -	4.95 9.95 14.95	- - -	Vdc
Input Voltage (Note 2) (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
	"1" Level V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0 5.0 10 15	-1.2 -0.25 -0.62 -1.8	- - - -	-1.0 -0.2 -0.5 -1.5	-1.7 -0.36 -0.9 -3.5	- - - -	-0.7 -0.14 -0.35 -1.1	- - - -	mAdc
	Sink I <sub>OL</sub>	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8	- - -	0.36 0.9 2.4	- - -	mAdc
Input Current	I <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	µAdc
Input Capacitance	C <sub>in</sub>	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package) Inh = PCA <sub>in</sub> = V <sub>DD</sub> , Zener = VCO <sub>in</sub> = 0 V, PCB <sub>in</sub> = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 µA	I <sub>DD</sub>	5.0 10 15	- - -	5.0 10 20	- - -	0.005 0.010 0.015	5.0 10 20	- - -	150 300 600	µAdc
Total Supply Current (Note 3) (Inh = "0", f <sub>o</sub> = 10 kHz, C <sub>L</sub> = 50 pF, R1 = 1.0 MΩ, R2 = ∞, R <sub>SF</sub> = ∞, and 50% Duty Cycle)	I <sub>T</sub>	5.0 10 15	I <sub>T</sub> = (1.46 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (2.91 µA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (4.37 µA/kHz) f + I <sub>DD</sub>							mAdc

2. Noise immunity specified for worst-case input combination.  
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc  
2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc  
2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

3. To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left( \frac{V_{COin} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2} \right)^{3/4} + 1.6 \times \left( \frac{V_{COin} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left( \frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu\text{A}, C_L \text{ in pF, } V_{COin}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and } R1, R2, R_{SF} \text{ in } M\Omega, C_L \text{ on } V_{COout}$$

# SC14046B

## ELECTRICAL CHARACTERISTICS (Note 4) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	- - -	180 90 65	350 150 110	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	- - -	100 50 37	175 75 55	ns

## PHASE COMPARATORS 1 and 2

Input Resistance – PCA <sub>in</sub>	$R_{in}$	5.0	1.0	2.0	-	M $\Omega$
		10	0.2	0.4	-	
		15	0.1	0.2	-	
- PCB <sub>in</sub>	$R_{in}$	15	150	1500	-	M $\Omega$
Minimum Input Se-sitivity AC Coupled — PCA <sub>in</sub> C series = 1000 pF, f = 50 kHz	$V_{in}$	5.0	-	200	300	mV p-p
		10	-	400	600	
		15	-	700	1050	
DC Coupled – PCA <sub>in</sub> , PCB <sub>in</sub>	-	5 to 15	See Noise Immunity			

## VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency (VCO <sub>in</sub> = V <sub>DD</sub> , C1 = 50 pF R1 = 5.0 k $\Omega$ , and R2 = $\infty$ )	$f_{max}$	5.0	0.5	0.7	-	MHz
		10	1.0	1.4	-	
		15	1.4	1.9	-	
Test Frequency (Note 5) (VCO <sub>in</sub> = V <sub>DD</sub> , C1 = 3.3 nF R1 = 1.69 k $\Omega$ , and R2 = 8.25 k $\Omega$ )	-	15	300	-	460	kHz
Temperature – Frequency Stability (R2 = $\infty$ )	-	5.0	-	0.12	-	%/ $^\circ\text{C}$
		10	-	0.04	-	
		15	-	0.015	-	
Linearity (R2 = $\infty$ ) (VCO <sub>in</sub> = 2.5 V $\pm$ 0.3 V, R1 > 10 k $\Omega$ ) (VCO <sub>in</sub> = 5.0 V $\pm$ 2.5 V, R1 > 400 k $\Omega$ ) (VCO <sub>in</sub> = 7.5 V $\pm$ 5.0 V, R1 $\geq$ 1000 k $\Omega$ )	-	5.0	-	1.0	-	%
		10	-	1.0	-	
		15	-	1.0	-	
Output Duty Cycle	-	5 to 15	-	50	-	%
Input Resistance – VCO <sub>in</sub>	$R_{in}$	15	150	1500	-	M $\Omega$

## SOURCE-FOLLOWER

Offset Voltage (VCO <sub>in</sub> minus SF <sub>out</sub> , R <sub>SF</sub> > 500 k $\Omega$ )	-	5.0	-	1.65	2.2	V
		10	-	1.65	2.2	
		15	-	1.65	2.2	
Linearity (VCO <sub>in</sub> = 2.5 V $\pm$ 0.3 V, R <sub>SF</sub> > 50 k $\Omega$ ) (VCO <sub>in</sub> = 5.0 V $\pm$ 2.5 V, R <sub>SF</sub> > 50 k $\Omega$ ) (VCO <sub>in</sub> = 7.5 V $\pm$ 5.0 V, R <sub>SF</sub> > 50 k $\Omega$ )	-	5.0	-	0.1	-	%
		10	-	0.6	-	
		15	-	0.8	-	

## ZENER DIODE

Zener Voltage ( $I_Z = 50$ $\mu\text{A}$ )	$V_Z$	-	6.7	7.0	7.3	V
Dynamic Resistance ( $I_Z = 1.0$ mA)	$R_Z$	-	-	100	-	$\Omega$

4. The formula given is for the typical characteristics only.

5. This is a special test parameter as requested by the customer. Component values are not within recommended range. Component values are valid for this parameter only.

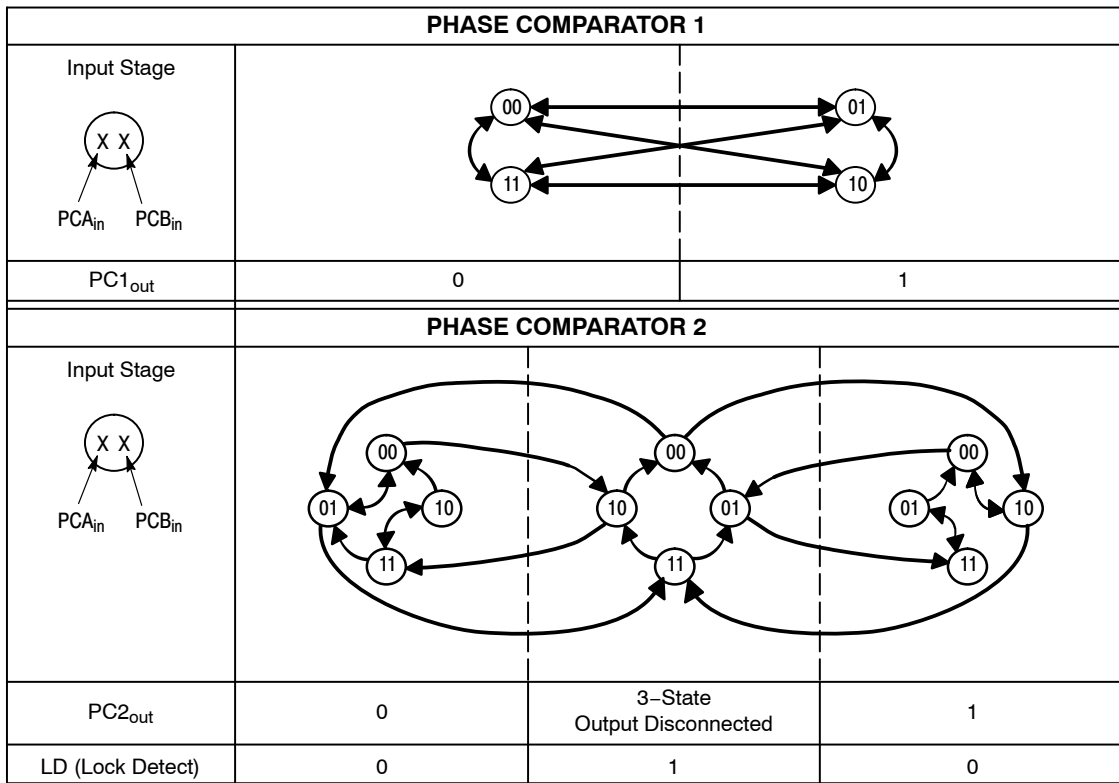
# SC14046B

## ORDERING INFORMATION

Device	Package	Shipping†
SC14046BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
SC14046BDWR2G		1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# SC14046B



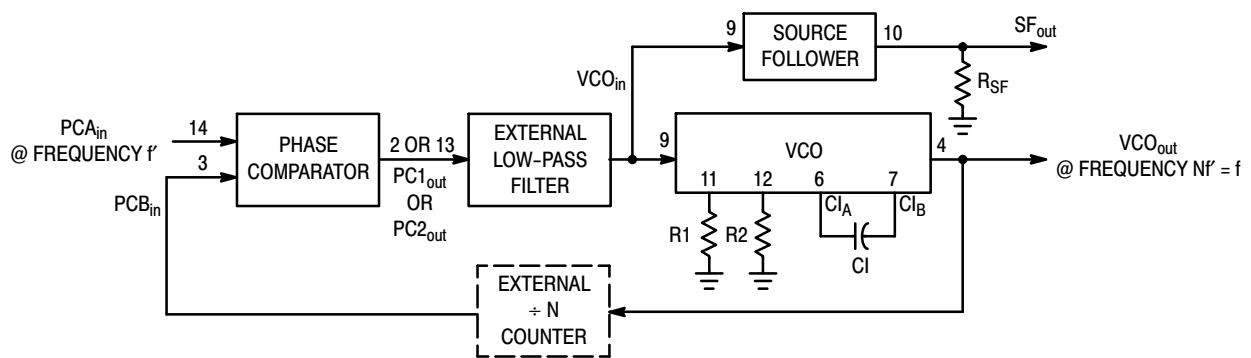
Refer to Waveforms in Figure 3.

**Figure 1. Phase Comparators State Diagrams**

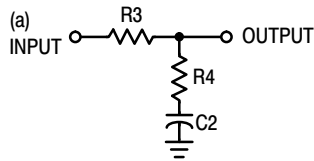
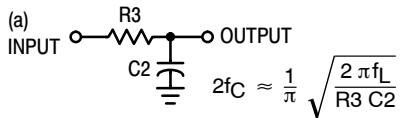
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA <sub>in</sub> .	VCO in PLL system adjusts to center frequency (f <sub>0</sub> ).	VCO in PLL system adjusts to minimum frequency (f <sub>min</sub> ).
Phase angle between PCA <sub>in</sub> and PCB <sub>in</sub> .	90° at center frequency (f <sub>0</sub> ), approaching 0° and 180° at ends of lock range (2f <sub>L</sub> )	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f <sub>L</sub> ).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2f <sub>L</sub> = full VCO frequency range = f <sub>max</sub> - f <sub>min</sub> .	
Capture frequency range (2f <sub>C</sub> ).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f <sub>C</sub> ≤ f <sub>L</sub>	f <sub>C</sub> = f <sub>L</sub>
Center frequency (f <sub>0</sub> ).	The frequency of VCO <sub>out</sub> , when VCO <sub>in</sub> = 1/2 V <sub>DD</sub>	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (V_{CO} \text{ input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (V_{CO} \text{ input} = V_{DD})$ <p>Where: 10K ≤ R<sub>1</sub> ≤ 1 M                      10K ≤ R<sub>2</sub> ≤ 1 M                      100pF ≤ C<sub>1</sub> ≤ .01 μF</p>	
Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.		

**Figure 2. Design Information**

# SC14046B



## Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} \approx \frac{N}{2\pi \Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} \approx R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

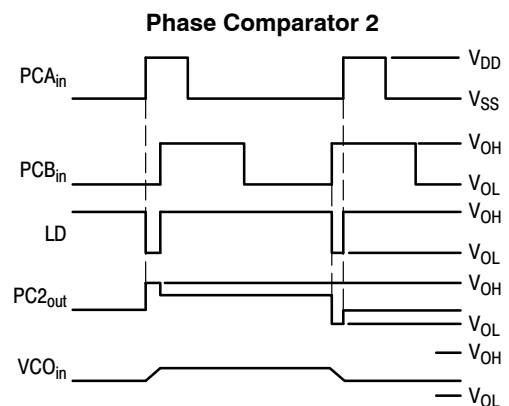
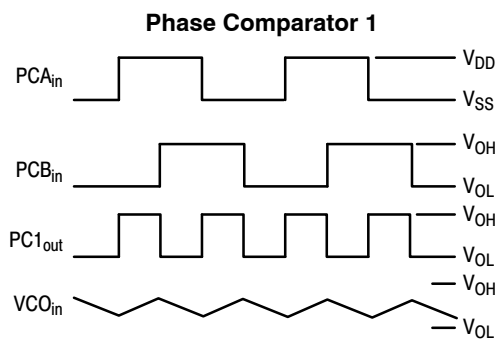
NOTE: Sometimes R3 is split into two series resistors each R3 ÷ 2. A capacitor C<sub>C</sub> is then placed from the midpoint to ground. The value for C<sub>C</sub> should be such that the corner frequency of this network does not significantly affect Ω<sub>n</sub>. In Figure B, the ratio of R3 to R4 sets the damping, R4 ≈ (0.1)(R3) for optimum results.

## LOW-PASS FILTER

Definitions: N = Total division ratio in feedback loop  
 $K\phi = V_{DD}/\pi$  for Phase Comparator 1  
 $K\phi = V_{DD}/4\pi$  for Phase Comparator 2  
 $KVCO = \frac{2\pi \Delta f VCO}{V_{DD} \Delta V}$   
 for a typical design  $\Omega_n \approx \frac{2\pi f_r}{10}$  (at phase detector input)  
 $\zeta \approx 0.707$

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi KVCO}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K\phi KVCO}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi KVCO}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K\phi KVCO})$
$F(s) = \frac{1}{R_3 C_2 S + 1}$	$F(s) = \frac{R_3 C_2 S + 1}{S(R_3 C_2 + R_4 C_2) + 1}$

## Waveforms



Note: for further information, see:

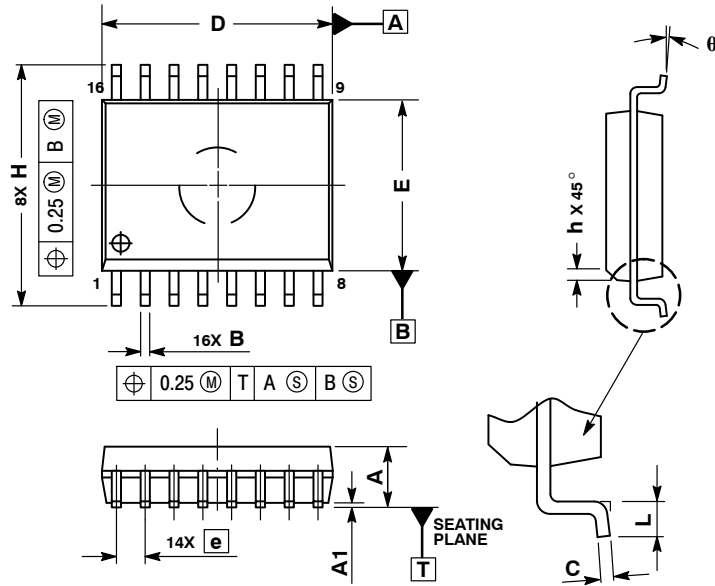
- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przepelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

**Figure 3. General Phase-Locked Loop Connections and Waveforms**

# SC14046B

## PACKAGE DIMENSIONS

SOIC-16 WB  
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751G-03  
ISSUE C



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
q	0 °	7 °

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

SC14046B/D