SC1452
Dual 150mA LDO Regulator with Programmable Reset

POWER MANAGEMENT

Description

The SC1452 is a state of the art device intended to provide maximum performance and flexibility in battery operated systems. It has been designed specifically to fully support a single Li-Ion battery and its external charger voltages.

The SC1452 contains two independently enabled, ultra low dropout voltage regulators (ULDOs). It operates from an input voltage range of 2.25V to 6.5V, and a wide variety of output voltage options are available which are designed to provide an initial tolerance of ±1% and ±2% over temperature.

Each regulator has an associated active-low reset signal which is asserted when the voltage output declines below the preset threshold. Once the output recovers, the reset continues to be asserted (delayed) for a predetermined time, 50ms for reset A and 150ms for reset B. In the case of regulator B, the delay time may be reduced by the addition of an external capacitor.

The SC1452 has a bypass pin to enable the user to capacitively decouple the bandgap reference for very low output noise (down to 50µVrms).

The devices utilize CMOS technology to achieve very low operating currents (typically 130uA with both outputs supplying 150mA). The dropout voltage is typically 155mV at 150mA, helping to prolong battery life. In addition, the devices are guaranteed to provide 400mA of peak current for applications which require high initial inrush current. They have been designed to be used with low ESR ceramic capacitors to save cost and PCB area.
The SC1452 comes in the low profile 10-lead MSOP package.

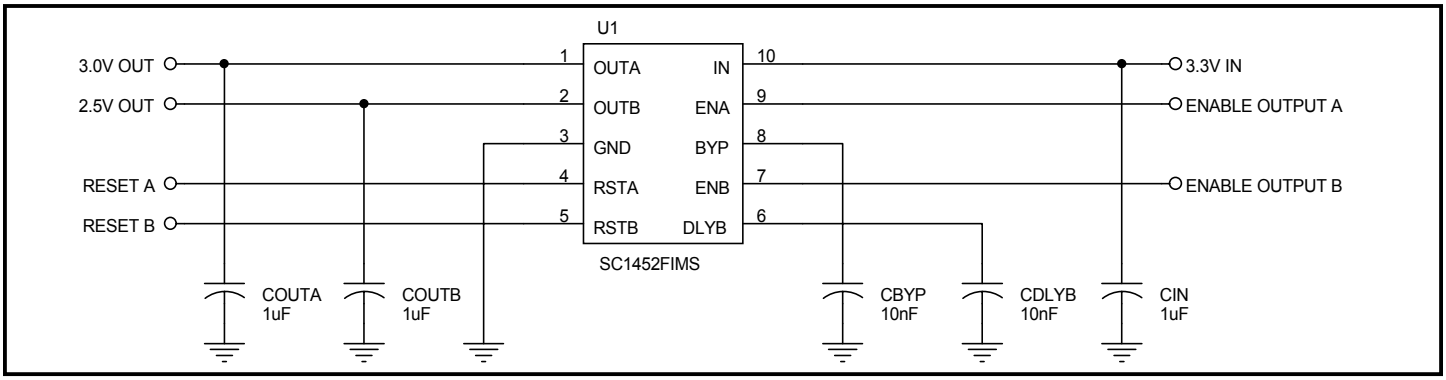
Features

- Up to 150mA per regulator output
- Low quiescent current (130µA typical with both outputs at 150mA)
- Low dropout voltage
- Wide selection of output voltages
- Stable operation with ceramic caps
- Tight load and line regulation
- Current and thermal limiting
- Reverse input polarity protection
- <1µA off-mode current
- Logic controlled enable
- Active low resets valid for V_{IN} down to 0V
- Programmable reset
- Full industrial temperature range
- 10-Pin MSOP package. Also available in Lead-free, fully WEEE and RoHS compliant

Applications

- Cellular telephones
- Palmtop/Laptop computers
- Battery-powered equipment
- Bar code scanners
- SMPS post regulator/dc to dc modules
- High efficiency linear power supplies
- DSP supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-5 to +7	V
Enable Input Voltage	V_{EN}	-5 to $+V_{IN}$	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-60 to +150	°C
Thermal Impedance Junction to Ambient	θ_{JA}	113	°C/W
Thermal Impedance Junction to Case	θ_{JC}	42	°C/W
ESD Rating (Human Body Model)	ESD	2	kV

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IN} = V_{OUT} + 1V, I_{OUTA} = I_{OUTB} = 1mA, C_{IN} = C_{OUT} = 1.0 µF, V_{ENA} = V_{ENB} = V_{IN}.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IN						
Input Supply Voltage	V_{IN}		**2.25**		**6.5**	V
Quiescent Current	I_Q	V_{ENA} = 0V, V_{ENB} = V_{IN}, I_{OUTB} = 150mA or		110	150	µA
		V_{ENB} = 0V, V_{ENA} = V_{IN}, I_{OUTA} = 150mA			**200**	
		V_{ENA} = V_{ENB} = V_{IN}, I_{OUTA} = I_{OUTB} = 150mA		130	200	µA
					250	
		V_{IN} = 6.5V, V_{ENA} = V_{ENB} = 0V (OFF)		0.2	1.0	µA
					1.5	
OUTA, OUTB						
Output Voltage(1)	V_{OUT}	I_{OUT} = 1mA	-1%	V_{OUT}	+1%	V
		0mA ≤ I_{OUT} ≤ 150mA, V_{OUT} +1V ≤V_{IN} ≤ 5.5V	**-2%**		**+2%**	
Line Regulation(1)	$REG_{(LINE)}$	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 1mA		2.5	10	mV
					12	
Load Regulation(1)	$REG_{(LOAD)}$	0.1mA ≤ I_{OUT} ≤150mA		-5	-20	mV
					-30	

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{IN} = V_{OUT} + 1V, I_{OUTA} = I_{OUTB} = 1mA, C_{IN} = C_{OUT} = 1.0 µF, V_{ENA} = V_{ENB} = V_{IN}.
Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Dropout Voltage[1][2]	V_D	I_{OUT} = 1mA		1		mV
		I_{OUT} = 50mA		52	70	mV
					90	
		I_{OUT} = 150mA		155	210	mV
					270	
Current Limit	I_{LIM}		**400**			mA
Ripple Rejection	PSRR	f = 120Hz, C_{BYP} = 10nF		59		dB
Output Voltage Noise	e_n	f = 10Hz to 100kHz, I_{OUT} = 50mA, C_{BYP} = 10nF, C_{OUT} = 2.2µF, 1.8V output		27		μV_{RMS}
		f = 10Hz to 100kHz, I_{OUT} = 50mA, C_{BYP} = 10nF, C_{OUT} = 2.2µF, 3.3V output		55		
BYP						
Start-up Rise Time	t_r	C_{BYP} = 10nF		1.25		ms
ENA, ENB						
Enable Input Threshold	V_{IH}		**1.6**			V
	V_{IL}				**0.4**	
Enable Input Bias Current[3]	$I_{ENA/B}$	0V ≤ $V_{ENA/B}$ ≤ V_{IN}	**-0.5**		**+0.5**	µA
RSTA, RSTB						
Reset Threshold	$V_{TH(RST)}$	V_{OUT} falling	**88**	90	**92**	$\%V_{OUT}$
		V_{OUT} rising	**90**	92	**94**	
Reset A Delay	t_{RSTA}		**30**	50	**70**	ms
Reset B Delay	t_{RSTB}	V_{DLYB}= 0V	**90**	150	**210**	ms
		C_{DLYB}= 10nF		4		
Reset A, B Output Voltage [4]	V_{OH}	I_{SOURCE}= 0.5mA	**90**	98		$\%V_{OUT}$
	V_{OL}	I_{SINK}= 1.2mA		0.02	**0.10**	V
DLYB						
Delay Voltage Threshold	$V_{TH(DLYB)}$			1.250		V
Delay Source Current	I_{DLYB}	V_{OUTB} < V_{TH}	**2.1**	3.0	**3.9**	µA

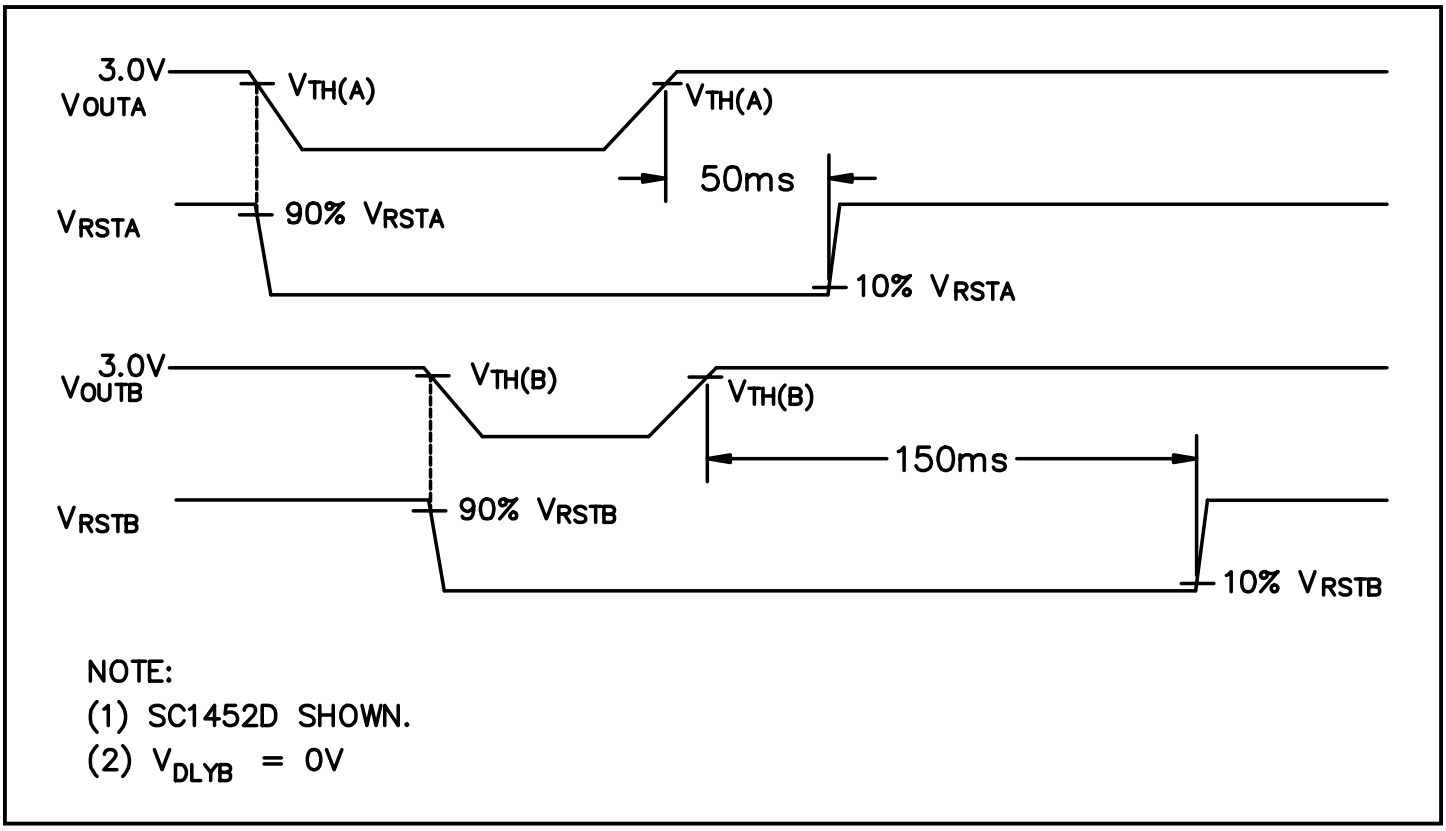
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{IN} = V_{OUT} + 1V, I_{OUTA} = I_{OUTB} = 1mA, C_{IN} = C_{OUT} = 1.0 µF, V_{ENA} = V_{ENB} = V_{IN}.
Values in **bold** apply over full operating temperature range.

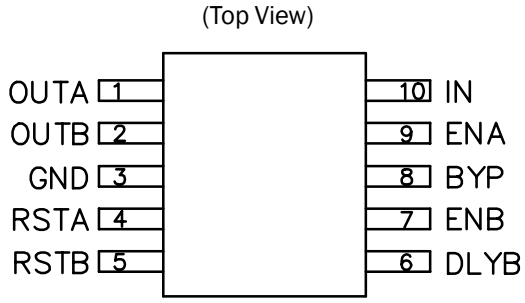
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Over Temperature Protection						
High Trip Level	T_{HI}			150		°C
Hysteresis	T_{HYST}			20		°C

NOTES:
(1) Low duty cycle pulse testing with Kelvin connections required.
(2) Defined as the input to output differential at which the output drops 100mV below the value measured at a differential of 1V. Not measurable on 1.5V and 1.8V outputs due to minimum V_{IN} constraints.
(3) Guaranteed by design.
(4) V_{OHA} will be a percentage of V_{OUTA}, and V_{OHB} will be a percentage of V_{OUTB}.

Timing Diagrams



Pin Configuration



Ordering Information

Part Numbers	Package
SC1452XIMSTR (1)(2)	MSOP-10
SC1452XIMSTRT (1)(2)(3)	

Notes:
(1) Where X denotes voltage options - see Voltage Options table.
(2) Only available in tape and reel packaging. A reel contains 2500 devices.
(3) Lead-free product. This product is fully WEEE and RoHS compliant.

Voltage Options

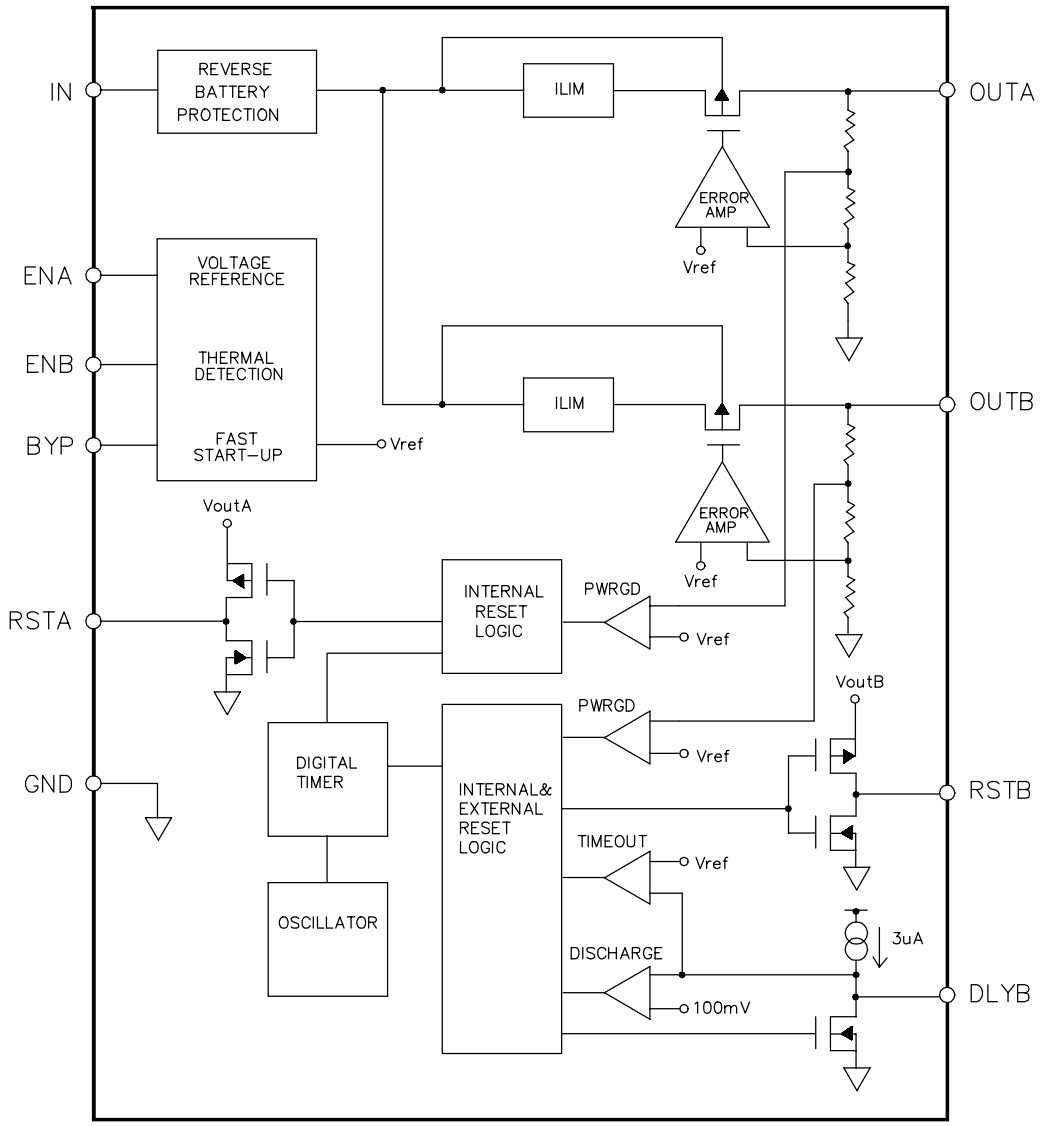
Replace X in the part number (SC1452XIMS) by the letter shown below for the corresponding voltage option:

X	V_{OUTA} (V)	V_{OUTB} (V)
A	1.8	1.8
B	2.5	2.5
C	2.8	2.8
D	3.0	3.0
E	3.3	3.3
F	3.0	2.5
G	3.0	1.8
H	3.0	2.8
J	3.3	2.5
K	3.3	2.8

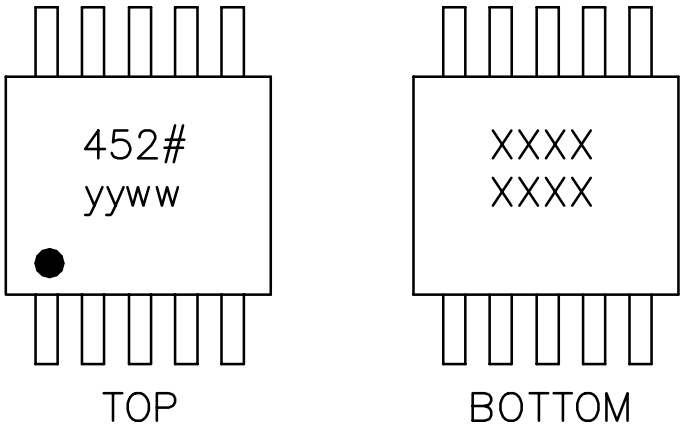
Pin Descriptions

Pin #	Pin Name	Pin Function
1	OUTA	Regulator A output.
2	OUTB	Regulator B output.
3	GND	Ground pin.
4	RSTA	Power on reset for output A. Active low when OUTA is below the reset threshold. RSTA goes high 50ms (typical) after OUTA rises above the reset threshold.
5	RSTB	Power on reset for output B. Active low when OUTB is below the reset threshold. RSTB goes high 150ms (typical - can be adjusted using C_{DLYB}) after OUTB rises above the reset threshold.
6	DLYB	Programmable delay for RESETB. Delay time can be set by connecting a capacitor, $C_{DLYB,}$ between this pin and ground. Ground this pin if using the default delay time.
7	ENB	Active high enable pin for output B. CMOS compatible input. Connect to IN if not being used.
8	BYP	Bypass pin for bandgap reference. Connect a 10nF capacitor, C_{BYP}, between this pin and ground for low noise operation.
9	ENA	Active high enable pin for output A. CMOS compatible input. Connect to IN if not being used.
10	IN	Input pin for both regulators.

Block Diagram



Marking Information



# = Voltage options (Example: 452F)
yyww = Datecode (Example: 0008)
XXXX = Lot Number (Example: E01102)

Applications Information

Theory Of Operation

The SC1452 is intended for applications where very low dropout voltage, low supply current and low output noise are critical. Furthermore, the SC1452, by combining two ultra low dropout (ULDO) regulators, along with enable controls and power-on resets (which function is usually served by external devices), provides a very space efficient solution for multiple supply requirements.

The SC1452 contains two ULDOs, both of which are supplied by one input supply, between IN and GND. Each ULDO has its own active high enable pin (ENA/ENB). Pulling this pin low causes that specific ULDO to enter a very low power shutdown state.

Each ULDO also has its own power on reset pin (RSTA/RSTB), which asserts low whenever the output voltage is below the reset threshold for that output. Each reset remains asserted low until a specific delay time after the output rises back above the reset threshold. For output A, this delay time is typically 50ms. Output B has a programmable reset delay. If DLYB is grounded, the reset delay will be controlled by an internal timer to 150ms. If a capacitor is connected between DLYB and GND, a constant current, I_{DLYB}, charges this capacitor until the delay threshold, $V_{TH(DLYB)}$, is reached, or the internal timer times out. See "Adjusting RSTB Delay Time". One advantage of on-board resets is that they remain asserted low all the way down to V_{IN} = 0V, whereas external devices may require pull-down resistors.

A bypass pin (BYP) is provided to decouple the bandgap reference to reduce output noise (on both outputs) and also to improve power supply rejection.

The SC1452 contains an internal bandgap reference which is fed into the inverting input of two error amplifiers, one for each output. The output voltage of each regulator is divided down internally using a resistor divider and compared to the bandgap voltage. The error amplifier drives the gate of a low $R_{DS(ON)}$ P-channel MOSFET pass device.

Each regulator has its own current limit circuitry to ensure that the output current will not damage the device during output short, overload or start-up. The current limit is guaranteed to be greater than 400mA to allow fast charging of the output capacitor and high initial currents for DSP initialization.

The SC1452 has a fast start-up circuit to speed up the initial charging time of the bypass capacitor to enable the output voltage to come up quicker.

The SC1452 includes thermal shutdown circuitry to turn off the device if T_J exceeds 150°C (typical), with the device remaining off until T_J drops by 20°C (typical). Reverse battery protection circuitry ensures that the device cannot be damaged if the input supply is accidentally reversed, limiting the reverse current to less than 1.5mA.

Adjusting RSTB Delay Time

The power on reset delay for regulator B, t_{RSTB}, can be *reduced* externally by connecting a capacitor to the delay time set pin DLYB. If DLYB is connected to ground, the internally controlled delay time of 150ms (typ.) will apply.

Referring to the block diagram, as the output of regulator B (V_{OUTB}) rises and reaches the reset threshold voltage (92% $V_{OUTB(NOM)}$), two things happen:
1) the internal 150ms timer starts;
2) the 3µA current source turns on, charging C_{DLYB} (if connected).

If DLYB is connected to ground, RSTB goes high 150ms after V_{OUTB} crosses the threshold voltage. If a capacitor is connected between DLYB and ground, the voltage at DLYB can be described by the following equation:

$$V_{DLYB} = \frac{3 \bullet 10^{-6} \bullet t}{C_{DLYB}}$$

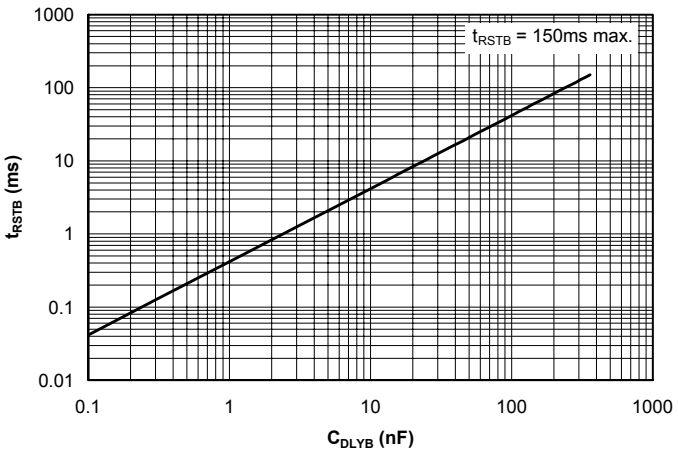
An internal comparator compares this voltage to a 1.25V reference, and triggers the reset high once this voltage is reached. The delay time can be calculated by rearranging the above equation, solving for t:

$$t_{RSTB} = \frac{C_{DLYB} \bullet 1.25}{3 \bullet 10^{-6}} = 416{,}667 \bullet C_{DLYB}$$

Note that the *maximum* delay time is 150ms, as RSTB goes high when either the internal timer or externally set timer times out, so if t_{RSTB} is set externally for 200ms, the reset delay will still be 150ms. Thus for a 150ms delay, DLYB should be grounded, and for a delay time

Applications Information (Cont.)

less than 150ms, C_{DLYB} can be calculated using the equation above, or read from the chart below.



Component Selection

Output capacitor - Semtech recommends a minimum capacitance of 1µF at the output with an equivalent series resistance (ESR) of < 1Ω over temperature. The SC1452 has been designed to be used with ceramic capacitors, but does not have to be used with ceramic capacitors, allowing the designer a choice. Increasing the bulk capacitance will further reduce output noise and improve the overall transient response.

Input capacitor - Semtech recommends the use of a 1µF ceramic capacitor at the input. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving overall load transient response.

Bypass capacitor - Semtech recommends the use of a 10nF ceramic capacitor to bypass the bandgap reference. Increasing this capacitor to 100nF will further improve power supply rejection. C_{BYP} may be omitted if low noise operation is not required.

Thermal Considerations

The worst-case power dissipation for this part is given by:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUTA(MIN)}) \bullet I_{OUTA(MAX)} + (V_{IN(MAX)} - V_{OUTB(MIN)}) \bullet I_{OUTB(MAX)} + V_{IN(MAX)} \bullet I_{Q(MAX)} \quad (1)$$

For all practical purposes, equation (1) can be reduced to the following expression:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUTA(MIN)}) \bullet I_{OUTA(MAX)} + (V_{IN(MAX)} - V_{OUTB(MIN)}) \bullet I_{OUTB(MAX)} \quad (2)$$

Looking at a typical application:
$V_{IN(MAX)}$ = 4.2V
V_{OUTA} = 3V - 2% (worst case) = 2.94V
V_{OUTB} = 3.3V - 2% (worst case) = 3.234V
$I_{OUTA} = I_{OUTB}$ = 150mA
T_A = 85°C
Inserting these values into equation (2) above gives us:

$$P_{D(MAX)} = (4.2 - 2.94) \bullet 0.15 + (4.2 - 3.234) \bullet 0.15 = 0.189 + 0.145 = 0.334W$$

Using this figure, we can calculate the maximum thermal impedance allowable to maintain $T_J \leq 125°C$:

$$\theta_{JA(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(125 - 85)}{0.334} = 120°C/W$$

With the standard MSOP-10 Land Pattern shown at the end of this datasheet, and minimum trace widths, the thermal impedance junction to ambient for SC1452 is 113°C/W. Thus no additional heatsinking is required for the above conditions. The junction temperature can be further reduced by using larger trace widths and connecting pcb copper area to the GND pin (pin 3), which connects directly to the device substrate. Lower junction temperatures improve overall output voltage accuracy.

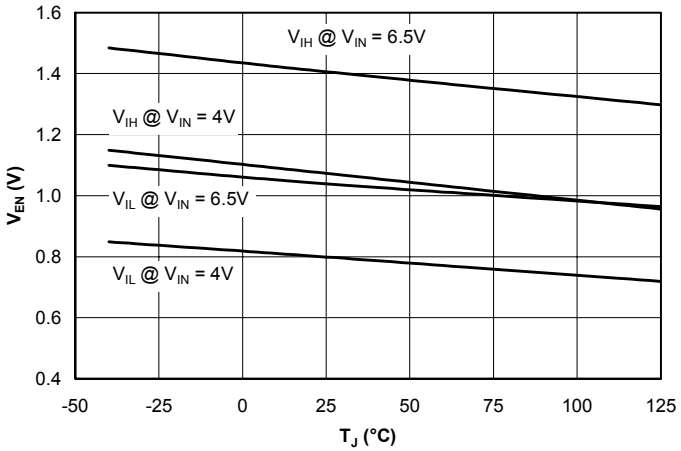
Layout Considerations

While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation.
1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.
2) Place the input, output and bypass capacitors close to the device for optimal transient response and device behaviour.

Applications Information (Cont.)

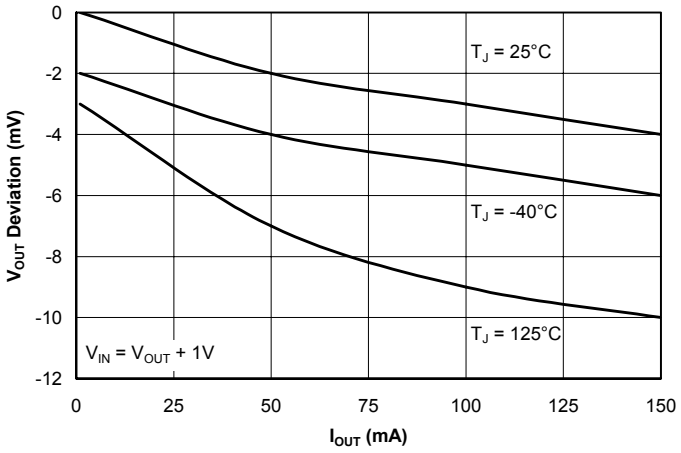
3) Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground.

Enable Input Voltage vs. Junction Temperature vs. Input Voltage

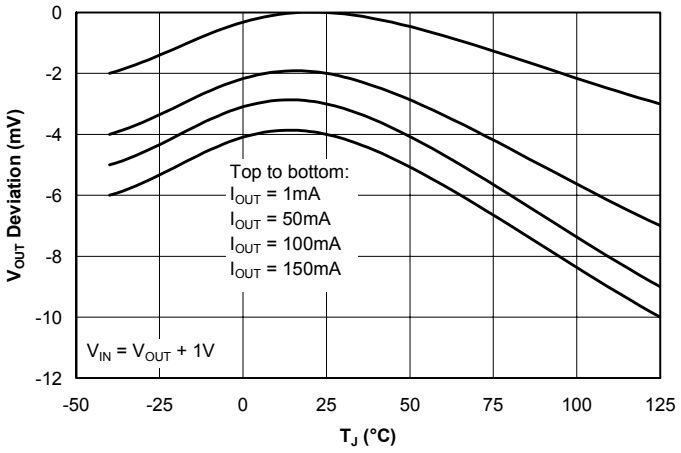


Typical Characteristics

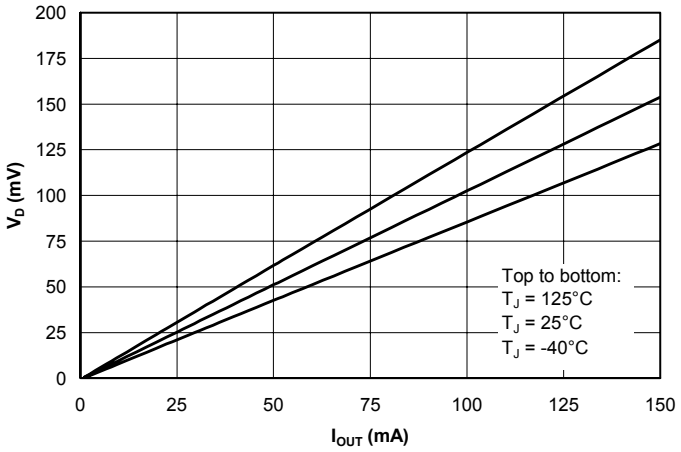
Output Voltage vs. Output Current vs. Junction Temperature



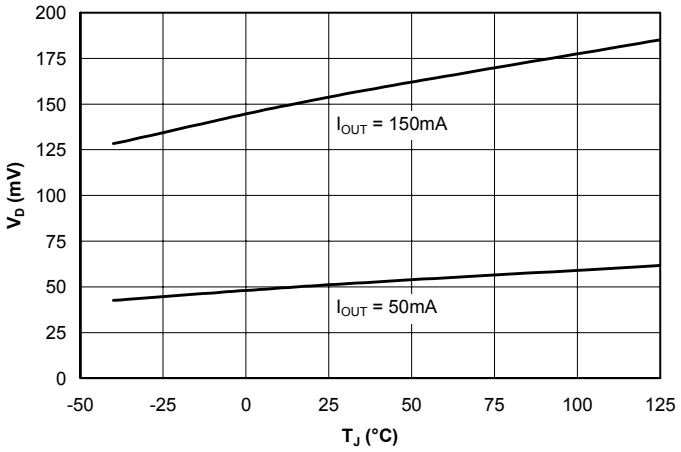
Output Voltage vs. Junction Temperature vs. Output Current



Dropout Voltage vs. Output Current vs. Junction Temperature

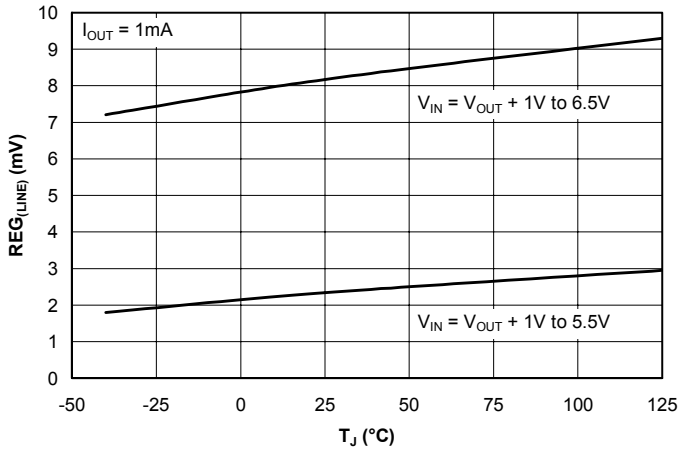


Dropout Voltage vs. Junction Temperature vs. Output Current

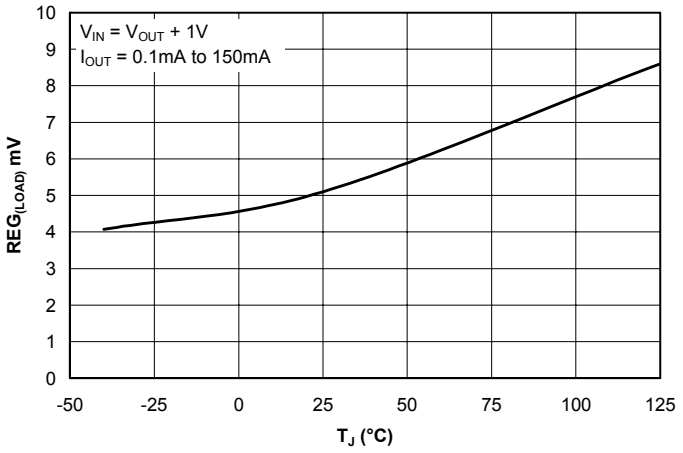


Typical Characteristics (Cont.)

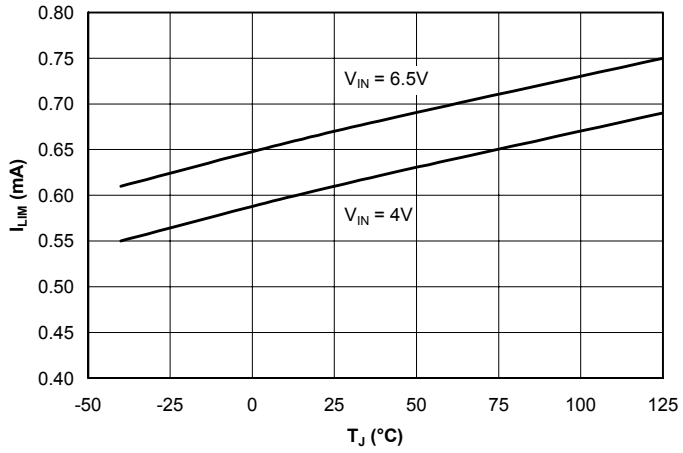
Line Regulation vs. Junction Temperature



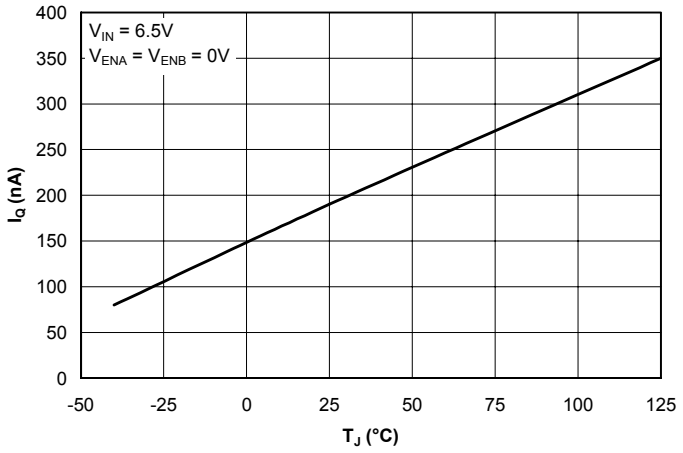
Load Regulation vs. Junction Temperature



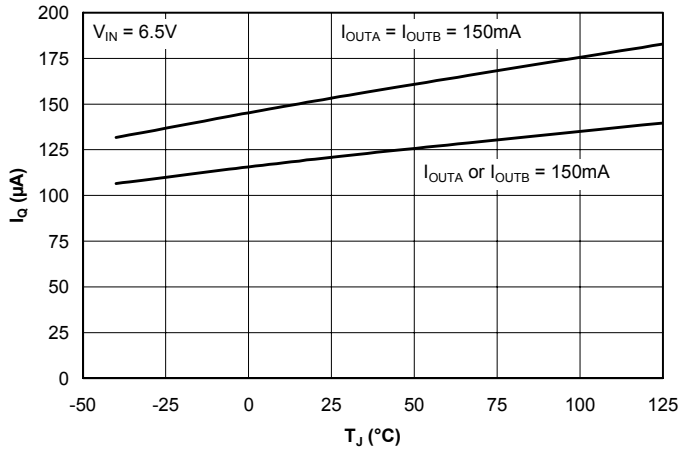
Current Limit vs. Junction Temperature vs. Input Voltage



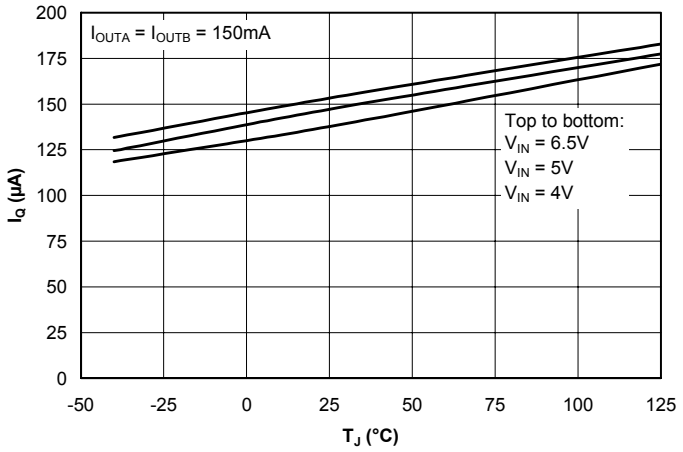
Off-State Quiescent Current vs. Junction Temperature



Quiescent Current vs. Junction Temperature vs. Output Current

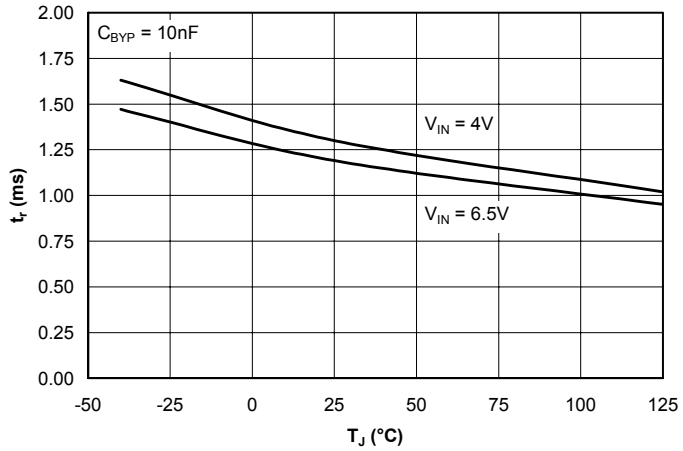


Quiescent Current vs. Junction Temperature vs. Input Voltage

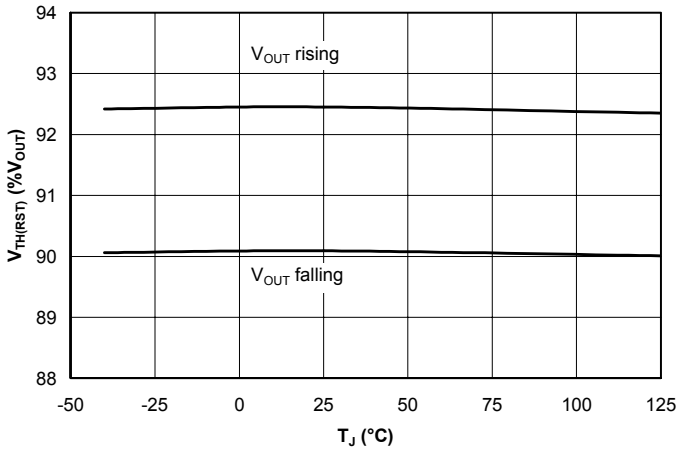


Typical Characteristics (Cont.)

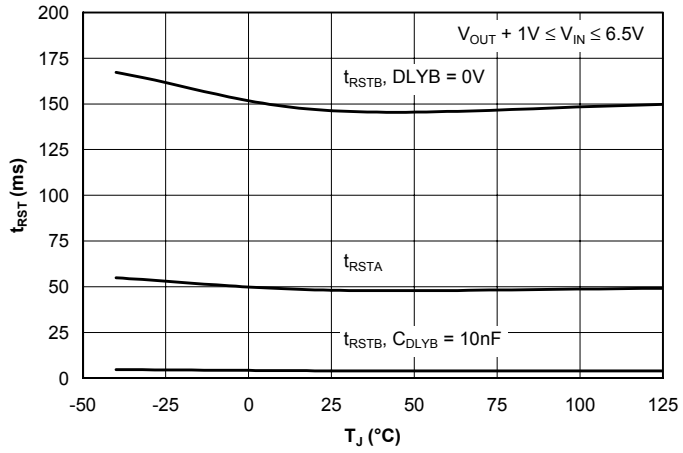
Bypass Start-up Rise Time vs. Junction Temperature vs. Input Voltage



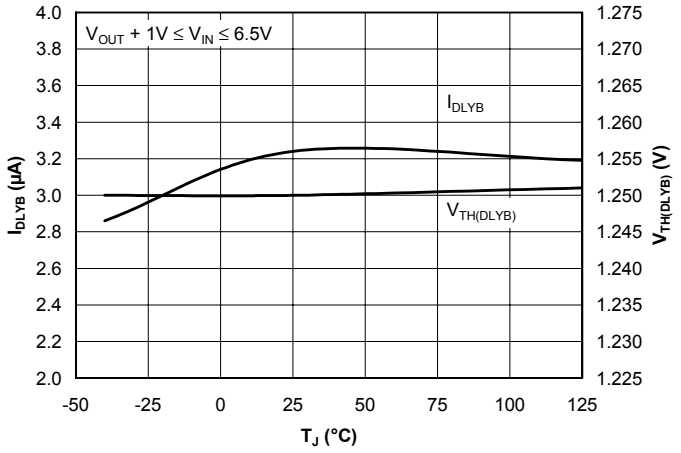
Reset Threshold Voltage vs. Junction Temperature



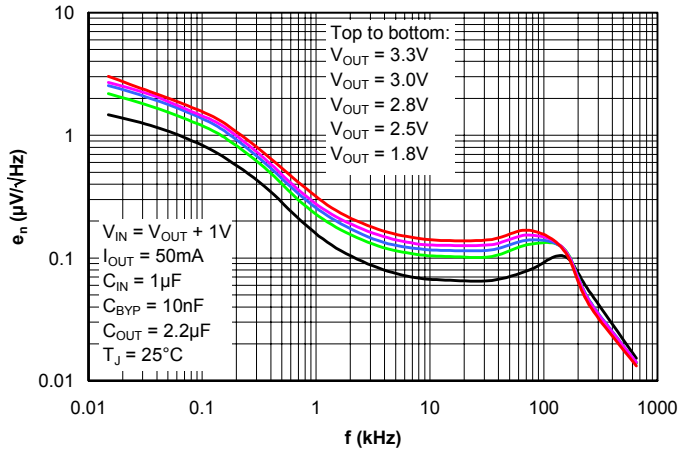
Reset Delay Times vs. Junction Temperature



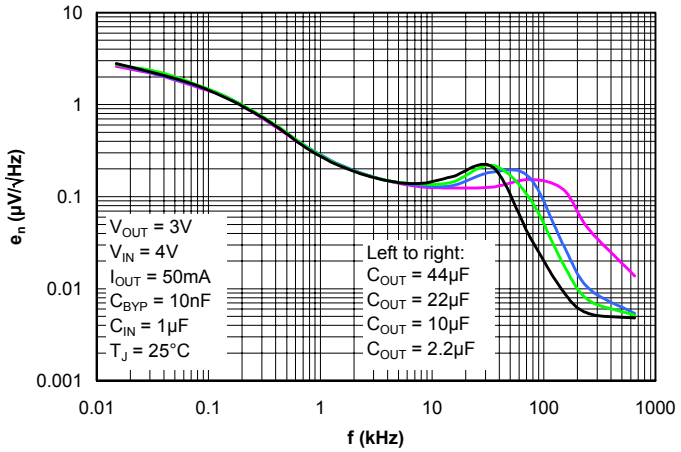
Delay Source Current and Voltage Threshold vs. Junction Temperature



Output Spectral Noise Density vs. Frequency vs. Output Voltage

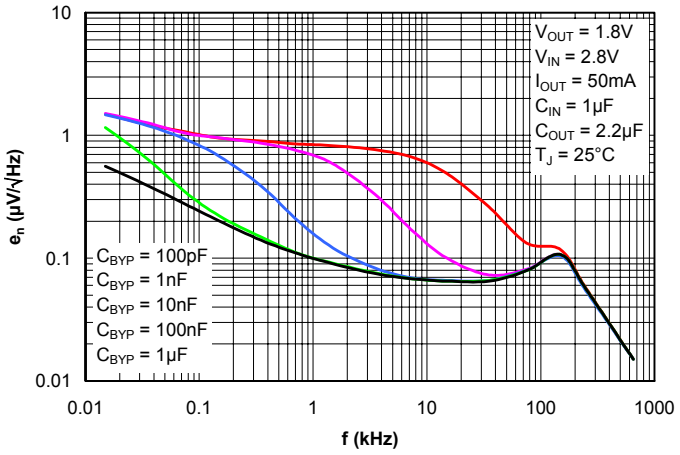


Output Spectral Noise Density vs. Frequency vs. Output Capacitance

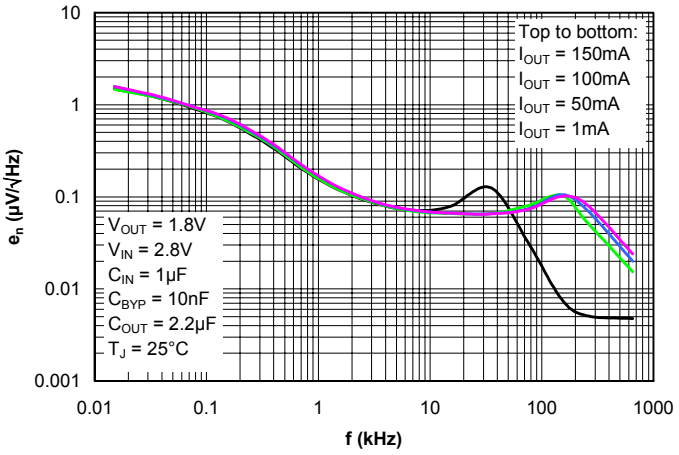


Typical Characteristics (Cont.)

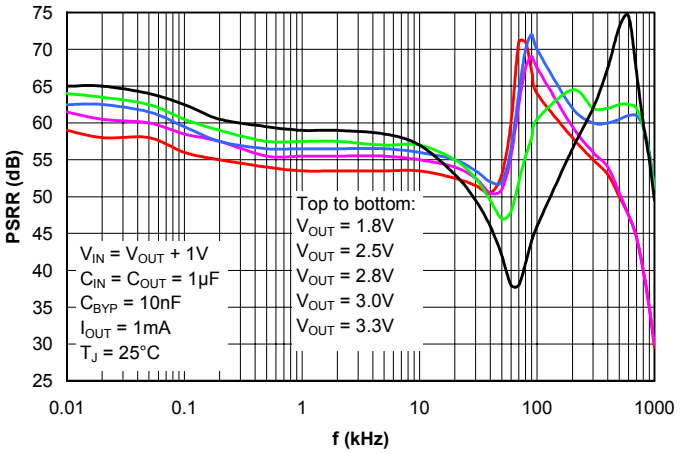
Output Spectral Noise Density vs. Frequency vs. Bypass Capacitance



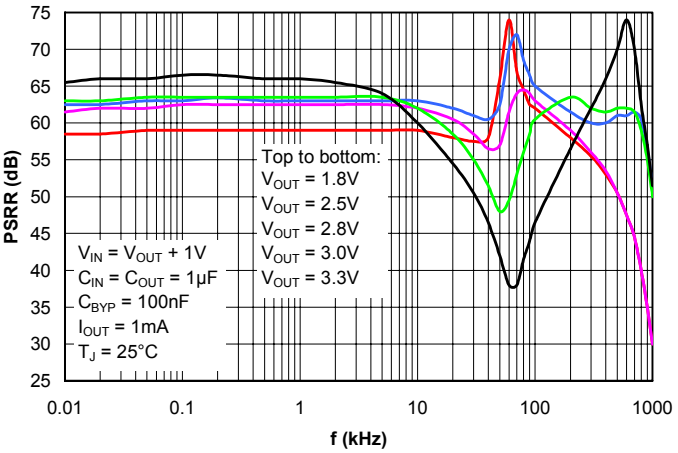
Output Spectral Noise Density vs. Frequency vs. Output Current



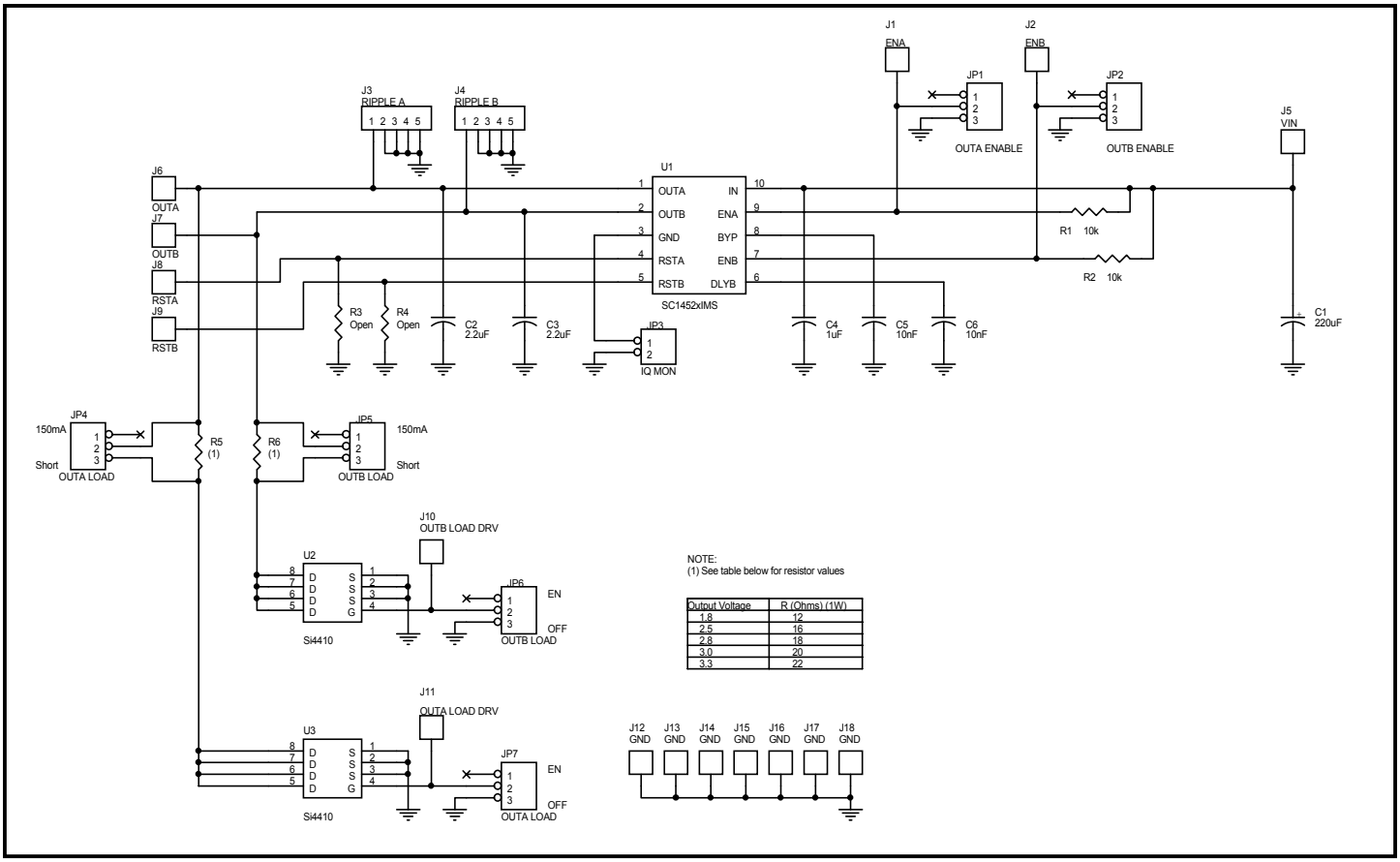
PSRR vs. Frequency vs. Output Voltage (C_{BYP} = 10nF)



PSRR vs. Frequency vs. Output Voltage (C_{BYP} = 100nF)

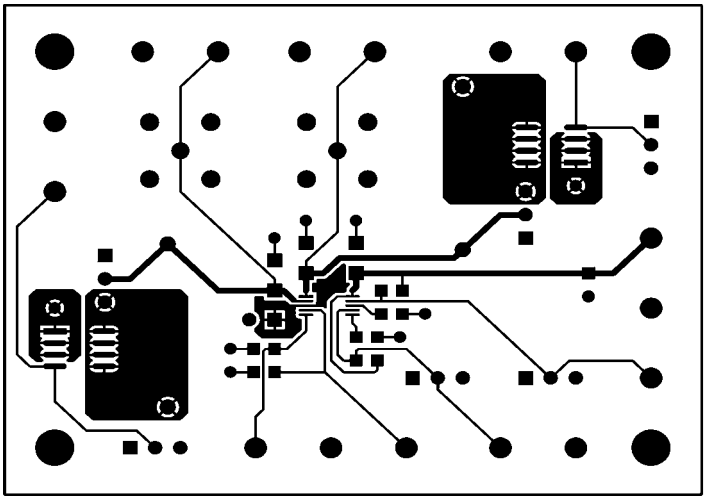


Evaluation Board Schematic

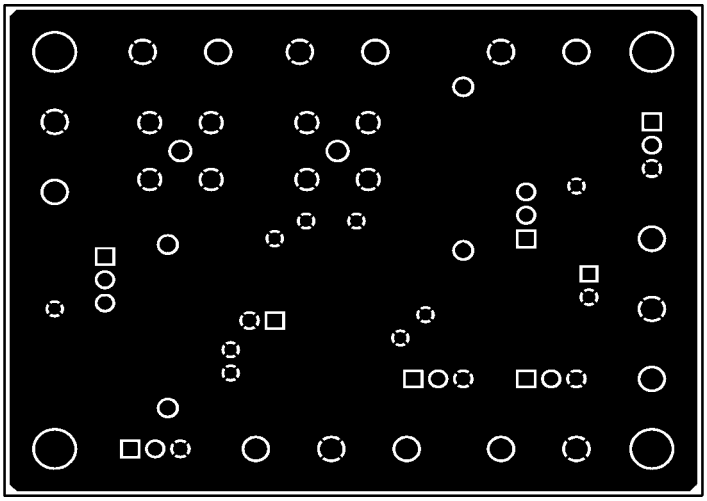


Output Voltage	R (Ohms) (1W)
1.8	12
2.5	16
2.8	18
3.0	20
3.3	22

Evaluation Board Gerber Plots

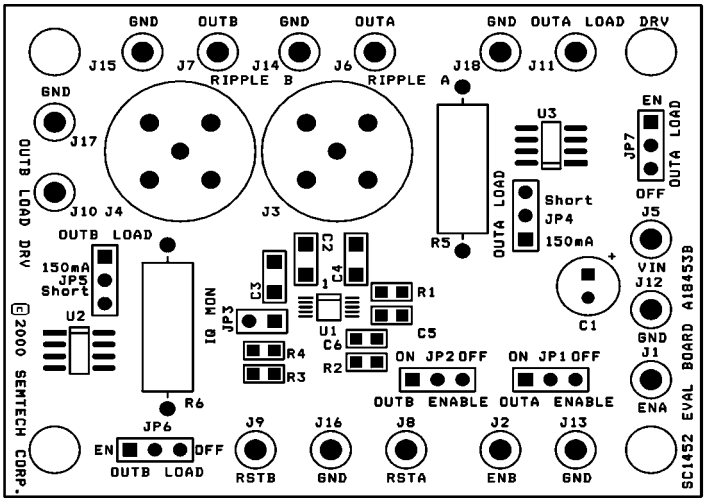


Top Copper



Bottom Copper

Evaluation Board Gerber Plots (Cont.)

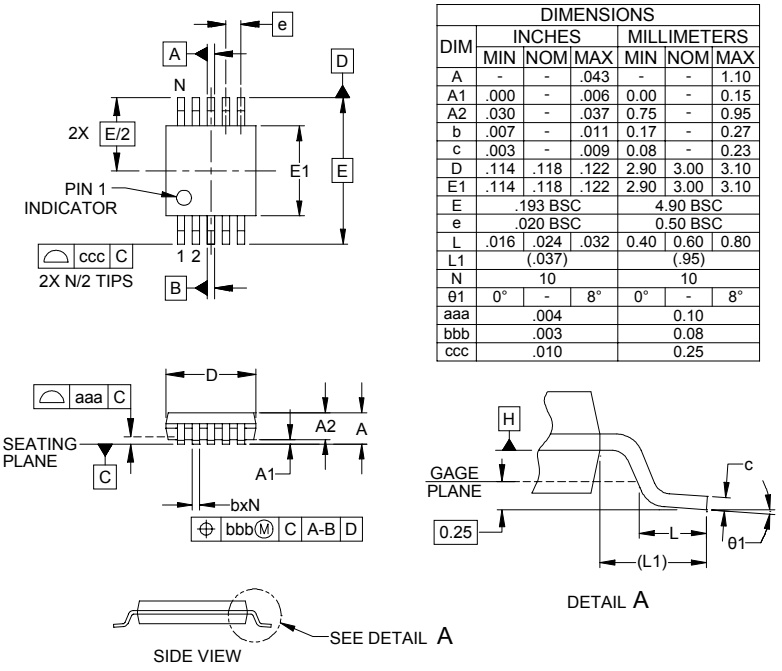


Top Silk Screen

Evaluation Board Bill of Materials

Quantity	Reference	Part/Description	Vendor	Notes
1	C1	220µF, 10V	Various	
2	C2, C3	2.2µF ceramic	Murata	GRM42-6X7R225K16
1	C4	1µF ceramic	Murata	GRM42-6X7R105K25
2	C5, C6	10nF ceramic	Various	
2	J1, J2	Test pin	Various	White
2	J3, J4	BNC socket	Various	V_{OUT} ripple monitor
3	J5 - J7	Test pin	Various	Red
2	J8, J9	Test pin	Various	Yellow
2	J10, J11	Test pin	Various	Orange
7	J12 - J18	Test pin	Various	Black
6	JP1, JP2, JP4 - JP7	Header, 3 pin	Various	
1	JP3	Header, 2 pin	Various	
2	R1, R2	10kΩ, 1/10W	Various	
2	R3, R4	Not placed		
2	R5, R6	See schematic	Various	1W
1	U1	**SC1452xIMS**	Semtech	
2	U2, U3	Si4410	Vishay	

Outline Drawing - MSOP-10

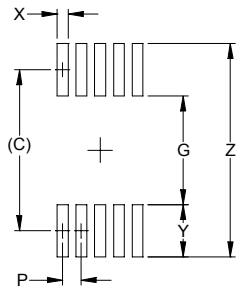


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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