TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

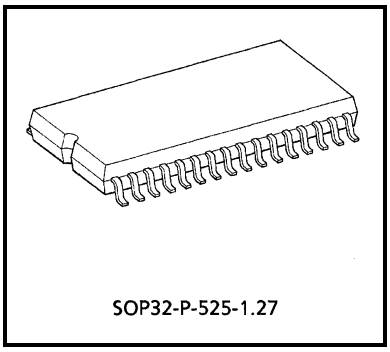
TMPN3120FE5MG

Neuron® Chip for Distributed Intelligent Control Networks (LONWORKS®)

The TMPN3120FE5MG features extra single-chip memory in the form of a 3 Kbyte EEPROM, a 4 Kbyte SRAM, and a 16 Kbyte ROM.

Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes. These nodes may then be easily integrated into highly reliable distributed intelligent control networks.

The typical functions for this chip are described below.



SOP32-P-525-1.27

Weight: 1.1 g (typ.)

Features

- Main features of the 20 MHz Neuron Chip
  (compared with the TMPN3120E1M)
  - Increased communication speed
    The maximum transmission speed has been increased twofold:
    1.25 Mbps → 2.5 Mbps (This value applies to Single-Ended Mode only.)
  - Shortened response time
    The amount of time required from I/O input to I/O output has been greatly reduced.
    Maximum speed 7 ms → 3 to 4 ms
  - Increased I/O object speed
    The execution time for all objects has been halved.
    Example) Serial I/O 9600 bps
    Parallel I/O 1.2 µs/byte

- I/O functions
  - Eleven programmable I/O pins
  - Two programmable 16-bit timers and counters built in
  - More than thirty different types of I/O functions to handle a wide range of input and output
  - ROM firmware image containing preprogrammed I/O drivers, greatly simplifying application programs
- Network functions
  - High-impedance communication port
  - Two CPUs for communication protocol processing built in
    The communications and application CPUs execute in parallel.
  - Equipped with a built-in LonTalk protocol supporting all seven levels of the ISO OSI reference model
  - The ROM firmware image contains a complete network operating system, greatly simplifying application programs.
  - Built-in twisted-pair wire transceiver with improved common-mode and drive current capabilities
  - Equipped with communications modes and communication speeds to support various types of external transceivers
  - Communication port transceiver modes and logical addresses are stored within the EEPROM.
    Can be amended via the network.
- Other functions
  - Application programs are also stored within the EEPROM.
    Can be updated by downloading over the network.
  - Built-in watchdog timer
  - Each chip has a unique ID number.
    Effective during the logical installation of networks
  - Low electrical consumption mode supported through a sleep mode
  - Built-in selectable reset time
    Prolongs the power-on reset time for at least 50 ms and keeps the operation stable during this time. The reset time for reset after power on, however, can be set to 3-clock delay mode by programming.
  - High-impedance communication port (CP0 to CP3)
    The communication port pins (CP0 to CP3) attain high impedance. This eliminates the need for an external relay.
  - Built-in low-voltage detection circuit
    Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
    An external LVD must be used to assert reset at a power supply voltage below 4.5 V if the Neuron Chip is operated at 20 MHz.
  - Built-in programmable LVD (low-voltage detection) circuit
    An external LVD input pin (LVDin) is used to assert reset at a given voltage.
  - Firmware version 10
  - The package is SOP32-P-525-1.27 (lead-free type).

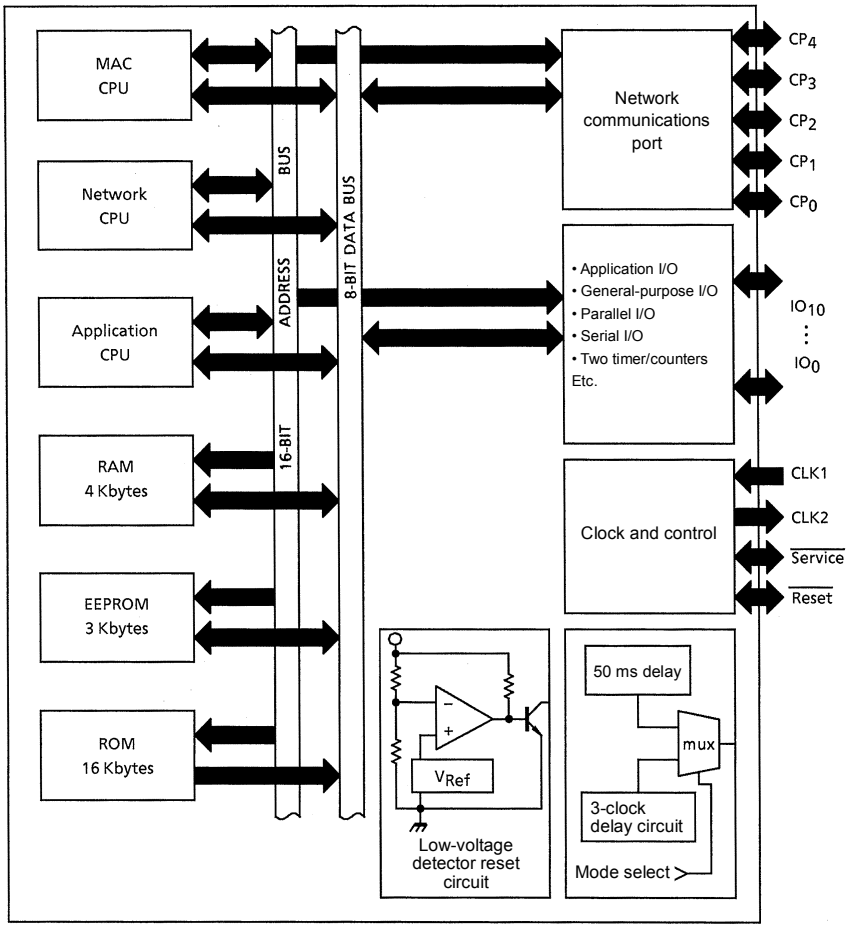
- Timing for the main I/O objects during 20 MHz Neuron Chip operations

I/O Model	10 MHz Timing	20 MHz Timing
Parallel	2.4 µs/byte	1.2 µs/byte
Bitshift	1, 10 or 15 kbps	2, 20 or 30 kbps
Magcard	Up to 8334 bps	Up to 16668 bps
Magtrack1	Up to 7246 bps	Up to 14492 bps
Neurowire master	1, 10 or 20 kbps	2, 20 or 40 kbps
Neurowire slave	Up to 18 kbps	Up to 36 kbps
Serial	600, 1200, 2400 or 4800 bps	1200, 2400, 4800 or 9600 bps
Touch	Supported	Not supported
Frequency output	Resolution: 0.4 to 51.2 µs Max range: 26.21 to 3355 ms	Resolution: 0.2 to 25.6 µs Max range: 13.1 to 1678 ms
Other timer/counter	Resolution: 0.2 to 25.6 µs Max range: 13.1 to 1678 ms	Resolution: 0.1 to 12.8 µs Max range: 6.55 to 839 ms

The specifications for the main timers during 20 MHz operations are as follows:

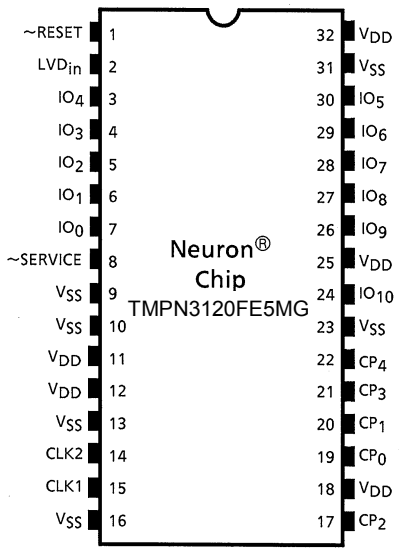
Watchdog timer	420 ms
Millisecond timers	1 to 32000 ms
Second timers	1 to 65000 s
Delay ( ) function	1 to 32767 counts
Get_tick_count ( ) function	409.6 µs per count

Block Diagram



Item	TMPN3120FE5MG
CPU	8-bit CPU × 3
RAM	4,096 bytes
ROM	16,384 bytes
EEPROM	3,072 bytes
16-bit timer/counter	2 channels
External memory interface	Not available
Package	32-pin SOP

Pin Connections



Note: All NC pins should be open.

Pin Functions

Pin No.	Pin Name	I/O	Pin Function
15	CLK1	Input	Oscillator connection, or external clock input
14	CLK2	Output	Oscillator connection. Leave open when the external clock is input to CLK1.
1	~RESET	I/O (built-in pull-up)	Reset pin (active low)
8	~SERVICE	I/O (built-in configurable pull-up)	Service pin. Indicator output during operation.
7 to 4	IO_0 to IO_3	I/O	Large current sink capacity (20 mA). General I/O port.
3, 30 to 28	IO_4 to IO_7	I/O (built-in configurable pull-up)	General I/O port. One of IO_4 to IO_7 can be specified as the No.1 timer/counter input. Output signals can be output to IO_0. IO_4 can be used as the No.2 timer/counter input with IO_1 as output.
27, 26, 24	IO_8 to IO_{10}	I/O	General I/O port. Can be used for serial communication with other devices.
11, 12, 18, 25, 32	V_{DD}	Input	Power input (5.0 V typ.)
9, 10, 13, 16, 23, 31	V_{SS}	Input	Power input (0 V GND)
2	LVD_{in}	Input	Input pin for programmable LVD (normally connected to V_{DD})
19, 20, 17, 21, 22	CP_0 to CP_4	I/O	Bidirectional port for communications. Supports several communications protocols through specifying of mode.

* : ● The ~SERVICE and IO_4 to IO_7 terminals are programmable pull-ups.
● All V_{DD} terminals must be externally connected.
● All V_{SS} terminals must be externally connected.

Maximum Ratings (V_{SS} = 0 V, V_{SS} typ.)

Item	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 7.0	V
Input voltage	$V_{IN\ (1)}$	−0.3 to V_{DD} + 0.3 V	V
Input voltage CP_0 to CP_3	$V_{IN\ (2)}$	−0.5 to V_{DD} + 1.3 V $V_{IN\ (2)} \leq$ 7.3 (Note 1)	V
Drain current	I_{DD}	200	mA
Source current	I_{SS}	300	mA
Power dissipation	P_D	800	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: V_{IN} (2) should not exceed 7.3 V.

Operating Conditions

Item	Symbol	Min	Typ.	Max	Unit
Operating voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage (TTL)	V_{IH}	2.0	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input voltage (CMOS)	V_{IH}	V_{DD} − 0.8 V	—	V_{DD}	V
	V_{IL}	V_{SS}	—	0.8	V
Input voltage CP_0 to CP_3 (differential mode)	V_{IH}	—	—	V_{DD} + 1.0 V	V
	V_{IL}	−0.1	—	—	
Operating frequency	f_{osc}	0.625	—	20	MHz
Operating temperature	T_{opr}	−40	—	85	°C

Electrical Characteristics

DC characteristic (V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = −40 to 85°C)

(The above operating conditions apply unless otherwise stated.)

Item	Symbol	Pins	Test Condition	Min	Max	Unit
LOW level input voltage (1)	V_{IL} (1)	IO_0 to IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—	0	0.8	V
LOW level input voltage (2)	V_{IL} (2)	~RESET	—	0	V_{DD} × 0.3	V
HIGH level input voltage (1)	V_{IH} (1)	IO_0 to IO_{10} CP_0, CP_3, CP_4, ~SERVICE	—	2.0	V_{DD}	V
HIGH level input voltage (2)	V_{IH} (2)	~RESET	—	V_{DD} − 0.7 V	V_{DD}	V
LOW output voltage (1)	V_{OL} (1)	IO_0 to IO_3 ~SERVICE, ~RESET	I_{OL} = 20 mA	0	0.8	V
			I_{OL} = 10 mA	0	0.4	
LOW output voltage (2)	V_{OL} (2)	CP_2, CP_3	I_{OL} = 40 mA	0	1.0	V
LOW output voltage (3)	V_{OL} (3)	Others (Note 1)	I_{OL} = 1.4 mA	0	0.4	V
HIGH output voltage (1)	V_{OH} (1)	IO_0 to IO_3	I_{OH} = −1.4 mA	V_{DD} − 0.4 V	V_{DD}	V
HIGH output voltage (2)	V_{OH} (2)	~SERVICE	I_{OH} = −1.4 mA	V_{DD} − 0.4 V	V_{DD}	V
HIGH output voltage (3)	V_{OH} (3)	CP_2, CP_3	I_{OH} = −40 mA	V_{DD} − 1.0 V	V_{DD}	V
HIGH output voltage (4)	V_{OH} (4)	Others (Note 1)	I_{OH} = −1.4 mA	V_{DD} − 0.4 V	V_{DD}	V
Input current	I_{IN}	(Note 2)	V_{IN} = V_{SS} to V_{DD}	−10	10	μA
Pull-up current	I_{PU} (Note 3)	IO_4 to IO_7 ~SERVICE, ~RESET	V_{IN} = 0 V	−30	−300	μA
Low-voltage detection level	V_{LVD}	V_{DD}	—	3.8	4.5	V

Note 1: Output voltage characteristics exclude the CLK2 pin.
Note 2: Excludes pull-up input pins.
Note 3: The IO_4 to IO_7 and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

Item		Symbol	Typ.	Max	Unit
Operating mode current consumption	20 MHz clock	$I_{DD\ (OP)}$	34	55	mA
	10 MHz clock		16	30	
	5 MHz clock		8.5	15	
	2.5 MHz clock		4.5	8	
	1.25 MHz clock		2.3	5	
	0.625 MHz clock		1.3	3	
Sleep mode current consumption		$I_{DD\ (SLP)}$	16	100	μA

Note: Test conditions for current dissipation:

V_{DD} = 5 V; all output = under no load; all input ≤ 0.2 V or ≥ (V_{DD} − 0.2 V); programmable pull-up = off; crystal oscillator clock input; differential receiver disabled.

The current value (typ.) is a typical value when Ta = 25°C.

The current value (max) applies to the rated temperature range at V_{DD} = 5.5 V.

200 μA (typ.) to 600 μA (max) is added to the current of the differential receiver when the receiver is enabled.

The differential receiver is enabled by either of the following conditions:

- When the Neuron Chip is in Run mode and the communication ports are in Differential mode.
- When the Neuron Chip is in Sleep mode, the communication ports are in Differential mode, and the Comm Port Wakeup is not masked.

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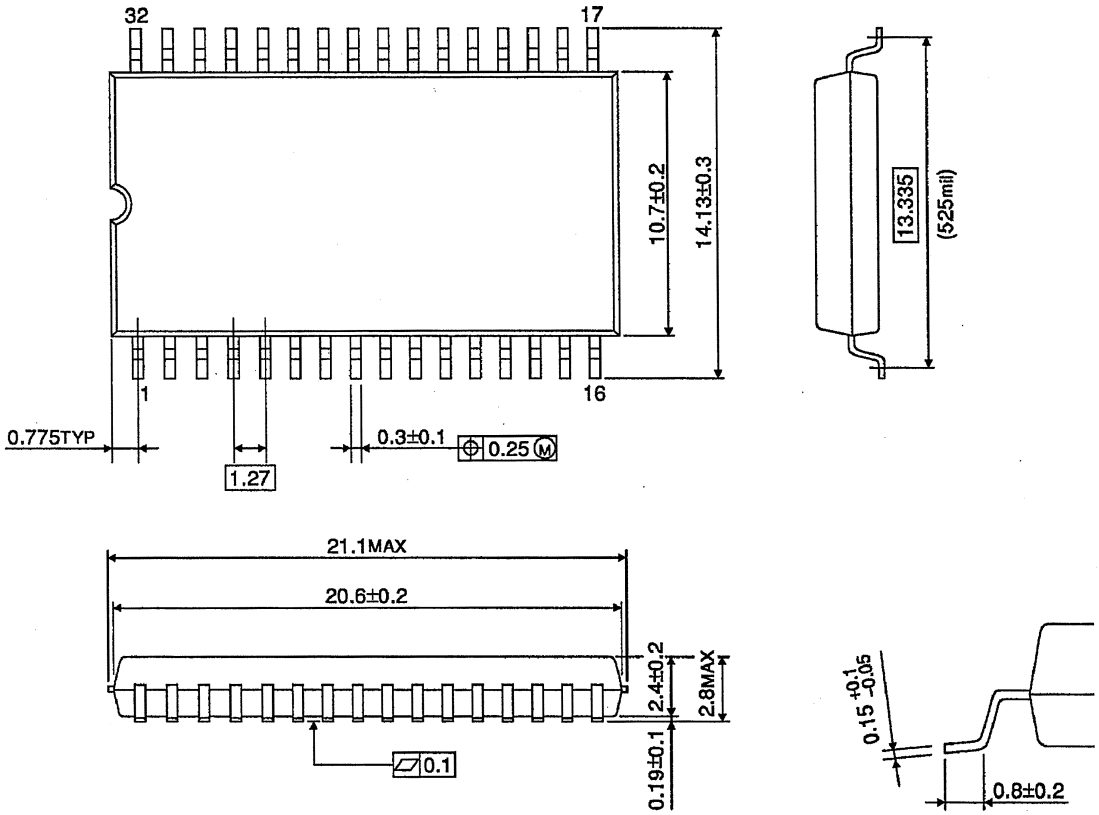
Package Dimensions

SOP32-P-525-1.27 Unit : mm



Weight : 1.1g (typ.)

Lead-free type

About solderability, following conditions were confirmed

- Solderability

(1) Use of Sn-37Pb solder Bath
- solder bath temperature = 230°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature = 245°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

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