

**Low Cost 5 REN Ringing SLIC for ISDN Modem/TA and WL**

The HC55171B low cost, 5 REN ringing SLIC is designed to accommodate a wide variety of short loop applications and provides the same degree of flexibility as the high performance HC55171. The flexible features include open circuit tip to ring DC voltages, user defined ringing waveforms, ring trip detection thresholds, and loop current limits that can be tailored for many applications. Additional features of the HC55171B are complex impedance matching, pulse metering, and transhybrid balance. The HC55171B is designed for use in short loop, low cost systems where traditional ring generation is not economically feasible.

The device is manufactured in a high voltage Dielectric Isolation (DI) process. The DI process provides substrate latch up immunity, resulting in a robust system design. A thermal shutdown with an alarm output and line fault protection are also included for operation in harsh environments.

**Ordering Information**

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE    | PKG. NO. |
|-------------|------------------|------------|----------|
| HC55171BIM  | -40 to 85        | 28 Ld PLCC | N28.45   |
| HC55171BIB  | -40 to 85        | 28 Ld SOIC | M28.3    |

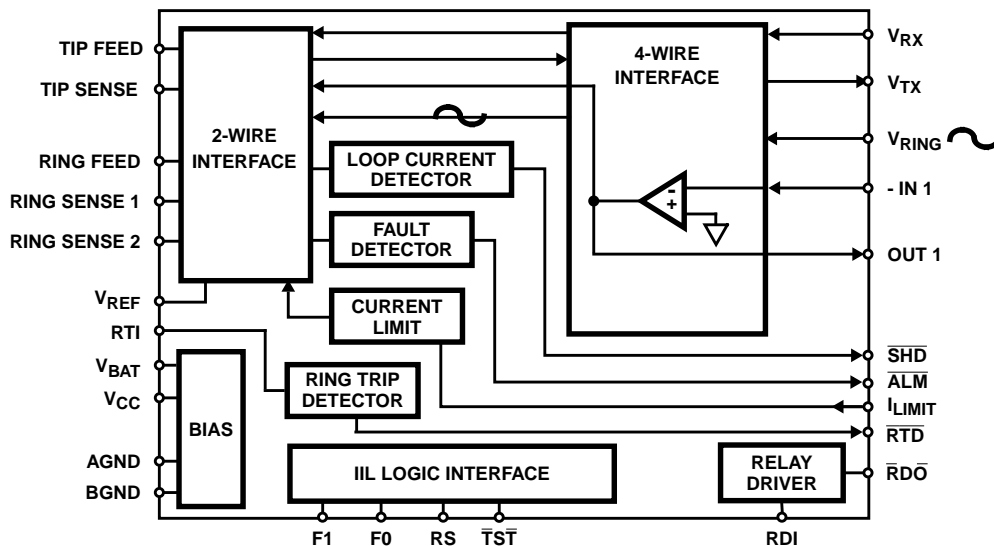
**Features**

- Load Drive Capability . . . . . 5 REN
- Trapezoidal, Square or Sine Wave Capability
- Ringing from -80V Battery . . . . . 75V<sub>p-p</sub>
- Ringing from -75V Battery . . . . . 70V<sub>p-p</sub>
- Ringing Current Independent of Loop Current Setting
- Ringing Crest Factor Independent of REN Loading
- Latchup Immune to Inductive Kick Back and Hot Plug
- Fax, Answering Machine and MTU Compatible
- Resistive and Complex Impedance Matching
- Programmable Loop Current Limit
- Switch Hook, Ring Trip and Ground Key Detection
- Single Low Voltage +5V Supply

**Applications**

- Solid State Line Interface Circuit for Hybrid Fiber Coax, Set Top Box, Voice/Data Modems
- Related Literature
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9636, Implementing an Analog Port for ISDN
  - AN549, The HC-5502/4X Telephone SLIC

**Block Diagram**



**Absolute Maximum Ratings**  $T_A = 25^{\circ}\text{C}$

|                            |               |
|----------------------------|---------------|
| Maximum Supply Voltages    |               |
| ( $V_{CC}$ )               | -0.5V to +7V  |
| ( $V_{CC}$ )-( $V_{BAT}$ ) | 90V           |
| Relay Drivers              | -0.5V to +15V |

**Operating Conditions**

|                                     |               |
|-------------------------------------|---------------|
| Temperature Range                   |               |
| HC55171BIM, HC55171BIB              | -40°C to 85°C |
| Relay Drivers                       | +5V to +12V   |
| Positive Power Supply ( $V_{CC}$ )  | +5V $\pm$ 5%  |
| Negative Power Supply ( $V_{BAT}$ ) | -16V to -80V  |

**Thermal Information**

|  |   |
|--|---|
| Thermal Resistance (Typical, Note 1)           | $\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ ) |
| PLCC Package                                   | 55  |
| SOIC Package                                   | 70  |
| Maximum Junction Temperature, Plastic Packages | 150°C   |
| Maximum Storage Temperature Range              | -65°C to 150°C                                |
| Maximum Lead Temperature (Soldering 10s)       | 300°C (SOIC, PLCC - Lead Tips Only)           |

**Die Characteristics**

|                        |            |
|------------------------|------------|
| Transistor Count       | 224        |
| Diode Count            | 28         |
| Die Dimensions         | 175 x 144  |
| Substrate Potential    | $V_{BAT}$  |
| Process                | Bipolar-DI |
| ESD (Human Body Model) | 500V       |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied*

**NOTES:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation board PC board in free air.
- All grounds (AGND, BGND) must be applied before  $V_{CC}$  or  $V_{BAT}$ . Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AGND must be applied first.

**Electrical Specifications** Unless Otherwise Specified, Typical Parameters are at  $T_A = 25^{\circ}\text{C}$ , Min-Max Parameters are over Operating Temperature Range,  $V_{BAT} = -24\text{V}$ ,  $V_{CC} = +5\text{V}$ , AGND = BGND = 0V. All AC Parameters are specified at 600Ω 2-Wire terminating impedance.

| PARAMETER  | TEST CONDITIONS  | MIN  | TYP        | MAX        | UNITS             |
|--|--|------|------------|------------|-------------------|
| <b>RINGING TRANSMISSION PARAMETERS</b>           |  |      |            |            |                   |
| $V_{RING}$ Input Impedance                       | (Note 3)   | -    | 5.4        | -          | kΩ                |
| 4-Wire to 2-Wire Gain                            | $V_{RING}$ to $V_{T-R}$ (Note 3)   | -    | 40         | -          | V/V               |
| <b>AC TRANSMISSION PARAMETERS</b>                |  |      |            |            |                   |
| RX Input Impedance                               | 300Hz to 3.4kHz (Note 3)   | -    | 108        | -          | kΩ                |
| OUT1 Positive Output Voltage Swing               | $R_L = 10\text{k}\Omega$ (Note 3)  | +2.5 | -          | -          | V                 |
| OUT1 Negative Output Voltage Swing               | $R_L = 10\text{k}\Omega$ (Note 3)  | -4.5 | -          | -          | V                 |
| 4-Wire Input Overload Level                      | 300Hz to 3.4kHz $R_L = 1200\Omega$ , 600Ω Reference (Note 3)               | -    | +3.1       | -          | $V_{PEAK}$        |
| 2-Wire Return Loss                               | Matched for 600Ω, f = 300Hz (Note 3)                                       | 37   | -          | -          | dB                |
|  | Matched for 600Ω, f = 1000Hz (Note 3)                                      | 40   | -          | -          | dB                |
|  | Matched for 600Ω, f = 3400Hz (Note 3)                                      | 30   | -          | -          | dB                |
| 2-Wire Longitudinal to Metallic Balance Off Hook | Per ANSI/IEEE STD 455-1976 300Hz to 3400Hz (Note 3)                        | 40   | -          | -          | dB                |
| 4-Wire Longitudinal Balance Off Hook             | 300Hz to 3400Hz (Note 3)   | 40   | -          | -          | dB                |
| Longitudinal Current Capability                  | $I_{LINE} = 40\text{mA}$ , $T_A = 25^{\circ}\text{C}$ (Note 3)             | -    | 40         | -          | $\text{mA}_{RMS}$ |
| Insertion Loss, 2-Wire to 4-Wire                 | 0dBmO, 1kHz, Includes Transhybrid Amp Gain = 3                             | -    | $\pm 0.05$ | $\pm 0.2$  | dB                |
| Insertion Loss, 4-Wire to 2-Wire                 | 0dBmO, 1kHz  | -    | $\pm 0.05$ | $\pm 0.2$  | dB                |
| Insertion Loss, 4-Wire to 4-Wire                 | 0dBmO, 1kHz, Includes Transhybrid Amp Gain = 3                             | -    | -          | $\pm 0.35$ | dB                |
| Frequency Response                               | 300Hz to 3400Hz Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω | -    | $\pm 0.02$ | $\pm 0.06$ | dB                |

## HC55171B

**Electrical Specifications** Unless Otherwise Specified, Typical Parameters are at  $T_A = 25^\circ\text{C}$ , Min-Max Parameters are over Operating Temperature Range,  $V_{BAT} = -24\text{V}$ ,  $V_{CC} = +5\text{V}$ ,  $AGND = BGND = 0\text{V}$ . All AC Parameters are specified at  $600\Omega$  2-Wire terminating impedance. **(Continued)**

| PARAMETER  | TEST CONDITIONS  | MIN   | TYP     | MAX        | UNITS            |
|--|--|-------|---------|------------|------------------|
| Level Linearity  | +3 to 0dBm, Referenced to -10dBm (Note 3)                        | -     | -       | $\pm 0.10$ | dB               |
|  | 0 to -40dBm, Referenced to -10dBm (Note 3)                       | -     | -       | $\pm 0.12$ | dB               |
|  | -40 to -55dBm, Referenced to -10dBm (Note 3)                     | -     | -       | $\pm 0.30$ | dB               |
| Absolute Delay, 2-Wire to 4-Wire   | 300Hz to 3400Hz (Note 3)   | -     | -       | 1.0        | $\mu\text{s}$    |
| Absolute Delay, 4-Wire to 2-Wire   | 300Hz to 3400Hz (Note 3)   | -     | -       | 1.0        | $\mu\text{s}$    |
| Absolute Delay, 4-Wire to 4-Wire   | 300Hz to 3400Hz (Note 3)   | -     | 0.95    | -          | $\mu\text{s}$    |
| Transhybrid Loss   | $V_{IN} = 1V_{P-P}$ at 1kHz (Note 3)                             | 36    | 40      | -          | dB               |
| Total Harmonic Distortion<br>2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire | Reference Level 0dBm at 600 $\Omega$<br>300Hz to 3400Hz (Note 3) | -     | -       | -50        | dB               |
| Idle Channel Noise<br>2-Wire and 4-Wire                                  | C-Message (Note 3)   | -     | 3       | -          | dBmC             |
|  | Psophometric (Note 3)  | -     | -87     | -          | dBmp             |
| PSRR, $V_{CC}$ to 2-Wire   | 30Hz to 200Hz, $R_L = 600\Omega$ (Note 3)                        | 30    | 35      | -          | dB               |
| PSRR, $V_{CC}$ to 4-Wire   |  | 45    | 47      | -          | dB               |
| PSRR, $V_{BAT}$ to 2-Wire  |  | 23    | 28      | -          | dB               |
| PSRR, $V_{BAT}$ to 4-Wire  |  | 33    | 38      | -          | dB               |
| PSRR, $V_{CC}$ to 2-Wire   | 200Hz to 3.4kHz, $R_L = 600\Omega$ (Note 3)                      | 33    | 35      | -          | dB               |
| PSRR, $V_{CC}$ to 4-Wire   |  | 44    | 46      | -          | dB               |
| PSRR, $V_{BAT}$ to 2-Wire  |  | 40    | 50      | -          | dB               |
| PSRR, $V_{BAT}$ to 4-Wire  |  | 50    | 60      | -          | dB               |
| PSRR, $V_{CC}$ to 2-Wire   | 3.4kHz to 16kHz, $R_L = 600\Omega$ (Note 3)                      | 30    | 34      | -          | dB               |
| PSRR, $V_{CC}$ to 4-Wire   |  | 35    | 40      | -          | dB               |
| PSRR, $V_{BAT}$ to 2-Wire  |  | 30    | 40      | -          | dB               |
| PSRR, $V_{BAT}$ to 4-Wire  |  | 40    | 50      | -          | dB               |
| <b>DC PARAMETERS</b>   |  |       |         |            |                  |
| Loop Current Programming Range   | (Note 4)   | 20    | -       | 60         | mA               |
| Loop Current Programming Accuracy  |  | -15   | -       | +15        | %                |
| Loop Current During Power Denial   | $R_L = 200\Omega$ , $V_{BAT} = -48\text{V}$                      | -     | $\pm 4$ | -          | mA               |
| Fault Current, Tip to Ground   | (Note 3)   | -     | 90      | -          | mA               |
| Fault Current, Ring to Ground  |  | -     | 100     | -          | mA               |
| Fault Current, Tip and Ring to Ground                                    | (Note 3)   | -     | 130     | -          | mA               |
| Switch Hook Detection Threshold  |  | 9     | 12      | 15         | mA               |
| Ring Trip Comparator Voltage Threshold                                   |  | -0.28 | -0.24   | -0.22      | V                |
| Thermal ALARM Output   | Safe Operating Die Temperature Exceeded<br>(Note 3)              | 140   | -       | 160        | $^\circ\text{C}$ |
| Dial Pulse Distortion  | (Note 3)   | -     | 0.1     | 0.5        | ms               |

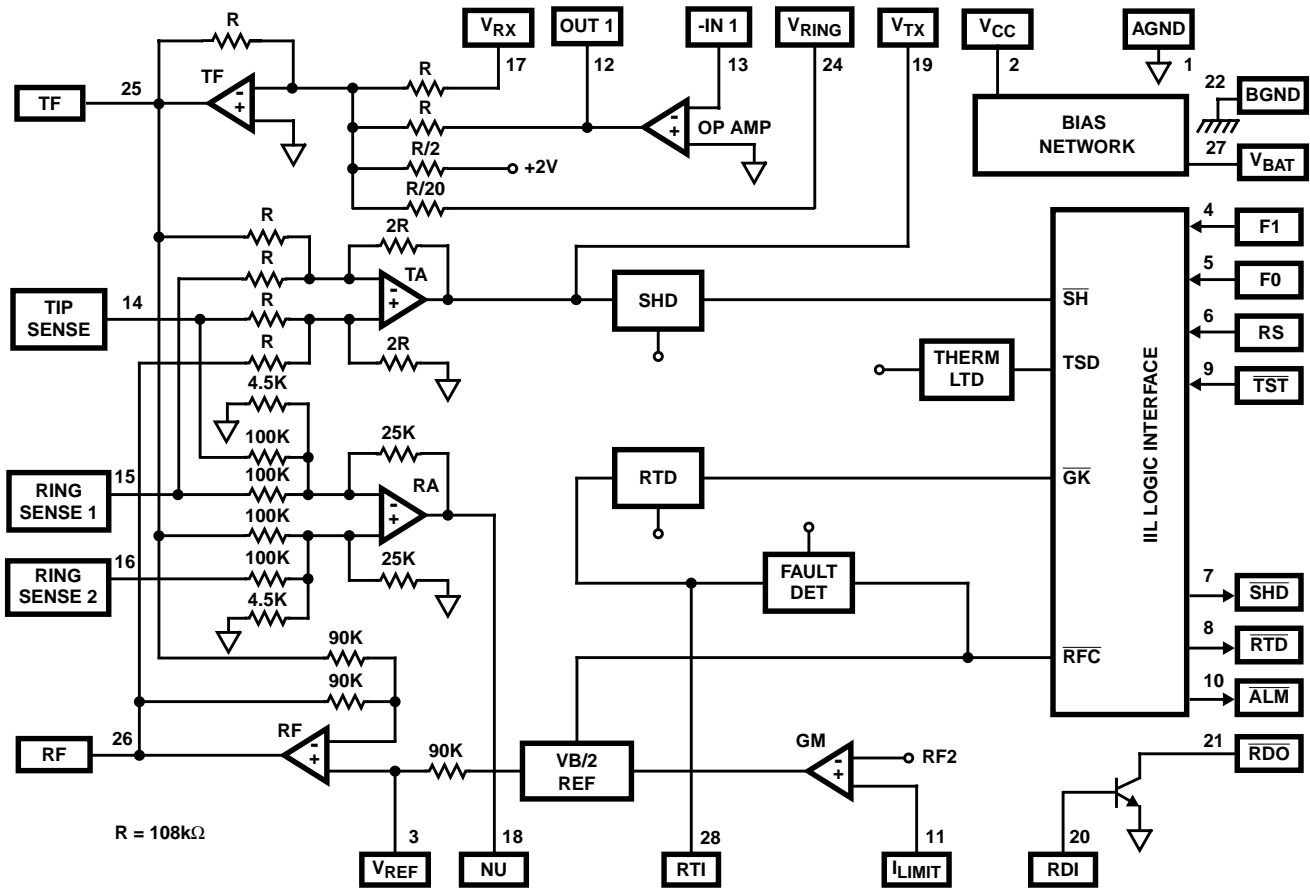
## HC55171B

**Electrical Specifications** Unless Otherwise Specified, Typical Parameters are at  $T_A = 25^\circ\text{C}$ , Min-Max Parameters are over Operating Temperature Range,  $V_{\text{BAT}} = -24\text{V}$ ,  $V_{\text{CC}} = +5\text{V}$ ,  $\text{AGND} = \text{BGND} = 0\text{V}$ . All AC Parameters are specified at  $600\Omega$  2-Wire terminating impedance. **(Continued)**

| PARAMETER  | TEST CONDITIONS   | MIN | TYP      | MAX       | UNITS         |
|--|---|-----|----------|-----------|---------------|
| <b>UNCOMMITTED RELAY DRIVER</b>  |   |     |          |           |               |
| On Voltage, $V_{\text{OL}}$  | $I_{\text{OL}} (\overline{\text{RDO}}) = 30\text{mA}$   | -   | 0.2      | 0.5       | V             |
| Off Leakage Current  |   | -   | $\pm 10$ | $\pm 100$ | $\mu\text{A}$ |
| <b>TTL/CMOS LOGIC INPUTS (F0, F1, RS, <math>\overline{\text{TST}}</math>, RDI)</b> |   |     |          |           |               |
| Logic Low Input Voltage  |   | 0   | -        | 0.8       | V             |
| Logic High Input Voltage   |   | 2.0 | -        | 5.5       | V             |
| Input Current  | $I_{\text{IH}}, 0\text{V} \leq V_{\text{IN}} \leq 5\text{V}$  | -   | -        | -1        | $\mu\text{A}$ |
| Input Current  | $I_{\text{IL}}, 0\text{V} \leq V_{\text{IN}} \leq 5\text{V}$  | -   | -        | -100      | $\mu\text{A}$ |
| <b>LOGIC OUTPUTS (SHD, RTD, ALM)</b>   |   |     |          |           |               |
| Logic Low Output Voltage   | $I_{\text{LOAD}} = 800\mu\text{A}$  | -   | 0.3      | 0.6       | V             |
| Logic High Output Voltage  | $I_{\text{LOAD}} = 40\mu\text{A}$   | 2.7 | -        | 5.5       | V             |
| <b>POWER DISSIPATION</b>   |   |     |          |           |               |
| Power Dissipation On Hook  | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -80\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 300      | -         | mW            |
|  | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -48\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 150      | -         | mW            |
| Power Dissipation Off Hook   | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -24\text{V}, R_{\text{LOOP}} = 600\Omega, I_{\text{L}} = 25\text{mA}$ | -   | 280      | -         | mW            |
| $I_{\text{CC}}$  | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -80\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 3        | 6         | mA            |
|  | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -48\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 2        | 5         | mA            |
|  | $V_{\text{CC}} = +5\text{V}, V_{\text{BAT}} = -24\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 1.9      | 5         | mA            |
| $I_{\text{BAT}}$   | $V_{\text{CC}} = +5\text{V}, V_{\text{B}^-} = -80\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 3.6      | 7         | mA            |
|  | $V_{\text{CC}} = +5\text{V}, V_{\text{B}^-} = -48\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 2.6      | 6         | mA            |
|  | $V_{\text{CC}} = +5\text{V}, V_{\text{B}^-} = -24\text{V}, R_{\text{LOOP}} = \infty$                                | -   | 2.3      | 4.5       | mA            |

**NOTES:**

- These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.
- This parameter directly affects device junction temperature. Refer to Power Dissipation discussion of data sheet for design information.



HC55171B DEVICE TRUTH TABLE

| F1 | F0 | STATE                                       |
|----|----|---|
| 0  | 0  | Loop power Denial Active                    |
| 0  | 1  | Power Down Latch RESET, Power on RESET      |
| 1  | 0  | $\overline{RD}$ Active (unbalanced ringing) |
| 1  | 1  | Normal Loop feed                            |

The truth table for the internal logic of the HC55171B is provided in the above table. This family of ringing SLICs can be configured to support traditional unbalanced ringing and through SLIC balanced ringing. The device operating states used by through SLIC ringing applications are loop power denial and normal feed. During loop power denial, the tip and ring amplifiers are disabled (high impedance) and the DC voltage of each amplifier approaches ground. The SLIC will not provide current to the subscriber loop during this mode and will not detect loop closure. Voice transmission occurs during the normal loop feed mode. During normal loop feed the SLIC is completely operational and performs all transmission and supervisory functions.

**Power Dissipation**

Careful thermal design is required to guarantee that the maximum junction temperature of 150°C of the device is not exceeded. The junction temperature of the SLIC can be calculated using:

$$T_J = T_A + \theta_{JA}(I_{CC} V_{CC} + I_{BAT} V_{BAT} - ((I_{LOOP})^2 \cdot R_{LOOP})) \tag{EQ. 1}$$

Where  $T_A$  is maximum ambient temperature and  $\theta_{JA}$  is junction to air thermal resistance (and is package dependent). The entire term in parentheses yields the SLIC power dissipation. The power dissipation of the subscriber loop does not contribute to device junction temperature and is subtracted from the power dissipation term. Operating at 85°C, the maximum PLCC SLIC power dissipation is 1.18W. Likewise, the maximum SOIC SLIC power dissipation is 0.92W.

## Circuit Operation and Design Information

### SLIC DESIGN EQUATIONS

| FUNCTION                       | EQUATION  | DEFINITION OF TERMS   |
|--------------------------------|---|---|
| 2-Wire to 4-Wire Gain          | $\frac{V_{OUT1}}{V_{2W}} = -\left(\frac{200}{Z_{2W}}\right) \cdot \frac{R_{ZO}}{R_{RF}}$  | $V_{OUT1}$ = SLIC 4-wire Output<br>$V_{2W}$ = Voltage across 2-wire load<br>$Z_{2W}$ = 2-Wire Impedance   |
| 4-Wire To 2-wire Gain          | $\frac{V_{2W}}{V_{RX}} = -2 \cdot \left(\frac{Z_{2W}}{Z_{2W} + Z_{SLIC}}\right)$  | $V_{2W}$ = Voltage Across 2-Wire Load<br>$V_{RX}$ = SLIC 4-Wire Input<br>$Z_{2W}$ = 2-Wire Impedance<br>$Z_{SLIC}$ = SLIC Synthesized Impedance |
| 4-Wire To 4-wire Gain          | $\frac{V_{OUT1}}{V_{RX}} = -2 \cdot \left(\frac{Z_{2W}}{Z_{2W} + Z_{SLIC}}\right) \cdot \frac{200}{Z_{2W}} \cdot \frac{R_{ZO}}{R_{RF}}$ | $V_{OUT1}$ = SLIC 4-Wire Output<br>$V_{RX}$ = SLIC 4-Wire Input<br>$Z_{2W}$ = 2-Wire Impedance<br>$Z_{SLIC}$ = SLIC Synthesized Impedance       |
| Loop Current Limit Programming | $I_{LIMIT} = \frac{(0.6)(R_{IL1} + R_{IL2})}{(200 \times R_{IL2})}$   | $I_{LIMIT}$ = Programmed Loop Current Limit<br>$R_{IL1}$ = Programming Resistor<br>$R_{IL2}$ = Programming Resistor                             |
| Impedance Matching             | $R_{ZO} = K \cdot (Z_{2W} - 100)$<br>$R_{RF} = K \cdot 200 \cdot 2$   | $Z_{2W}$ = 2-Wire Impedance<br>$K = 100$  |

### Through SLIC Ringing

The HC55171B uses linear amplification to produce the ringing signal. As a result the ringing SLIC can produce sinusoid, trapezoid or square wave ringing signals. Regardless of the wave shape, the ringing signal is balanced. The balanced waveform is another way of saying that the tip and ring DC potentials are the same during ringing.

### Trapezoidal Ringing

The trapezoidal ringing waveform provides a larger RMS voltage to the handset. Larger RMS voltages to the handset provide more power for ringing and also increase the loop length supported by the ringing SLIC.

One set of component values will satisfy the entire ringing loop range of the SLIC. A single resistor sets the open circuit RMS ringing voltage, which will set the crest factor of the ringing waveform. The crest factor of the HC55171B ringing waveform is independent of the ringing load (REN) and the loop length. Another robust feature of the HC55171B ringing SLIC is the ring trip detector circuit. The suggested values for the ring trip detector circuit cover quite a large range of applications.

The assumptions used to design the trapezoidal ringing application circuit are listed below:

- Loop current limit set to 25mA.
- Impedance matching is set to 600Ω resistive.
- 2-wire surge protection is not required.
- System able to monitor  $\overline{RTD}$  and  $\overline{SHD}$ .

Logic ringing signal is used to drive RC trapezoid network.

### Crest Factor Programming

As previously mentioned, a single resistor is required to set the crest factor of the trapezoidal waveform. The only design variable in determining the crest factor is the battery voltage. The battery voltage limits the peak signal swing and therefore directly determines the crest factor.

A set of tables will be provided to allow selection of the crest factor setting resistor. The tables will include crest factors below the Bellcore minimum of 1.2 since many ringing SLIC applications are not constrained by Bellcore requirements.

**TABLE 1. CREST FACTOR PROGRAMMING RESISTOR FOR  $V_{BAT} = -80V$**

| $R_{TRAP}$ | CF   | RMS  | $R_{TRAP}$ | CF   | RMS  |
|------------|------|------|------------|------|------|
| 0Ω         | 1.10 | 65.0 | 825Ω       | 1.25 | 57.6 |
| 389Ω       | 1.15 | 62.6 | 964Ω       | 1.30 | 55.4 |
| 640Ω       | 1.20 | 60.0 | 1095Ω      | 1.35 | 53.3 |

The RMS voltage listed in the table is the open circuit RMS voltage generated by the SLIC.

**TABLE 2. CREST FACTOR PROGRAMMING RESISTOR FOR  $V_{BAT} = -75V$**

| $R_{TRAP}$ | CF   | RMS  | $R_{TRAP}$ | CF   | RMS  |
|------------|------|------|------------|------|------|
| 0Ω         | 1.10 | 60.9 | 1010Ω      | 1.25 | 53.7 |
| 500Ω       | 1.15 | 58.3 | 1190Ω      | 1.30 | 51.6 |
| 791Ω       | 1.20 | 55.9 | 1334Ω      | 1.35 | 49.7 |

**TABLE 3. CREST FACTOR PROGRAMMING RESISTOR FOR  $V_{BAT} = -65V$**

| R <sub>TRAP</sub> | CF   | RMS  | R <sub>TRAP</sub> | CF   | RMS  |
|-------------------|------|------|-------------------|------|------|
| 0Ω                | 1.10 | 52.5 | 1330Ω             | 1.25 | 45.9 |
| 660Ω              | 1.15 | 49.8 | 1600Ω             | 1.30 | 44.1 |
| 1040Ω             | 1.20 | 47.8 | 1800Ω             | 1.35 | 42.5 |

**TABLE 4. CREST FACTOR PROGRAMMING RESISTOR FOR  $V_{BAT} = -60V$**

| R <sub>TRAP</sub> | CF   | RMS  | R <sub>TRAP</sub> | CF   | RMS  |
|-------------------|------|------|-------------------|------|------|
| 0Ω                | 1.10 | 48.2 | 1460Ω             | 1.25 | 42.0 |
| 740Ω              | 1.15 | 45.6 | 1760Ω             | 1.30 | 40.4 |
| 1129Ω             | 1.20 | 43.7 | 2030Ω             | 1.35 | 38.8 |

The voltages listed in the tables are driven from a logic source that will not drive the ringing input negative. If the ringing input is driven negative by 200mV, the peak-to-peak ringing amplitudes can be increased.

**Ringing Voltage Limiting Factors**

As the load impedance decreases (increasing R<sub>EN</sub>), the source impedance of the SLIC during ringing slightly attenuates the ringing signal.

If additional surge protection resistance must be used with the trapezoidal circuit, the loop length performance of the circuit will decrease proportionally to the added resistance in the Tip and Ring leads. For example if 30Ω protection resistors is used in each of the Tip and Ring leads, the ringing loop length will decrease by a total of 60Ω.

**Low Level Ringing Interface**

The trapezoidal application circuit only requires a cadenced logic signal applied to the wave shaping RC network to achieve ringing. When not ringing, the logic signal should be held low. When the logic signal is low, Tip will be near ground and Ring will be near battery. When the logic signal is high, Tip will be near battery and Ring will be near ground.

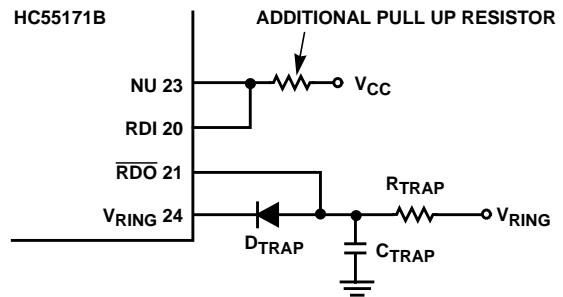
**Loop Detector Interface**

The  $\overline{RTD}$  output should be monitored for off hook detection during the ringing period. At all other times, the  $\overline{SHD}$  should be monitored for off hook detection. The application circuit can be modified to redirect the ring trip information through the  $\overline{SHD}$  interface. The change can be made by rewiring the application circuit, adding a pullup resistor to pin 23 and setting F0 low for the entire duration of the ringing period. The modifications to the application circuit for the single detector interface are shown in Figure 1.

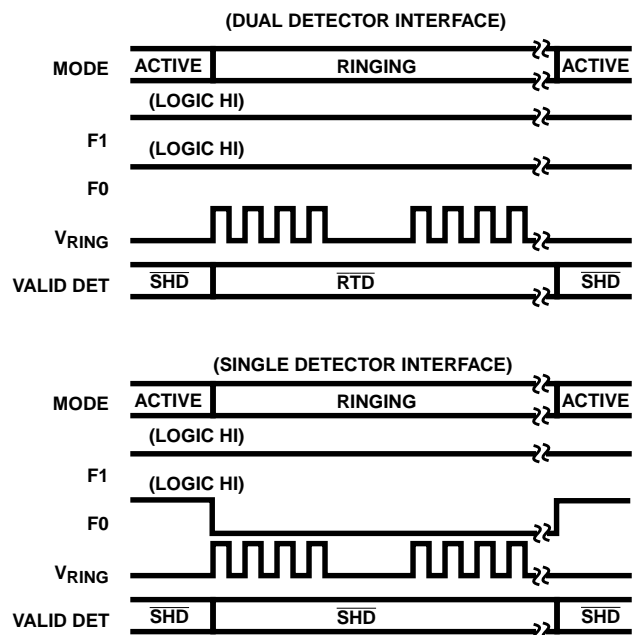
**SLIC Operating State During Ringing**

The SLIC control pin F1 should always be a logic high during ringing. The control pin F0 will either be a constant logic high (two detector interface) or a logic low (single detector

interface). Figure 2 shows the control interface for the dual detector interface and the single detector interface.



**FIGURE 1. APPLICATION CIRCUIT WIRING FOR SINGLE LOOP DETECTOR INTERFACE**

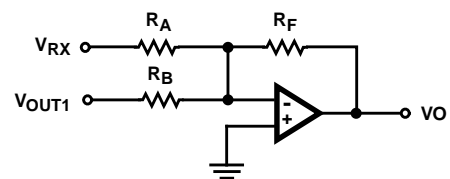


**FIGURE 2. DETECTOR LOGIC INTERFACES**

**Additional Application Information**

**Transhybrid Balance**

Since the receive signal and its echo are 180 degrees out of phase, the summing node of an operational amplifier can be used to cancel the echo. Nearly all CODECs have an internal amplifier for echo cancellation. The circuit in Figure 3 shows the cancellation amplifier circuit.



**FIGURE 3. TRANSHYBRID AMPLIFIER CIRCUIT**



When the SLIC is matched to a 600Ω load and only the sense resistors are used, the 4-wire to 4-wire gain is equal to 5/12 as predicted by the design equations. Therefore, by configuring the transhybrid amplifier with a gain of 2.4 in the echo path, cancellation can be achieved. The following equations:

$$V_O = -\left(V_{RX}\left(\frac{R_F}{R_A}\right) + V_{OUT1}\left(\frac{R_F}{R_B}\right)\right) \quad (\text{EQ. 2})$$

Substituting the fact that  $V_{OUT1}$  is -5/12 of  $V_{RX}$ :

$$V_O = -\left(V_{RX}\left(\frac{R_F}{R_A}\right) - V_{RX}\left(-\left(\frac{5}{12}\right)\right)\left(\frac{R_F}{R_B}\right)\right) \quad (\text{EQ. 3})$$

Since cancellation implies that under these conditions, the output  $V_O$  should be zero, set Equation 2 equal to zero and solve for  $R_B$ .

$$R_B = \frac{R_A}{2.4} \quad (\text{EQ. 4})$$

Another outcome of the transhybrid gain selection is the 2-wire to 4-wire gain of the SLIC as seen by the CODEC. The 5/12 voltage gain in the transmit path is relevant to the receive input as well as any signals from the 2-wire side. Therefore by setting the  $V_{OUT1}$  gain to 2.4 in the previous analysis, the 2-wire to 4-wire gain was set to unity.

**Single Supply CODEC Interface**

The majority of CODECs that interface to the ringing SLIC operate from a single +5V supply and ground. Figure 4 shows the circuitry required to properly interface the ringing SLIC to the single supply CODEC.

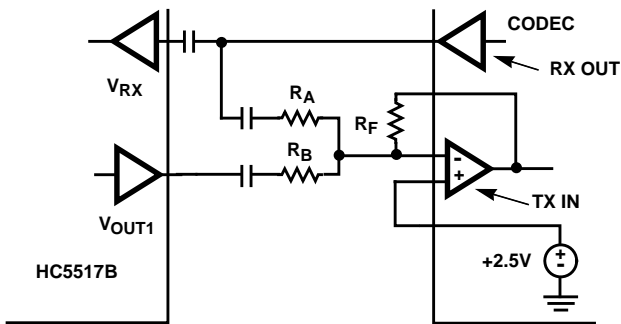


FIGURE 4. SINGLE SUPPLY CODEC INTERFACE

The CODEC signal names may vary from different manufacturers, but the function provided will be the same. The DC reference from the CODEC is used to bias the analog signals between +5V and ground. The capacitors are required so that the DC gain is unity for proper biasing from the CODEC reference. Also, the capacitors block DC signals that may interfere with SLIC or CODEC operation.

**Layout Guidelines and Considerations**

The printed circuit board trace length to all high impedance nodes should be kept as short as possible. Minimizing length will reduce the risk of noise or other unwanted signal pickup. The short lead length also applies to all high gain inputs. The set of circuit nodes that can be categorized as such are:

- $V_{RX}$  pin 27, the 4-wire voice input (low gain input).
- -IN1 pin 13, the inverting input of the internal amplifier.
- $V_{REF}$  pin 3, the noninverting input to ring feed amplifier.
- $V_{RING}$  pin 24, the 20V/V input for the ringing signal.

For multi layer boards, the traces connected to tip should not cross the traces connected to ring. Since they will be carrying high voltages, and could be subject to lightning or surge depending on the application, using a larger than minimum trace width is advised.

The 4-wire transmit and receive signal paths should not cross. The receive path is any trace associated with the  $V_{RX}$  input and the transmit path is any trace associated with  $V_{TX}$  output. The physical distance between the two signal paths should be maximized to reduce crosstalk, or separated by a ground trace.

The operating mode control signals and detector outputs should be routed away from the analog circuitry. Though the digital signals are nearly static, care should be taken to minimize coupling of the sharp digital edges to the analog signals.

The part has two ground pins, one is labeled AGND and the other BGND. Both pins should be connected together as close as possible to the SLIC. If a ground plane is available, then both AGND and BGND should be connected directly to the ground plane.

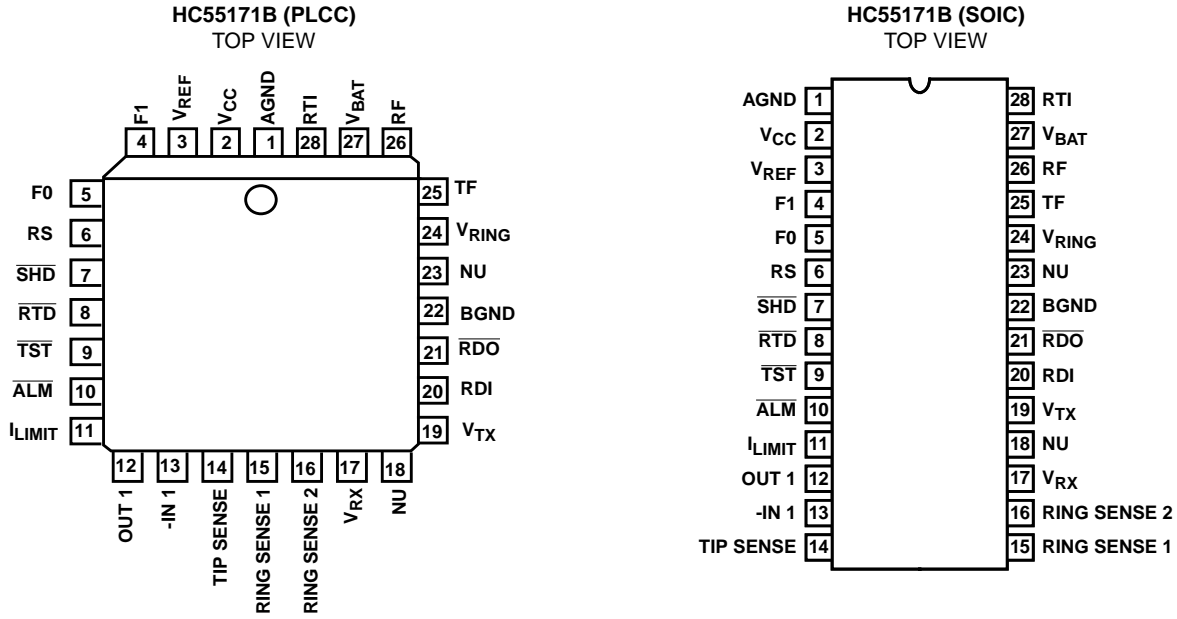
A ground plane that provides a low impedance return path for the supply currents should be used. A ground plane provides isolation between analog and digital signals. If the layout density does not accommodate a ground plane, a single point grounding scheme should be used.



**Pin Descriptions**

| PLCC | SYMBOL            | DESCRIPTION   |
|------|-------------------|---|
| 1    | AGND              | Analog Ground - Serves as a reference for the transmit output and receive input terminals.  |
| 2    | V <sub>CC</sub>   | Positive Voltage Source - Most Positive Supply.   |
| 3    | V <sub>REF</sub>  | An external voltage connected to this pin will override the internal V <sub>BAT</sub> /2 reference.   |
| 4    | F1                | Power Denial - An active low TTL compatible logic control input. When enabled, the output of the ring amplifier will ramp close to the output voltage of the tip amplifier.   |
| 5    | F0                | TTL compatible logic control input that must be tied high for proper SLIC operation.  |
| 6    | RS                | TTL compatible logic control input that must be tied high for proper SLIC operation.  |
| 7    | SHD               | Switch Hook Detection - An active low TTL compatible logic output. Indicates an off-hook condition.   |
| 8    | RTD               | Ring Trip Detection - An active low TTL compatible logic output. Indicates an off-hook condition when the phone is ringing.   |
| 9    | TST               | A TTL logic input. A low on this pin will keep the SLIC in a power down mode. The TST pin in conjunction with the ALM pin can provide thermal shutdown protection for the SLIC. Thermal shutdown is implemented by a system controller that monitors the ALM pin. When the ALM pin is active (low) the system controller issues a command to the TST pin (low) to power down the SLIC. The timing of the thermal recovery is controlled by the system controller. |
| 10   | ALM               | A TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded.  |
| 11   | I <sub>LMT</sub>  | Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions.   |
| 12   | OUT1              | The analog output of the spare operational amplifier.   |
| 13   | -IN1              | The inverting analog input of the spare operational amplifier. The non-inverting input is internally connected to AGND.   |
| 14   | TIP SENSE         | An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor. Functions with the RING terminal to receive voice signals and for loop monitoring purpose.  |
| 15   | RING SENSE 1      | An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals and for loop monitoring purposes.   |
| 16   | RING SENSE 2      | This is an internal sense mode that must be tied to RING SENSE 1 for proper SLIC operation.   |
| 17   | V <sub>RX</sub>   | Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.  |
| 18   | NU                | Not used in this application. This pin should be left floating.   |
| 19   | V <sub>TX</sub>   | Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.   |
| 20   | RDI               | TTL compatible input to drive the uncommitted relay driver.   |
| 21   | RDO               | This is the output of the uncommitted relay driver.   |
| 22   | BGND              | Battery Ground - All loop current and some quiescent current flows into this terminal.  |
| 23   | NU                | Not used in this application. This pin should be either grounded or left floating.  |
| 24   | V <sub>RING</sub> | Ring signal input.  |
| 25   | TF                | This is the output of the tip amplifier.  |
| 26   | RF                | This is the output of the ring amplifier.   |
| 27   | V <sub>BAT</sub>  | The negative battery source.  |
| 28   | RTI               | Ring Trip Input - This pin is connected to the external negative peak detector output for ring trip detection.  |

Pinouts



Trapezoidal Ringing Application Circuit

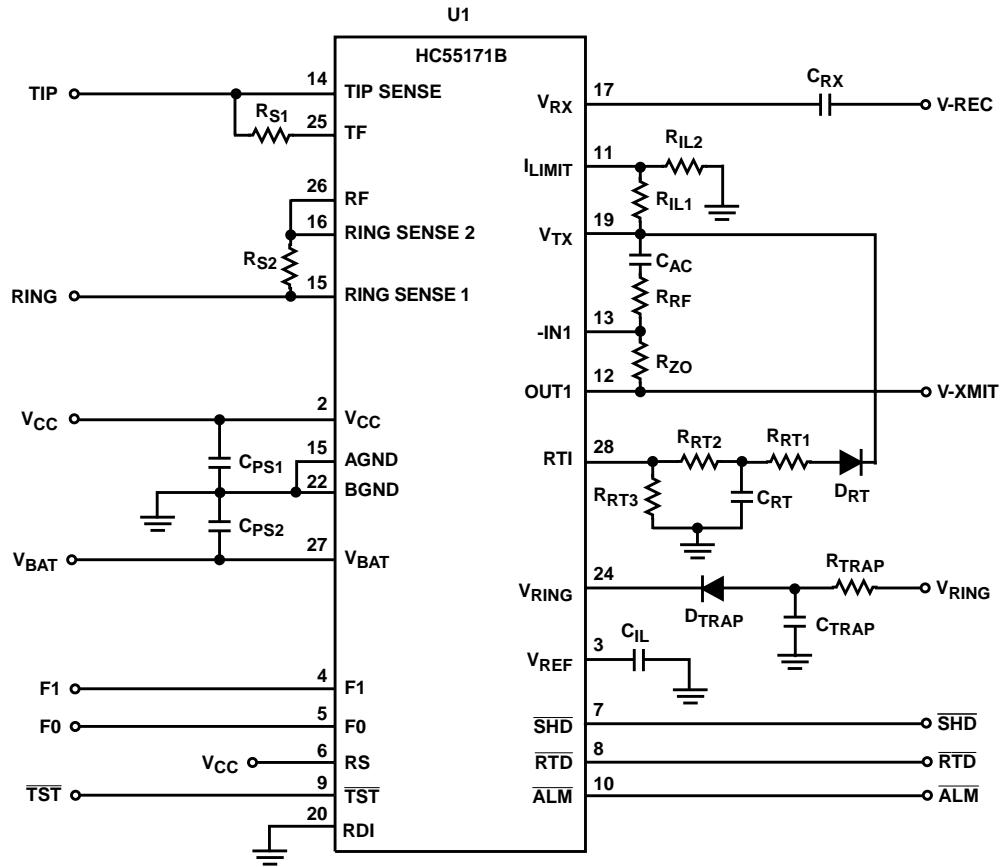


FIGURE 5. TRAPEZOIDAL RINGING APPLICATION CIRCUIT

**HC5517B Trapezoidal Ringing Application Circuit Parts List**

| COMPONENT         | VALUE    | TOLERANCE | RATING | COMPONENT          | VALUE        | TOLERANCE               | RATING |
|-------------------|----------|-----------|--------|--------------------|--------------|-------------------------|--------|
| U1 - Ringing SLIC | HC55171B | N/A       | N/A    | RIL2               | 7.68kΩ       | 1%                      | 1/8W   |
| RS1, RS2          | 49.9Ω    | 1%        | 1/2W   | RTRAP              | User-Defined | 1%                      | 1/8W   |
| RZO, RIL1         | 56.2kΩ   | 1%        | 1/8W   | CPS1, CPS2         | 0.1μF        | 10%                     | 100V   |
| RRT1              | 49.9kΩ   | 1%        | 1/8W   | CIL, CRT, CAC, CRX | 0.47μF       | 10%                     | 50V    |
| RRT2              | 1.5MΩ    | 1%        | 1/8W   | CTRAP              | 4.7μF        | 10%                     | 10V    |
| RRT3              | 51.1kΩ   | 1%        | 1/8W   | DRT, DTRAP         | 1N914        | Generic Rectifier Diode |        |
| RRF               | 45.3kΩ   | 1%        | 1/8W   |                    |              |                         |        |

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