# TEA1612T

## Zero voltage switching resonant converter controller

Rev. 01 — 24 September 2009 Product data sheet

## 1. General description

The TEA1612T is a monolithic integrated circuit implemented in a high-voltage double Diffused Metal Oxide Semiconductor (DMOS) process. The circuit is a high voltage controller for a zero-voltage switching resonant converter. The IC provides the drive function for two discrete power MOSFETs in a half-bridge configuration. It also includes a level-shift circuit, an oscillator with an accurately-programmable frequency range, a latched shut-down function, burst mode operation and a transconductance error amplifier.

The oscillator signal passes through a divide-by-two flip-flop before being fed to the output drivers in order to guarantee an accurate 50 % switching duty factor.

The circuit is very flexible and enables a broad range of applications for different mains voltages.

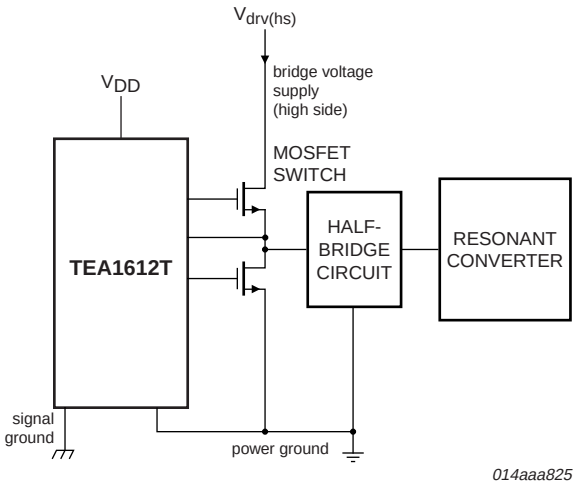



**Fig 1. Basic configuration**

## 2. Features

- Adjustable burst mode operation at low loads for low standby power
- Integrated high voltage level-shift function
- Integrated high voltage bootstrap diode
- Low start-up current
- Adjustable non-overlap time
- Internal Over Temperature Protection (OTP)
- Over Current Protection (OCP) that activates a shut-down timer

- Soft start timing pin
- Brown Out (BO) detection
- Transconductance error amplifier for ultra high-ohmic regulation feedback
- Latched shut-down circuit for Over Voltage Protection (OVP)
- Adjustable minimum and maximum frequencies
- Under Voltage Lock Out (UVLO)
- Fault latch reset input
- Wide (max. 20 V) supply voltage range
- PFC-off output

## 3. Applications

- TV and monitor power supplies
- High power adapter
- PC power supplies
- High voltage power supplies
- Office equipment

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TEA1612T | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |

## 5. Block diagram

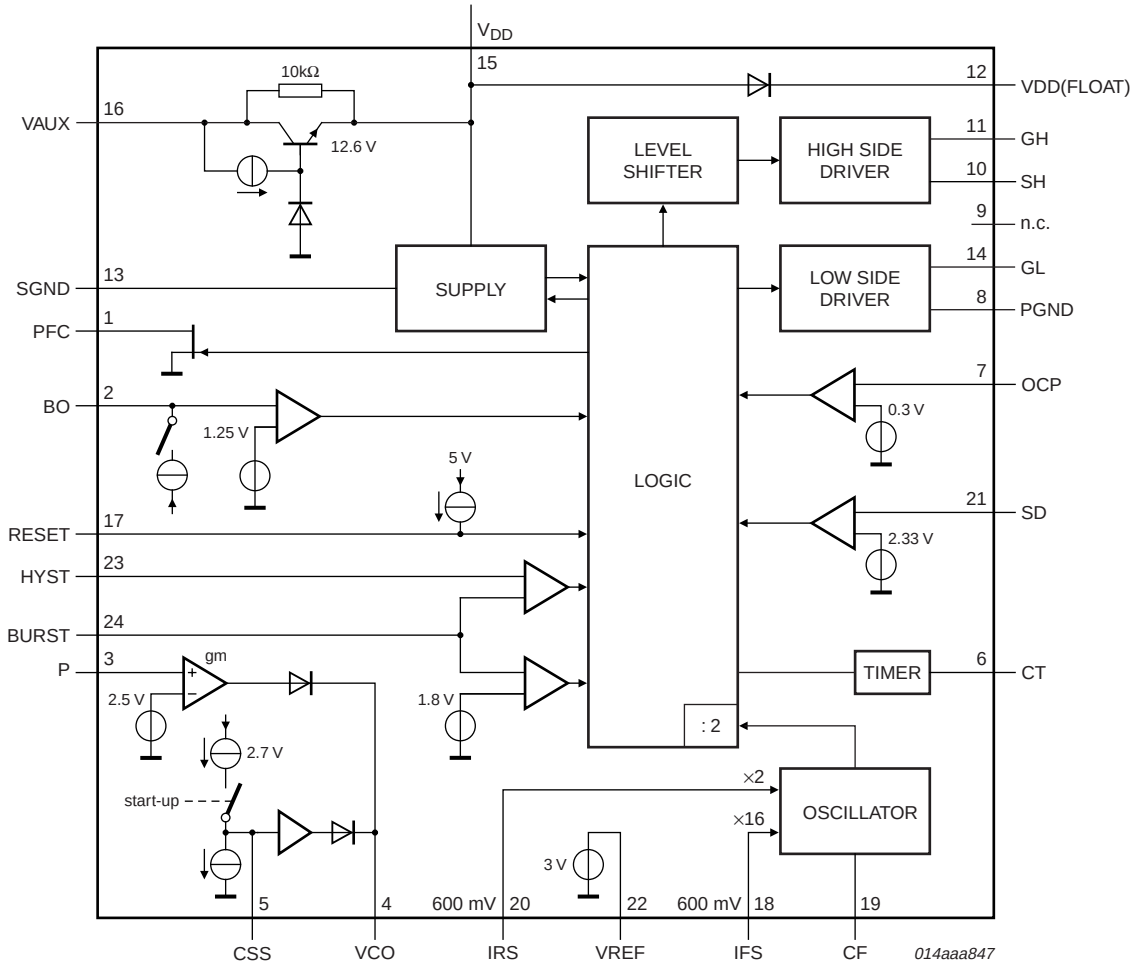



**Fig 2. Block diagram**

# 6. Pinning information

## 6.1 Pinning

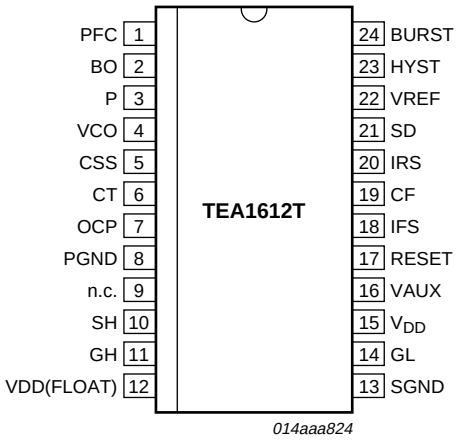



**Fig 3. Pin configuration**

## 6.2 Pin description

**Table 2. Pin description, proposal**

| Symbol | Pin | Description |
|---|---|---|
| PFC | 1 | PFC-control output |
| BO | 2 | brownout input |
| P | 3 | error amplifier non-inverting input |
| VCO | 4 | error amplifier output |
| CSS | 5 | soft start capacitor input |
| CT | 6 | timer capacitor input |
| OCP | 7 | overcurrent protection input |
| PGND | 8 | power ground |
| n.c. | 9 | not connected[1] |
| SH | 10 | high side switch source connection |
| GH | 11 | high side switch gate connection |
| VDD(FLOAT) | 12 | floating supply high side driver |
| SGND | 13 | signal ground |
| GL | 14 | low side switch gate connection |
| $V_{DD}$ | 15 | supply voltage |
| VAUX | 16 | auxiliary supply voltage |
| RESET | 17 | latch reset input |
| IFS | 18 | oscillator discharge current input |
| CF | 19 | oscillator capacitor |
| IRS | 20 | oscillator charge input current |
| SD | 21 | shut-down input |

**Table 2. Pin description, proposal**

| Symbol | Pin | Description |
|---|---|---|
| VREF | 22 | reference voltage |
| HYST | 23 | hysteresis reference input for burst mode |
| BURST | 24 | burst comparator input |

[1] Provided as a high voltage spacer

# 7. Functional description

## 7.1 Start-up

When the applied voltage at pin $V_{DD}$ reaches $V_{DD(init)}$ (see Figure 4), the low side power switch is turned-on while the high side power switch remains in the non-conducting state. This start-up output state guarantees the initial charging of the bootstrap capacitor ($C_{boot}$) used for the floating supply of the high side driver.

During start-up, the voltage on the frequency capacitor ($C_f$) is zero and defines the start-up state. The voltage at the soft start pin (CSS) is set to 2.7 V. The CSS pin voltage is copied to the VCO pin via a buffer and switching starts at about 80 % of the maximum frequency at the moment $V_{DD}$ reaches the start level.

The start-up state is maintained until $V_{DD}$ reaches the start level (13.5 V), the oscillator is activated and the converter starts operating.

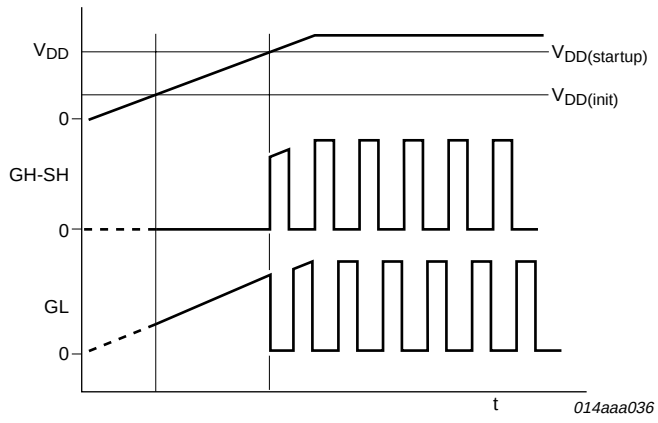



**Fig 4. Start-up**

## 7.2 Oscillator

The internal oscillator is a current-controlled oscillator that generates a sawtooth output. The frequency of the sawtooth is determined by the external capacitor $C_f$ and the currents flowing into the IFS and IRS pins.

The minimum frequency and the non-overlap time are set by the capacitor $C_f$ and resistors $R_{f(min)}$ and $R_{no}$. The maximum frequency is set by resistor $R_{\Delta f}$ (see Figure 7). The oscillator frequency is exactly twice the bridge frequency to achieve an accurate 50 % duty factor. An overview of the oscillator and driver signals is given in Figure 5.

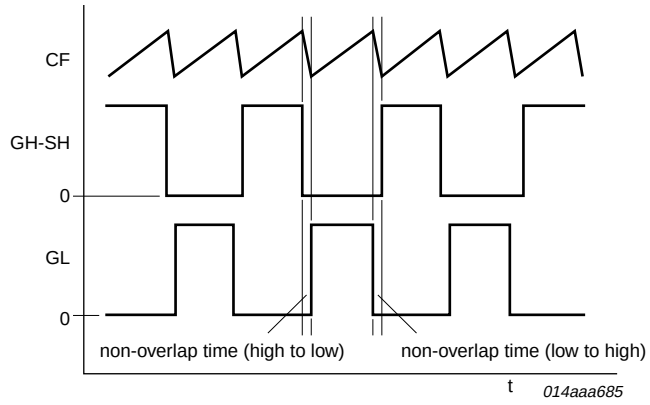



**Fig 5. Oscillator and driver signals**

## 7.3 Non-overlap time resistor

The non-overlap time resistor $R_{no}$ is connected between the 3 V reference pin VREF, and the IFS current input pin (see Figure 7). The voltage on the IFS pin is kept constant at a temperature independent value of 0.6 V. The current that flows into the IFS pin is determined by resistor's $R_{no}$ 2.4 V voltage drop divided by its value. The IFS input current equals 1/16 of the discharge current of capacitor $C_f$ and determines the falling slope of the oscillator.

The falling slope time is used to create a non-overlap time ($t_{no}$) between two successive switching actions of the half-bridge switches:

$$I_{IFS} = \frac{2.4V}{R_{no}}$$

$$t_{no} = \frac{C_f \times \Delta V_{Cf}}{16 \times I_{IFS}}$$

$$t_{IFS} = t_{no}$$

## 7.4 Minimum frequency resistor

The $R_{f(min)}$ resistor is connected between the VREF pin (3 V reference voltage) and the IRS current input pin (held at a temperature independent voltage level of 0.6 V). The charge current of the capacitor $C_f$ is twice the current flowing into the IRS pin.

The $R_{f(min)}$ resistor has a voltage drop of 2.4 V and its resistance defines the minimum charge current (rising slope) of the $C_f$ capacitor if the control current is zero. The minimum frequency is defined by this minimum charge current ($I_{IRS1}$) and the discharge current:

$$I_{IRS1} = \frac{2.4V}{R_{f(min)}}$$

$$t_{IRS1} = \frac{C_f \times \Delta V_{Cf}}{2 \times I_{IRS1}}$$

$$f_{osc(min)} = \frac{1}{t_{no} + t_{IRS1}}$$

$$f_{bridge(min)} = \frac{f_{osc(min)}}{2}$$

## 7.5 Maximum frequency resistor

The output voltage is regulated by changing the frequency of the half-bridge converter. The maximum frequency is determined by the $R_{\Delta f}$ resistor which is connected between the error amplifier output VCO and the oscillator current input pin IRS. The current that flows through the $R_{\Delta f}$ resistor ($I_{IRS2}$) is added to the current flowing through the $R_{f(min)}$ resistor. As a result, the charge current $I_{CF}$ increases and the oscillation frequency increases. As the falling slope of the oscillator is constant, the relationship between the output frequency and the charge current is not a linear function (see Figure 6 and Figure 7):

$$I_{IRS2} = \frac{V_{VCO} - 0.6}{R_{\Delta f}}$$

$$t_{IRS2} = \frac{C_f \times \Delta V_{Cf}}{2 \times (I_{IRS1} + I_{IRS2})}$$

The maximum output voltage of the error amplifier and the value of $R_{\Delta f}$ determine the maximum frequency:

$$I_{IRS2(max)} = \frac{V_{VCO(max)} - 0.6}{R_{\Delta f}}$$

$$t_{IRS(min)} = \frac{C_f \times \Delta V_{Cf}}{2 \times (I_{IRS2} + I_{IRS2(max)})}$$

$$f_{osc(max)} = \frac{1}{T_{OSC}}$$

$$f_{bridge(max)} = \frac{f_{osc(max)}}{2}$$

$$T_{OSC} = t_{IRS(min)} + t_{IFS}$$

Bridge frequency accuracy is optimum in the low frequency region. At higher frequencies both the non-overlap time and the oscillator frequency show a decay.

The frequency of the oscillator depends on the value of capacitor $C_f$, the peak-to-peak voltage swing $V_{CF}$, and the charge and discharge currents. However, at higher frequencies the accuracy decreases due to delays in the circuit.

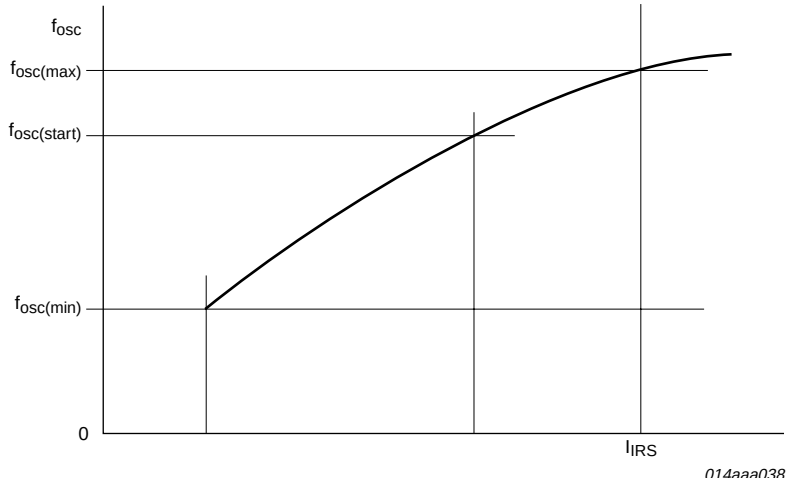



**Fig 6. Frequency range**

## 7.6 Error amplifier

The error amplifier is a transconductance amplifier. Thus the output current at pin VCO is determined by the amplifier transconductance, the differential voltage on input pin P, and the internal reference voltage (2.5 V). The output current $I_{VCO}$ is fed to the IRS input of the current-controlled oscillator.

The source capability of the error amplifier increases current in the IRS pin when the differential input voltage is positive. Therefore the minimum current is determined by resistor $R_{f(min)}$ and the minimum frequency setting is independent of the characteristics of the error amplifier.

The error amplifier has a maximum output current of 0.5 mA for an output voltage up to 2.5 V. If the source current decreases, the oscillator frequency also decreases resulting in a higher regulated output voltage.

During start-up, the output voltage of the amplifier is connected to the soft start (CSS) pin via a buffer. This will hold the VCO pin at a constant value of $V_{VCO(start)}$.

## 7.7 Soft start

The CSS pin voltage is copied to the VCO pin via a buffer. This buffer only has a source capability i.e. it can only charge the VCO pin. This means that the error amplifier output can increase the VCO pin voltage above the CSS voltage level.

At start-up the soft start capacitor is charged to $V_{VCO(start)}$ setting a start-up frequency of about 80 % of the maximum frequency. After start-up the external soft start capacitor is discharged by $I_{start(soft)}$. The VCO pin voltage follows the CSS voltage (discharging takes place via $R_{\Delta f}$) and the frequency sweeps down. The CSS capacitor determines the frequency sweep rate.

When the circuit comes into regulation, the error amplifier output controls the VCO pin voltage and the CSS voltage sweeps down further to zero volt.

## 7.8 VAUX input

The TEA1612T can start up either via a start-up bleeder resistor (connected to the high voltage and $V_{DD}$) or via the VAUX input. In the latter case the internal 10 kΩ resistor (from VAUX to $V_{DD}$) initiates charging of the $V_{DD}$ capacitor after which the series regulator takes over. The series regulator is active up to the moment that $V_{DD}$ equals $V_{DD(reg)}$. Further charging to $V_{DD(startup)}$ is done via the internal 10 kΩ resistor.

In oscillation state the start-up resistor is no longer capable of delivering the $V_{DD}$ supply current, so an auxiliary supply (for instance, via an auxiliary winding or a dV/dt supply) needs to take over. The VAUX input facilitates a series regulator which regulates its output voltage (= $V_{DD}$) to $V_{DD(reg)}$.

## 7.9 Burst mode

In the application the amount of converted power can be estimated from the actual operating frequency: the higher the frequency, the lower the output power. This frequency is proportional to the feedback current to the IRS pin which is measured via a sense resistor $R_{fb2}$ (see Figure 7). The actual feedback current equals $1/R_{fb2} \times (V_{BURST} - V_{IRS})$.

When the voltage at the BURST pin exceeds $V_{ref(BURST)}$, the TEA1612T output drivers (GL, GH) are made inactive (i.e. low). The output drivers are enabled again when the voltage at the BURST pin falls below the preset voltage at the HYST pin.

## 7.10 Shut-down

The shut-down input on pin SD has an accurate threshold level of 2.33 V. When the voltage on input SD reaches 2.33 V, the TEA1612T enters shut-down mode.

During shut-down mode, $V_{DD}$ is clamped by an internal Zener diode at 12.0 V with 1 mA input current. This clamp prevents $V_{DD}$ rising above the rating of 14 V due to low supply current to the TEA1612T in shut-down mode.

When the TEA1612T is in shut-down mode, it can only be activated again by lowering $V_{DD}$ to below the $V_{DD(rst)}$ level (typically 5.3 V) or by making the reset input active. The shut-down latch is then reset and a new start-up cycle can commence.

In shut-down mode the GL pin is high and the GH pin is low. In this way the bootstrap capacitor remains charged so that after a reset a new cycle can start well defined.

## 7.11 Latch reset input

The internal shut-down latch can be reset via the reset input.This input is active low.

## 7.12 Overcurrent protection and timer

The OCP input continuously compares the voltage on pin OCP with $V_{ref(OCP)}$. When the OCP pin voltage is higher than $V_{ref(OCP)}$, the timer capacitor CT will be charged with $I_{ch}$ during the next full CF cycle or else the timer capacitor will be discharged with $I_{leak}$.

In case the CT voltage exceeds $V_{trip(H)(CT)}$ the TEA1612T will switch to shut-down mode. The timer capacitor will be discharged with $I_{dch}$ until the CT voltage reaches $V_{trip(L)(CT)}$ after which a soft start cycle is started.

## 7.13 Overtemperature protection

The TEA1612T continuously monitors its temperature. When the temperature exceeds the $T_{otp(act)}$ level, the TEA1612T will switch to the shut-down mode.

## 7.14 Brownout protection

The brownout protection compares the actual BO pin with the $V_{trip(bo)}$ voltage. If the BO voltage (see Figure 7) is lower than $V_{trip(bo)}$, the TEA1612T switches to start-up mode and activates an internal current source $I_{bo(hys)}$ to create a brownout hysteresis. When the BO pin voltage becomes larger than $V_{trip(bo)}$, the TEA1612T will start-up again.

## 7.15 PFC disable function

The PFC output pin is an open-drain output. Operation of the PFC pin is internally enabled when the voltage on the BO pin is higher than $V_{trip(bo)}$. When the voltage is lower than $V_{trip(bo)}$, the PFC output is always in the open-drain state.

The PFC output is pulled low when:

- The overtemperature protection is active.
- The OCP timer has timed out.
- The TEA1612T has been set to shut-down.
- During the off-time in burst mode.

This PFC output signal can be used to switch off the power corrector in the application during Burst mode (and during protection) to further reduce standby power losses.

# 8. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltages** | | | | | | |
| $V_{drv(hs)}$ | high-side driver voltage | | | 0 | 600 | V |
| $V_{DD}$ | supply voltage | | [1] | 0 | 14 | V |
| $V_{aux}$ | auxiliary voltage | | [1] | 0 | 20 | V |
| **Voltages on pins P, SD, RESET, OCP, BO, PFC, BURST, HYST and CT** | | | | | | |
| $V_I$ | input voltage | | | 0 | 5 | V |
| **Currents** | | | | | | |
| $I_{IFS}$ | current on pin IFS | | | - | 1 ÷ 16 | mA |
| $I_{IRS}$ | current on pin IRS | | | - | 1 | mA |
| $I_{VREF}$ | current on pin VREF | | | - | –2 | mA |
| **Power and temperature** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb}$ < 70 °C | | - | 0.8 | W |
| $T_{amb}$ | ambient temperature | operating | | –25 | +70 | °C |
| $T_{stg}$ | storage temperature | | | –25 | +150 | °C |
| **Handling** | | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | | [2] | - | 2000 | V |
| | | | [3] | - | 200 | V |

[1] It is recommended that a 100 nF capacitor be placed as close as possible to the $V_{DD}$ pin (as indicated in Figure 7, and in the application note).

[2] Human body model class 2: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[3] Machine model class 2: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and 10 Ω resistor.

# 9. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 100 | K/W |

# 10. Characteristics

**Table 5. Characteristics**

*All voltages are referred to the ground pins which must be connected externally; positive currents flow into the IC; $V_{DD}$ = 13 V and $T_{amb}$ = 25 °C; tested using the circuit shown in Figure 7, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **High voltage pins VDD(FLOAT), GH and SH** | | | | | | |
| $I_{leak}$ | leakage current | $V_{DD(float)}$, $V_{GH}$ and $V_{SH}$ = 600 V | - | - | 30 | µA |
| **Supply pins $V_{DD}$, VAUX** | | | | | | |
| $V_{DD(init)}$ | initial supply voltage | low side on; high side off | - | 4 | 5 | V |
| $V_{DD(startup)}$ | start-up supply voltage | | 12.9 | 13.4 | 13.9 | V |
| $V_{DD(stop)}$ | stop supply voltage | | 9.0 | 9.4 | 9.8 | V |
| $V_{DD(hys)}$ | hysteresis of supply voltage | | 3.8 | 4.0 | 4.2 | V |
| $V_{DD(reg)}$ | regulation supply voltage | $V_{aux}$ = 17 V | - | 12.6 | - | V |
| $V_{DD}$ | supply voltage | $V_{aux}$ = 17 V, $I_{VDD}$ = 50 mA, oscillation state | - | 12.3 | - | V |
| | | clamp voltage in shut-down state; low side on; high side off; $I_{DD}$ = 1 mA | 11.0 | 12.0 | 13.0 | V |
| $V_{DD(rst)}$ | reset supply voltage | | 4.5 | 5.6 | 6.3 | V |
| $I_{DD}$ | supply current: | low side on; high side off; $C_f$ = 100 pF; $I_{IFS}$ = 0.5 mA; $I_{IRS}$ = 50 µA; low side off; high side off; $V_{DD}$ = 9 V[1] | | | | |
| | start-up | | 210 | 260 | 310 | µA |
| | operating | | - | 2.0 | - | mA |
| | shut-down | | - | 220 | 270 | µA |
| **Reference voltage on pin VREF** | | | | | | |
| $V_{ref}$ | reference voltage | $I_{ref}$ = 0 mA | 2.9 | 3.0 | 3.1 | V |
| $I_{ref}$ | reference current | source only | –2.0 | - | - | mA |
| $Z_o$ | output impedance | $I_{ref}$ = –1 mA | - | 5.0 | - | Ω |
| TC | temperature coefficient | $I_{ref}$ = 0 mA; $T_j$ = 25 °C to 150 °C | - | –0.3 | - | mV/K |
| **Current controlled oscillator pins IRS, IFS, CF** | | | | | | |
| $I_{ch(CF)min}$ | minimum charge current on pin CF | $I_{IRS}$ = 15 µA; $V_{CF}$ = 2 V | 28 | 30 | 32 | µA |
| $I_{ch(CF)max}$ | maximum charge current on pin CF | $I_{IRS}$ = 200 µA; $V_{CF}$ = 2 V | 340 | 380 | 420 | µA |
| $V_{IRS}$ | voltage on pin IRS | $I_{IRS}$ = 200 µA | 590 | 620 | 650 | mV |
| $I_{dch(CF)min}$ | minimum discharge current on pin CF | $I_{IFS}$ = 50 µA ÷ 16; $V_{CF}$ = 2 V | 47 | 50 | 53 | µA |
| $I_{dch(CF)max}$ | maximum discharge current on pin CF | $I_{IFS}$ = 1 mA ÷ 16; $V_{CF}$ = 2 V | 0.89 | 0.94 | 0.99 | mA |
| $V_{IFS}$ | voltage on pin IFS | $I_{IFS}$ = 1 mA ÷ 16 | 590 | 620 | 650 | mV |
| $f_{bridge(min)}$ | minimum bridge frequency | $C_f$ = 100 pF; $I_{IFS}$ = 0.5 mA ÷ 16; $I_{IRS}$ = 50 µA; $f_{bridge} = f_{OSC} \div 2$ | 156 | 167 | 178 | kHz |

**Table 5. Characteristics** *...continued*

*All voltages are referred to the ground pins which must be connected externally; positive currents flow into the IC; $V_{DD}$ = 13 V and $T_{amb}$ = 25 °C; tested using the circuit shown in Figure 7, unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{bridge(max)}$ | maximum bridge frequency | $C_f$ = 100 pF; $I_{IFS}$ = 1 mA ÷ 16; $I_{IRS}$ = 200 µA; $f_{bridge} = f_{OSC} \div 2$ | [2] | 395 | 440 | 485 | kHz |
| $V_{trip(L)}$ | LOW-level trip voltage | pin CF; DC level | | - | 1.27 | - | V |
| $V_{trip(H)}$ | HIGH-level trip voltage | pin CF; DC level | | - | 2.97 | - | V |
| $V_{CF(p-p)}$ | peak-to-peak voltage on pin CF | DC level | | 1.6 | 1.7 | 1.8 | V |
| $t_{no}$ | non-overlap time | $C_f$ = 100 pF; $I_{IFS}$ = 0.5 mA ÷ 16; $I_{IRS}$ = 50 µA | | 0.58 | 0.63 | 0.68 | µs |
| $I_{dch(osc)}/I_{IFS}$ | oscillator discharge current to current on pin IFS ratio | $I_{IFS}$ = 0.5 mA ÷ 16; | | 14.4 | 16 | 17.6 | - |
| **Output drivers** | | | | | | | |
| $I_{source(GH)}$ | source current on pin GH | high side; $V_{DD(float)}$ = 11.2 V; $V_{SH}$ = 0 V; $V_{GH}$ = 0 V | | - | 300 | - | mA |
| $I_{sink(GH)}$ | sink current on pin GH | high side; $V_{DD(float)}$ = 11.2 V; $V_{SH}$ = 0 V; $V_{GH}$ = 11.2 V | | - | 480 | - | mA |
| $I_{source(GL)}$ | source current on pin GL | low side; $V_{GL}$ = 0 V | | - | 300 | - | mA |
| $I_{sink(GL)}$ | sink current on pin GL | low side; $V_{GL}$ = 13 V | | - | 580 | - | mA |
| $V_{OH}$ | HIGH-level output voltage | pin GH; high side; $V_{DD(float)}$ = 11.2 V; $V_{SH}$ = 0 V; $I_{GH}$ = 10 mA | | - | 10.9 | - | V |
| | | pin GL; low side; $I_{GL}$ = 10 mA | | - | 12.6 | - | V |
| $V_{OL}$ | LOW-level output voltage | pin GH; high side; $V_{DD(float)}$ = 11.2 V; $V_{SH}$ = 0 V; $I_{GH}$ = 10 mA | | - | 0.17 | - | V |
| | | pin GL; low side; $I_{GL}$ = 10 mA | | - | 0.18 | - | V |
| $V_{Fd(bs)}$ | bootstrap diode forward voltage | $I_O$ = 5 mA | | 1.3 | 1.6 | 1.9 | V |
| **Shut-down input pin SD** | | | | | | | |
| $I_I$ | input current | $V_{SD}$ = 2.33 V | | - | - | 0.5 | µA |
| $V_{th(SD)}$ | threshold voltage on pin SD | | | 2.26 | 2.33 | 2.40 | V |
| **Error amplifier pins P, VCO** | | | | | | | |
| $I_{I(cm)}$ | common-mode input current | $V_{I(cm)}$ = 1 V | | - | –0.1 | –0.5 | µA |
| $V_{I(cm)}$ | common-mode input voltage | | | - | - | 2.5 | V |
| $V_{I(offset)}$ | offset input voltage | $V_{I(cm)}$ = 1 V; $I_{VCO}$ = –10 mA | | –2 | 0 | +2 | mV |
| $g_m$ | transconductance | $V_{I(cm)}$ = 1 V; source only | | - | 330 | - | µA/mV |
| $G_{ol}$ | open-loop gain | $R_L$ = 10 kΩ to GND; $V_{I(cm)}$ = 1 V | | - | 70 | - | dB |
| GB | gain bandwidth product | $R_L$ = 10 kΩ to GND; $V_{I(cm)}$ = 1 V | | - | 5 | - | MHz |
| $V_{VCO(max)}$ | maximum VCO voltage | operating; $R_L$ = 10 kΩ to GND | | 3.2 | 3.6 | 4.0 | V |
| $I_{VCO(max)}$ | maximum VCO current | operating; $V_{VCO}$ = 1 V | | –0.4 | –0.5 | –0.6 | mA |
| $V_{VCO(start)}$ | start VCO voltage | $I_{VCO}$ = 0.3 mA | | 2.5 | 2.7 | 2.9 | V |

**Table 5. Characteristics** *...continued*

*All voltages are referred to the ground pins which must be connected externally; positive currents flow into the IC; $V_{DD}$ = 13 V and $T_{amb}$ = 25 °C; tested using the circuit shown in Figure 7, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Reset pin** | | | | | | |
| $V_{rst}$ | reset voltage | | 2.15 | 2.4 | 2.65 | V |
| $V_{rst(hys)}$ | hysteresis of reset voltage | | - | 0.65 | - | V |
| $I_{I(rst)}$ | reset input current | | - | - | 1 | µA |
| **CSS pin** | | | | | | |
| $I_{start(soft)}$ | soft start current | | 12 | 15 | 18 | µA |
| **CT pin** | | | | | | |
| $I_{ch}$ | charge current | | 21 | 27 | 33 | µA |
| $I_{dch}$ | discharge current | | 8 | 10 | 12 | µA |
| $I_{leak}$ | leakage current | | 0.1 | 0.3 | 1 | µA |
| $I_{ch}/I_{dch}$ | charge current to discharge current ratio | | 2.4 | 2.7 | 3.0 | µA |
| $V_{trip(H)(CT)}$ | HIGH-level trip voltage on pin CT | | 2.7 | 3 | 3.3 | V |
| $V_{trip(L)(CT)}$ | LOW-level trip voltage on pin CT | | 0.6 | 0.7 | 0.8 | V |
| **OCP pin** | | | | | | |
| $V_{ref(OCP)}$ | reference voltage on pin OCP | | 280 | 305 | 330 | mV |
| **OTP** | | | | | | |
| $T_{otp(act)}$ | activation overtemperature protection temperature | | 120 | 135 | 150 | °C |
| **BO pin** | | | | | | |
| $V_{trip(bo)}$ | brownout trip voltage | | 1.19 | 1.25 | 1.31 | V |
| $I_{bo(hys)}$ | hysteresis of brownout current | | 14 | 16 | 18 | µA |
| **BURST pin** | | | | | | |
| $V_{ref(BURST)}$ | reference voltage on pin BURST | | 1.75 | 1.8 | 1.85 | V |
| **PFC pin** | | | | | | |
| $I_{leak}$ | leakage current | $V_{PFC}$ = 1 V | - | - | 1 | µA |
| $V_{sat}$ | saturation voltage | $I_{PFC}$ = 1 mA | - | - | 0.2 | V |
| **HYST pin** | | | | | | |
| $I_{leak}$ | leakage current | $V_{HYST}$ = 5 V | - | - | 1 | µA |

[1] The supply current $I_{DD}$ increases with the increasing bridge frequency to drive the capacitive load of two MOSFETs. Typical MOSFETs for the TEA1612T application are 8N50 (NXP type PHX80N50E, $Q_{G(tot)}$ = 55 nC (typ) and these will increase the supply current at 150 kHz according to the following formula: $\Delta I_{DD} = 2 \times Q_{G(tot)} \times f_{bridge} = 2 \times 55nC \times 150kHz = 16.5mA$

[2] The frequency of the oscillator depends on the value of capacitor $C_f$, the peak-to-peak voltage swing $V_{CF}$ and the charge/discharge currents $I_{ch(CF)}$ and $I_{dch(CF)}$.

## 11. Application information

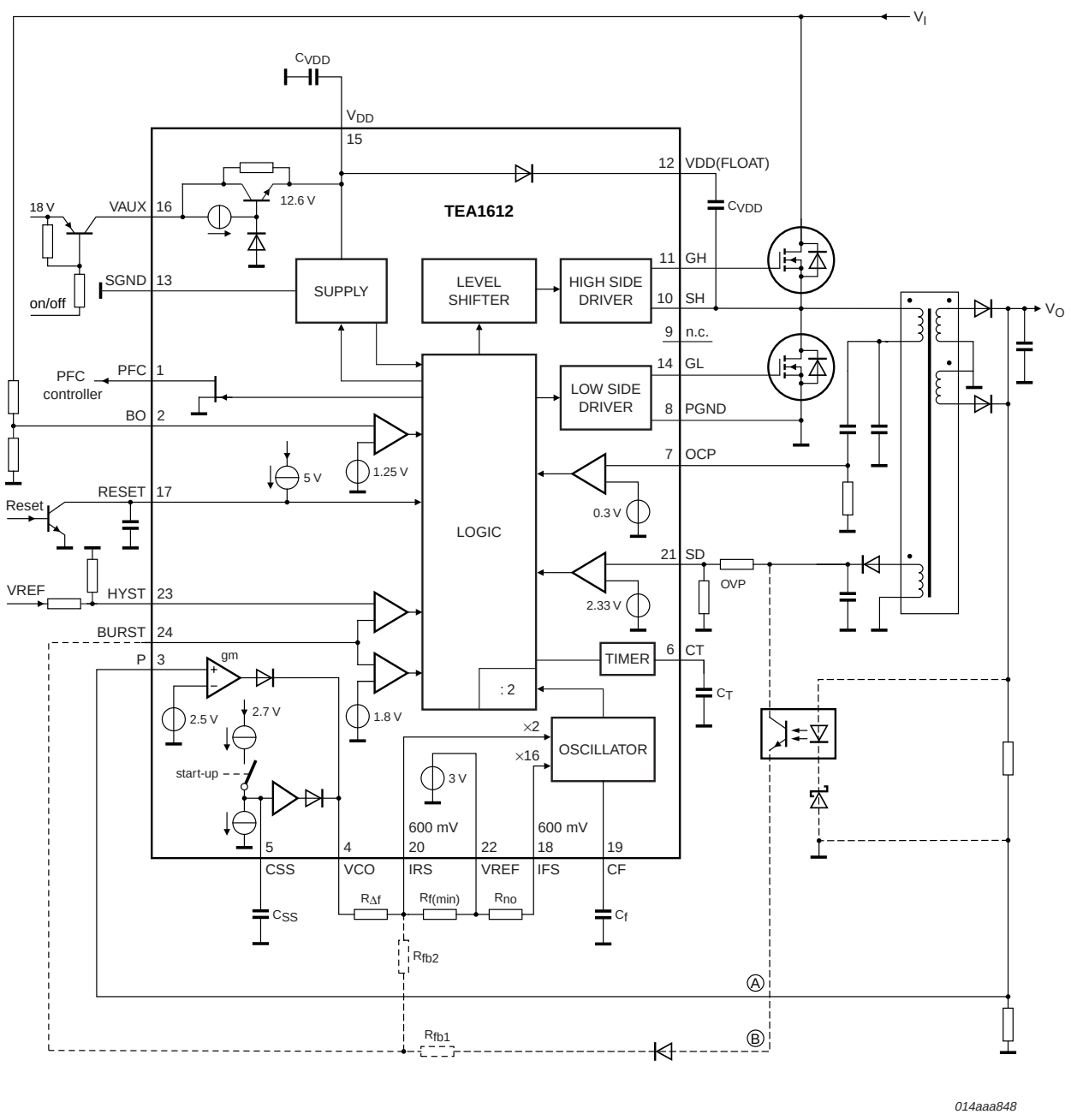
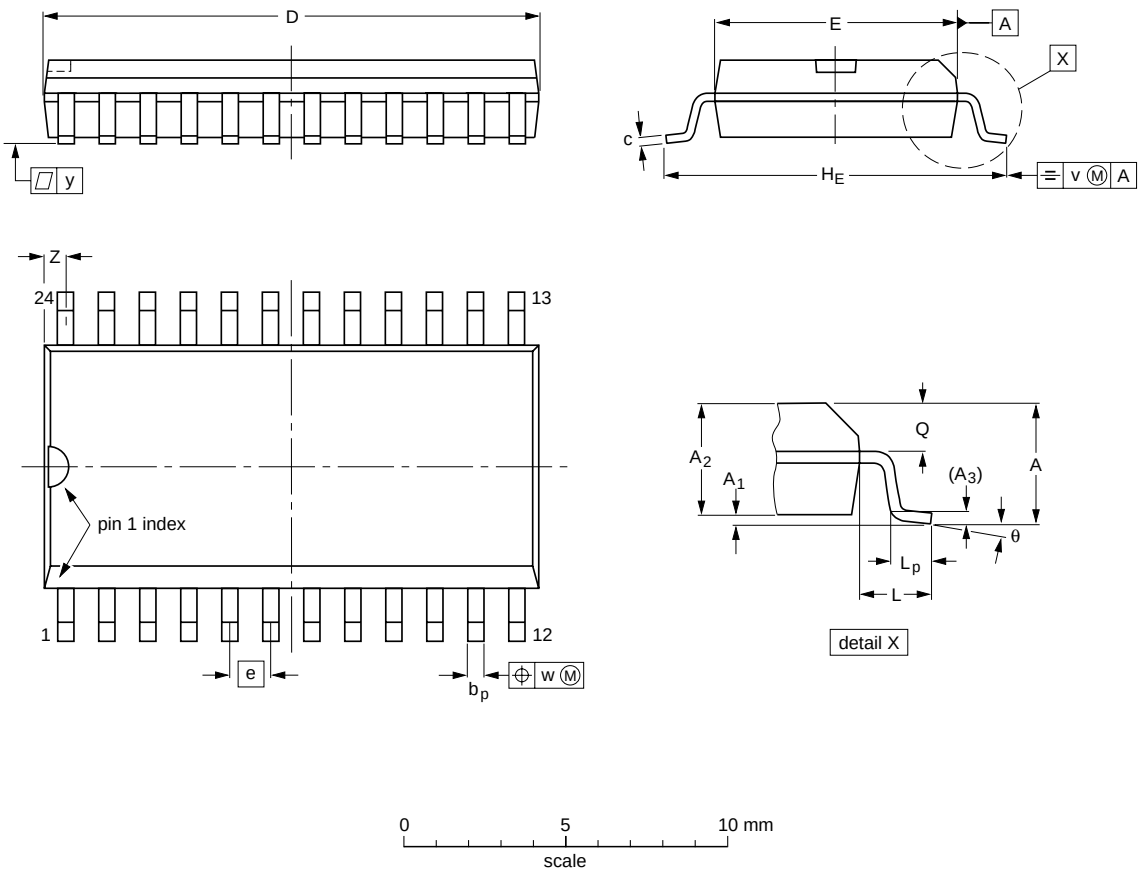



**Fig 7. Application diagram**

## 12. Package outline

**SO24: plastic small outline package; 24 leads; body width 7.5 mm** **SOT137-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.65 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.49<br>0.36 | 0.32<br>0.23 | 15.6<br>15.2 | 7.6<br>7.4 | 1.27 | 10.65<br>10.00 | 1.4 | 1.1<br>0.4 | 1.1<br>1.0 | 0.25 | 0.25 | 0.1 | 0.9<br>0.4 | $8^o$<br>$0^o$ |
| inches | 0.1 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60 | 0.30<br>0.29 | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT137-1 | 075E05 | MS-013 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT137-1 (SO24)**

## 13. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TEA1612T_1 | 20090924 | Product data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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## 16. Contents





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