TEA1750

GreenChip III SMPS control IC

Rev. 01 — 6 April 2007

Product data sheet

1. General description

The GreenChip III is the third generation of green Switched Mode Power Supply (SMPS) controller ICs. The TEA1750 combines a controller for Power Factor Correction (PFC) and a flyback controller. Its high level of integration allows the design of a cost-effective power supply with a very low number of external components.

The special built-in green functions provide high efficiency at all power levels. This applies to quasi-resonant operation at high power levels, quasi-resonant operation with valley skipping, as well as to reduced frequency operation at lower power levels. At low power levels, the PFC switches over to burst mode control to maintain high efficiency. In burst mode, soft-start and soft-stop functions are added to eliminate audible noise.

During low power conditions, the flyback controller switches to frequency reduction mode and limits the peak current to 25 % of its maximum value. This will ensure high efficiency at low power and good standby power performance while minimizing audible noise from the transformer.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified universal mains voltage in an effective and green way. A second low voltage Silicon On Insulator (SOI) IC is used for accurate, high speed protection functions and control.

The TEA1750 enables highly efficient and reliable supplies with power requirements up to 250 W, to be designed easily and with the minimum number of external components.

2. Features

2.1 Distinctive features

- Integrated PFC and flyback controller
- Universal mains supply operation (70 V AC to 276 V AC)
- High level of integration, resulting in a very low external component count and a cost-effective design

2.2 Green features

- On-chip start-up current source

2.3 PFC green features

- Valley/zero voltage switching for minimum switching losses (patented)
- Frequency limitation to reduce switching losses
- Burst mode operation if a low load is detected at the flyback output (patented)

2.4 Flyback green features

- Valley switching for minimum switching losses (patented)
- Frequency reduction with fixed minimum peak current at low power operation to maintain high efficiency at low output power levels

2.5 Protection features

- Safe restart mode for system fault conditions
- Continuous mode protection by means of demagnetization detection for both converters (patented)
- Undervoltage protection (foldback during overload)
- Accurate OverVoltage Protection (OVP) for both converters (adjustable for flyback converter)
- Open control loop protection for both converters
- IC overtemperature protection
- Low and adjustable OverCurrent Protection (OCP) trip level for both converters
- Soft (re)start for both converters
- Soft stop PFC to minimize audible noise
- Mains undervoltage protection / brown-out protection
- General purpose input for latched protection, e.g. to be used for system OverTemperature Protection (OTP)

3. Applications

- The device can be used in all applications that require an efficient and cost-effective power supply solution up to 250 W. Notebook adapters in particular can benefit from the high level of integration.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1750T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Block diagram

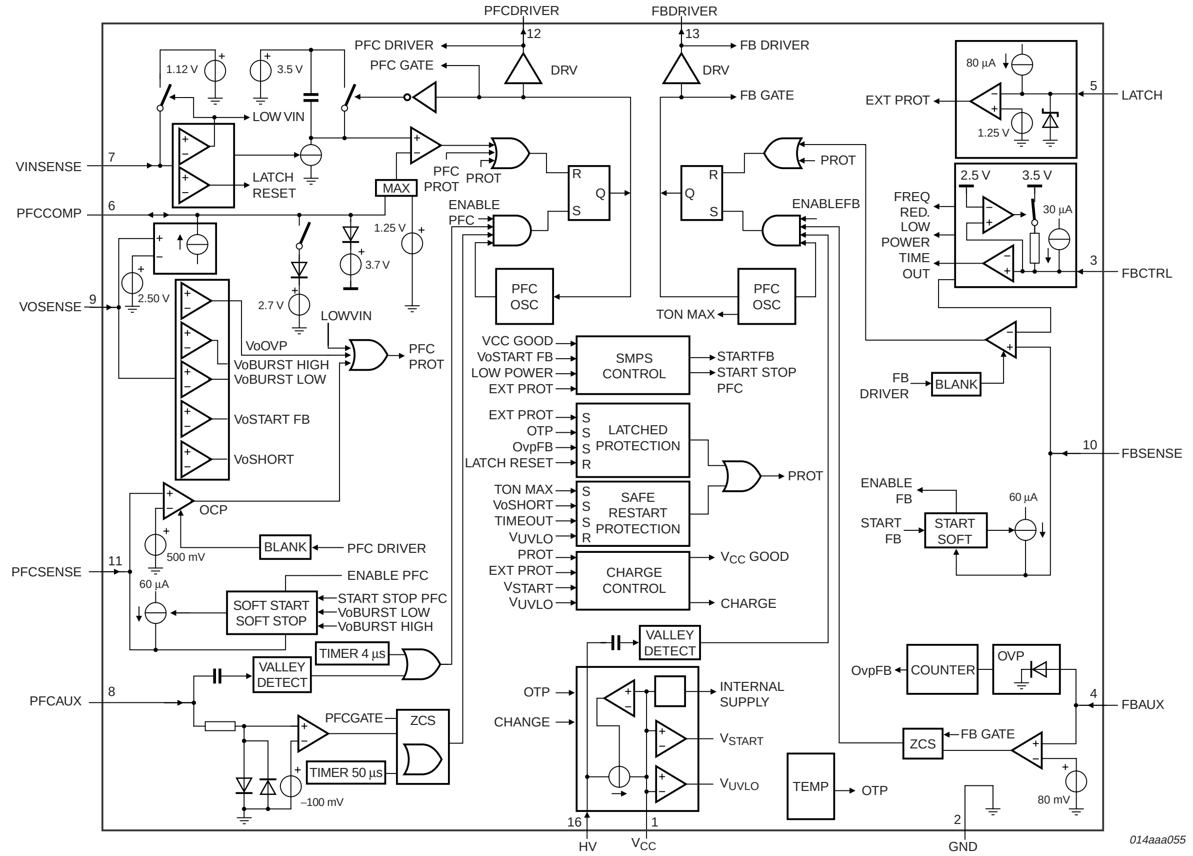


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

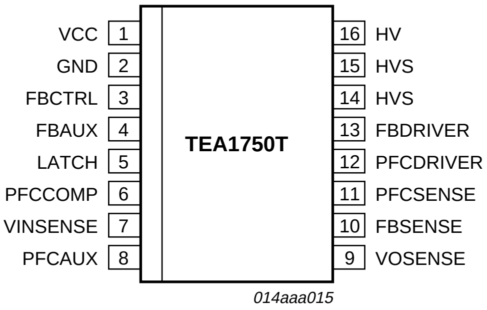


Fig 2. Pin configuration for TEA1750T (SOT109-1)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
GND	2	ground
FBCTRL	3	control input for flyback
FBAUX	4	input from auxiliary winding for demagnetization timing and overvoltage protection for flyback
LATCH	5	general purpose protection input
PFCCOMP	6	frequency compensation pin for PFC
VINSENSE	7	sense input for mains voltage
PFCAUX	8	input from auxiliary winding for demagnetization timing for PFC
VOSENSE	9	sense input for PFC output voltage
FBSENSE	10	programmable current sense input for flyback
PFCSENSE	11	programmable current sense input for PFC
PFCDRIVER	12	gate driver output for PFC
FBDRIVER	13	gate driver output for flyback
HVS	14, 15	high voltage safety spacer, not connected
HV	16	high voltage start-up and valley sensing of flyback part

7. Functional description

7.1 General control

The TEA1750 contains a controller for a power factor correction circuit as well as a controller for a flyback circuit. A typical configuration is shown in Figure 3.

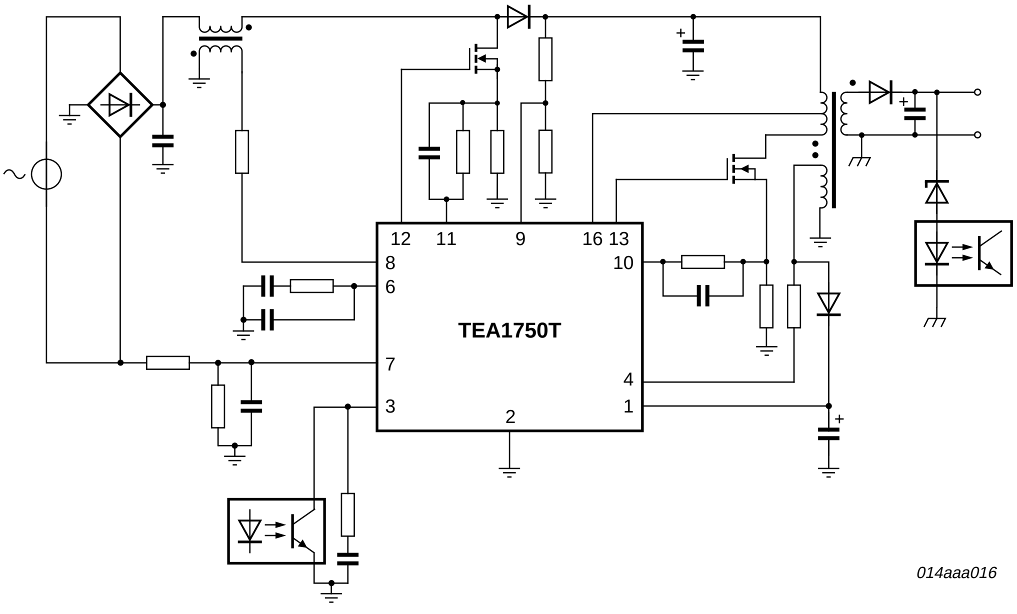


Fig 3. Typical configuration of TEA1750

7.1.1 Start-up and undervoltage lock-out

Initially the capacitor on the V_{CC} pin is charged from the high voltage mains via the HV pin.

As long as V_{CC} is below V_{trip}, the charge current is low. This protects the IC in case the V_{CC} pin is shorted to ground. For a short start-up time the charge current above V_{trip} is increased until V_{CC} reaches $V_{th(UVLO)}$. If V_{CC} is between $V_{th(UVLO)}$ and $V_{startup}$, the charge current is low again, ensuring a low duty cycle during fault conditions.

The control logic activates the internal circuitry and switches off the charge current when the voltage on pin V_{CC} passes the $V_{startup}$ level. First, the LATCH pin output is activated and the soft-start capacitors on the PFCSENSE and FBSENSE pins are charged. When the LATCH pin voltage exceeds the $V_{en(LATCH)}$ voltage and the soft-start capacitor on the PFCSENSE pin is charged, the PFC circuit is activated. The supply current from the HV pin is then switched on again and the PFC circuit charges the C_{bus} capacitor. When the voltage on pin VOSENSE reaches the $V_{start(fb)}$ level, the charge current is switched off and the flyback converter is activated (providing the soft-start capacitor on the FBSENSE pin is charged). The output voltage of the flyback converter is then regulated to its nominal output voltage. The IC supply is taken over by the auxiliary winding of the flyback converter. See Figure 4.

When the PFC is started, there is initially no supply take-over from the auxiliary winding. To make a small V_{CC} capacitor possible, the V_{CC} voltage is regulated to the $V_{startup}$ level, as long as the flyback converter has not yet started. Regulation is done by hysteretic control with a limited (high level) charge current. The hysteresis is typically 300 mV.

If during start-up the LATCH pin does not reach the $V_{en(LATCH)}$ level before V_{CC} reaches $V_{th(UVLO)}$, the LATCH pin output is de-activated and the charge current is switched on again.

As soon as the flyback converter is started, the voltage on the FBCTRL pin is monitored. If the output voltage of the flyback converter does not reach its intended regulation level in a predefined time, the voltage on the FBCTRL pin reaches the $V_{to(FBCTRL)}$ level and an error is assumed. The TEA1750 then initiates a safe restart.

When one of the protection functions is activated, both converters stop switching and the V_{CC} voltage drops to $V_{th(UVLO)}$. A latched protection recharges the V_{CC} capacitor via the HV pin, but does not restart the converters. For a safe-restart protection, the capacitor is recharged via the HV pin and the device restarts (see Figure 1)

In the event of an overvoltage protection of the PFC circuit (V_I on pin VOSENSE > $V_{ovp(VOSENSE)}$), only the PFC controller stops switching until the VOSENSE pin voltage drops below $V_{ovp(VOSENSE)}$ again. Also, if a mains undervoltage is detected (V_I on pin VINSENSE < $V_{stop(VINSENSE)}$), only the PFC controller stops switching until V_I on pin VINSENSE > $V_{start(VINSENSE)}$ again.

When the voltage on pin V_{CC} drops below the undervoltage lock-out level, both controllers stop switching and re-enter the safe restart mode. In the safe restart mode the driver outputs are disabled and the V_{CC} pin voltage is recharged via the HV pin.

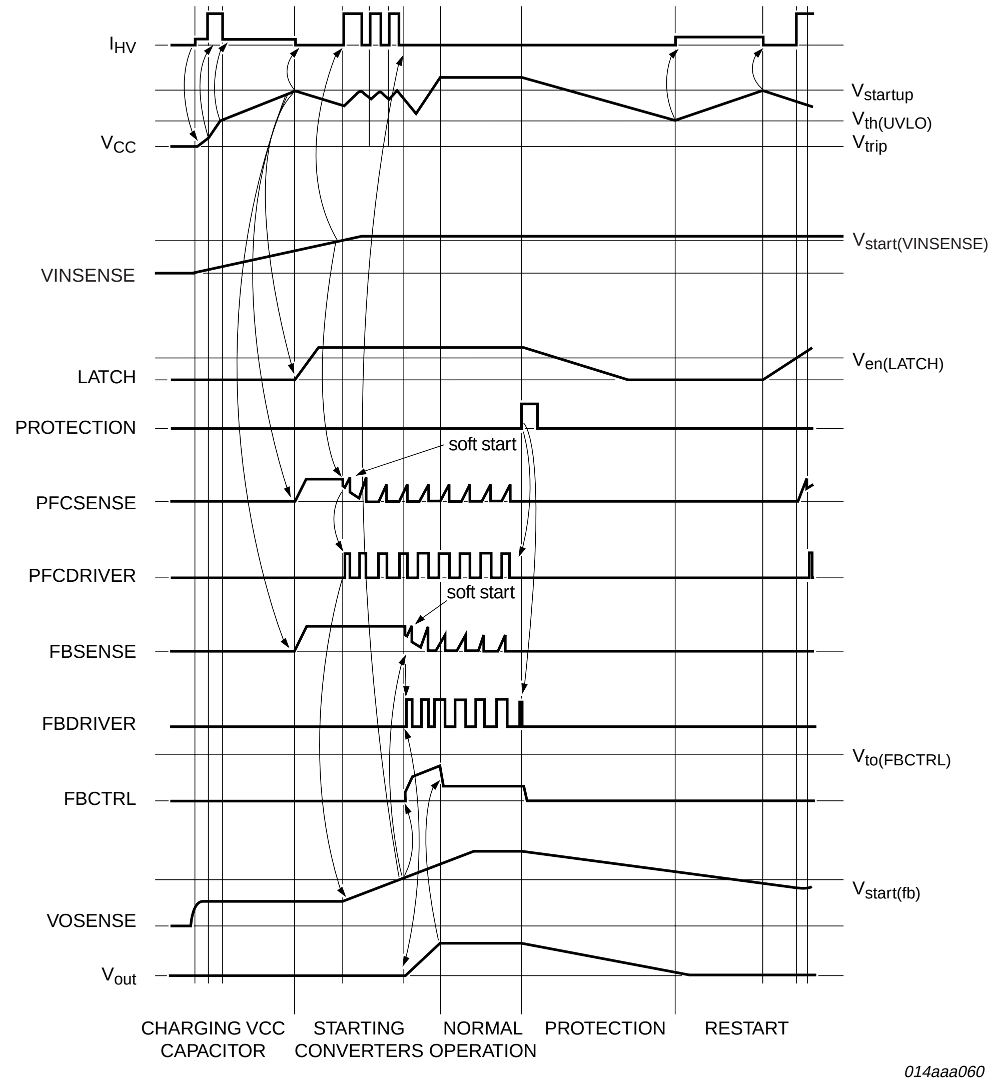


Fig 4. Start-up sequence, normal operation, and re-start sequence

7.1.2 Supply management

All internal reference voltages are derived from a temperature compensated and trimmed on-chip band gap circuit. Internal reference currents are derived from a temperature compensated and trimmed on-chip current reference circuit.

7.1.3 Latch input

Pin LATCH is a general purpose input pin, which can be used to switch off both converters. The pin sources a current, $I_{O(LATCH)}$ on pin LATCH (typ. 80 μA). Switching of both converters is stopped as soon as the voltage on this pin drops below 1.25 V.

At initial start-up, switching is inhibited until the voltage on the LATCH pin is above 1.35 V (typ.). No internal filtering is done on this pin. An internal Zener clamp of 2.7 V (typ.) protects this pin from excessive voltages.

7.1.4 Fast latch reset

In a typical application, the mains can be interrupted briefly to reset the latched protection. The PFC bus capacitor, C_{bus}, does not have to discharge for this latched protection to reset.

Typically the PFC bus capacitor, C_{bus}, has to discharge for the V_{CC} to drop to this reset level. When the latched protection is set, the clamping circuit of the VINSENSE circuit is disabled (see also Section 7.2.8). As soon as the VINSENSE voltage drops below 750 mV (typ.) and then is raised to 870 mV (typ.), the latched protection is reset.

The latched protection will also be reset by removing both the voltage on pin V_{CC} and on pin HV.

7.1.5 Overtemperature protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC only stops switching. As long as OTP is active, the V_{CC} capacitor is not recharged from the HV mains. The OTP circuit is supplied from the HV pin if the V_{CC} supply voltage is not sufficient.

OTP is a latched protection. It can be reset by removing both the voltage on pin V_{CC} and on pin HV or by the fast latch reset function, see Section 7.1.4

7.2 Power factor correction circuit

The power factor correction circuit operates in quasi-resonant or discontinuous conduction mode with valley switching. The next primary stroke is only started when the previous secondary stroke has ended and the voltage across the PFC MOSFET has reached a minimum value. The voltage on the PFCAUX pin is used to detect transformer demagnetization and the minimum voltage across the external PFC MOSFET switch.

7.2.1 t_{on} control

The power factor correction circuit is operated in t_{on} control. The resulting mains harmonic reduction of a typical application is well within the class-D requirements.

7.2.2 Valley switching and demagnetization (PFCAUX pin)

The PFC MOSFET is switched on after the transformer is demagnetized. Internal circuitry connected to the PFCAUX pin detects the end of the secondary stroke. It also detects the voltage across the PFC MOSFET. The next stroke is started if the voltage across the PFC MOSFET is at its minimum in order to reduce switching losses and electromagnetic interference (EMI) (valley switching).

If no demagnetization signal is detected on the PFCAUX pin, the controller generates a zero current signal (ZCS), 50 μs (typ.) after the last PFC gate signal.

If no valley signal is detected on the PFCAUX pin, the controller generates a valley signal 4 μs (typ.) after demagnetization was detected.

To protect the internal circuitry, for example during lightning events, it is advisable to add a 5 kΩ series resistor to this pin. To prevent incorrect switching due to external disturbance, the resistor should be placed close to the IC on the printed circuit board.

For applications with high transformer ringing frequencies (after the secondary stroke), the PFCAUX pin should be connected via a capacitor and a resistor to the auxiliary winding. A diode must than be placed from the ground connection to the PFCAUX pin.

7.2.3 Frequency limitation

To optimize the transformer and minimize switching losses, the switching frequency is limited to $f_{sw(PFC)max}$. If the frequency for quasi-resonant operation is above the $f_{sw(PFC)max}$ limit, the system switches over to discontinuous conduction mode. Also here, the PFC MOSFET is only switched on at a minimum voltage across the switch (valley switching).

7.2.4 Mains voltage compensation (VINSENSE pin)

The mathematical equation for the transfer function of a power factor corrector contains the square of the mains input voltage. In a typical application this results in a low bandwidth for low mains input voltages, while at high mains input voltages the Mains Harmonic Reduction (MHR) requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA1750 contains a correction circuit. Via the VINSENSE pin the average input voltage is measured and the information is fed to an internal compensation circuit. With this compensation it is possible to keep the regulation loop bandwidth constant over the full mains input range, yielding a fast transient response on load steps, while still complying with class-D MHR requirements.

In a typical application, the bandwidth of the regulation loop is set by a resistor and two capacitors on the PFCCOMP pin.

7.2.5 Soft start-up (pin PFCSENSE)

To prevent audible transformer noise at start-up or during hiccup, the transformer peak current, I_{DM}, is increased slowly by the soft start function. This can be achieved by inserting R_{SS1} and C_{SS1} between pin PFCSENSE and current sense resistor, R_{SENSE1}. An internal current source charges the capacitor to $V_{PFCSENSE} = I_{start(soft)PFC} \times R_{SS1}$. The voltage is limited to $V_{start(soft)PFC}$.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS1} and C_{SS1}.

$$\tau_{SoftStart} = 3 \times R_{SS1} \times C_{SS1}$$

The charging current $I_{start(soft)PFC}$ flows as long as the voltage on pin PFCSENSE is below 0.5 V (typ.). If the voltage on pin PFCSENSE exceeds 0.5 V, the soft start current source starts limiting current $I_{start(soft)PFC}$. As soon as the PFC starts switching, the $I_{start(soft)PFC}$ current source is switched off; see Figure 5.

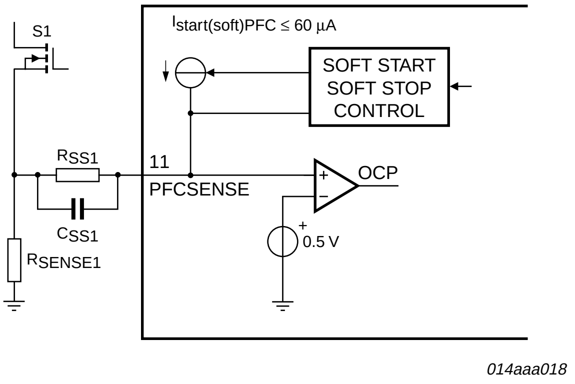


Fig 5. Soft start-up and soft stop of PFC

7.2.6 Burst mode control

When the output power of the flyback converter (see Section 7.3) is low, the flyback converter switches over to frequency reduction mode. When frequency reduction mode is entered by the flyback controller, the power factor correction circuit switches to burst mode control.

In burst mode control, switching of the power factor correction circuit is inhibited until the voltage on the VOSENSE pin has dropped to $V_{burst(L)}$. Switching then restarts with a soft-start to avoid audible noise (see Section 7.2.5). As soon as the voltage on the VOSENSE pin reaches $V_{burst(H)}$ the soft-stop circuit is activated, again to avoid audible noise. During the soft-stop time the output voltage of the power factor correction circuit overshoots, depending on the soft-start resistor and capacitor, R_{SS1} and $C_{SS1,}$ on the PFCSENSE pin. As the $V_{burst(H)}$ voltage is well below the $V_{reg(VOSENSE)}$ voltage, the PFC output voltage does not reach the normal operation output voltage of the power factor correction circuit in a typical application due to this overshoot.

The burst mode repetition rate is defined by the output power and the value of the bus capacitor, C_{bus}.

During burst mode operation the PFCCOMP pin is clamped between a voltage of 2.7 V (typ.) and 3.9 V (typ.). The lower clamp voltage limits the maximum power that is delivered during burst mode operation and yields a more sinusoidal input current during the burst pulse. The upper clamp voltage ensures that the PFC can return to its normal regulation point in a limited amount of time when returning from burst mode.

As soon as the flyback converter leaves frequency reduction mode, the power factor correction circuit restores normal operation. To prevent continuous on and off switching of the PFC circuit, a small hysteresis is built in (50 mV (typ.) on the FBCTRL pin).

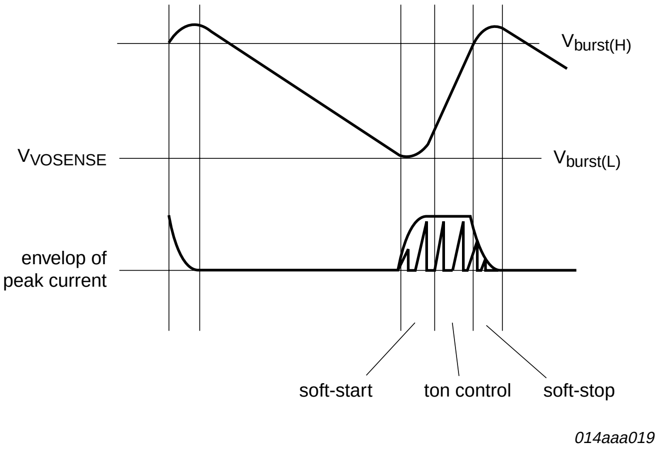


Fig 6. Burst mode control

7.2.7 Overcurrent protection (PFCSENSE pin)

The maximum peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor (R_{SENSE1}) on the source of the external MOSFET. The voltage is measured via the PFCSENSE pin.

7.2.8 Mains undervoltage lock-out / brown-out protection (VINSENSE pin)

To prevent the PFC from operating at very low mains input voltages, the voltage on the VINSENSE pin is sensed continuously. As soon as the voltage on this pin drops below the $V_{stop(VINSENSE)}$ level, switching of the PFC is stopped. If the low mains situation continues, the PFC bus voltage eventually drops. The voltage on the VOSENSE pin then drops below the $V_{start(fb)}$ level and the flyback converter is also disabled.

The voltage on pin VINSENSE is clamped to a minimum value, ($V_{start(VINSENSE)}$ − $\Delta V_{pu(VINSENSE)}$ for a fast restart as soon as the mains input voltage is restored after a mains dropout.

7.2.9 Overvoltage protection (VOSENSE pin)

To prevent output overvoltage during load steps and mains transients, an overvoltage protection circuit is built in.

As soon as the voltage on the VOSENSE pin exceeds the $V_{ovp(VOSENSE)}$ level, switching of the power factor correction circuit is inhibited. Switching of the PFC recommences as soon as the VOSENSE pin voltage drops below the $V_{ovp(VOSENSE)}$ level again.

When the resistor between pin VOSENSE and ground is open, the overvoltage protection is also triggered.

7.2.10 PFC open loop protection (VOSENSE pin)

The power factor correction circuit does not start switching until the voltage on the VOSENSE pin is above the $V_{th(ol)(VOSENSE)}$ level. This protects the circuit from open loop and VOSENSE short situations. As the VOSENSE pin draws a small input current, switching is also inhibited when the pin is left open.

7.2.11 Driver (pin PFCDRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 500 mA and a current sink capability of typically 1.2 A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

7.3 Flyback controller

The TEA1750 includes a controller for a flyback converter. The flyback converter operates in quasi-resonant or discontinuous conduction mode with valley switching. The auxiliary winding of the flyback transformer provides demagnetization detection and powers the IC after start-up.

7.3.1 Multi mode operation

The TEA1750 flyback controller can operate in multi modes; see Figure 7.

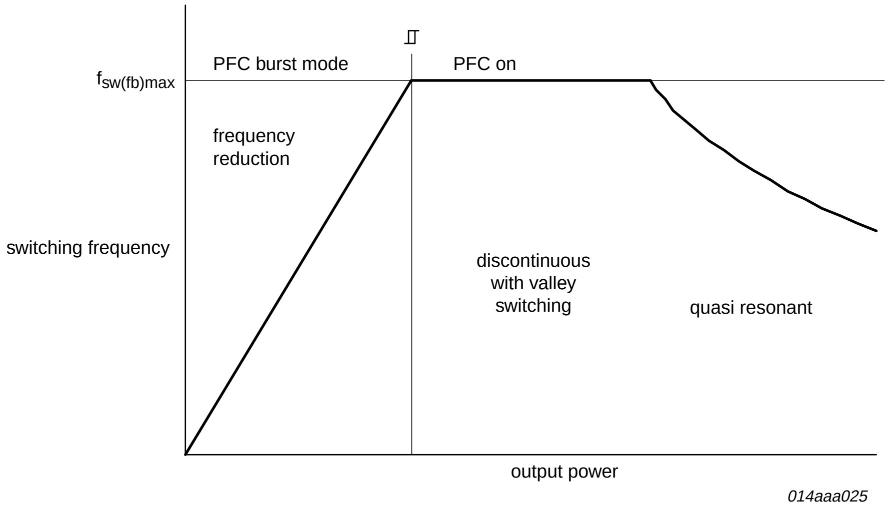


Fig 7. Multi mode operation flyback

At high output power the converter switches to quasi-resonant mode. The next converter stroke is started after demagnetization of the transformer current. In quasi-resonant mode switching losses are minimized as the converter only switches on when the voltage across the external MOSFET is at its minimum (valley switching, see also Section 7.3.2).

To prevent high frequency operation at lower loads, the quasi-resonant operation changes to discontinuous mode operation with valley skipping in which the switching frequency is limited for EMI to $f_{sw(fb)(max)}$ (125 kHz typ.). Again, the external MOSFET is only switched on when the voltage across the MOSFET is at its minimum.

At very low power and standby levels the frequency is controlled down by a voltage controlled oscillator (VCO). The minimum frequency can be reduced to zero. During frequency reduction mode, the primary peak current is kept at a minimal level of Ipkmax/4 to maintain a high efficiency. (Ipkmax is the maximum primary peak current set by the sense resistor and the maximum sense voltage.) As the primary peak current is low in frequency reduction mode operation (Ipk = Ipkmax/4), no audible noise is noticeable at switching frequencies in the audible range. Valley switching is also active in this mode.

In frequency reduction mode the PFC controller is switched to burst mode operation and the flyback maximum frequency changes linearly with the control voltage on the FBCTRL pin (see Figure 8). For stable on-off switching of the PFC burst mode, the FBCTRL pin has a 50 mV (typ.) hysteresis. At no load operation the switching frequency of the flyback can be reduced to (almost) zero.

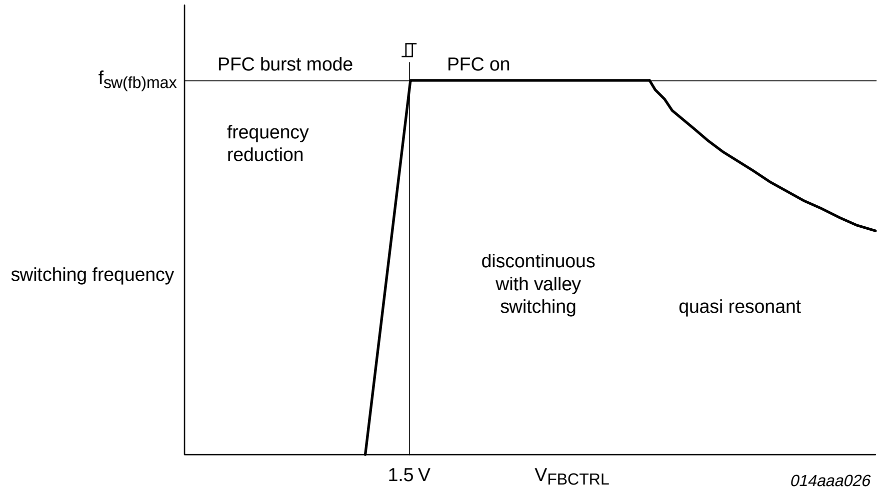


Fig 8. Frequency control of flyback part

7.3.2 Valley switching (HV pin)

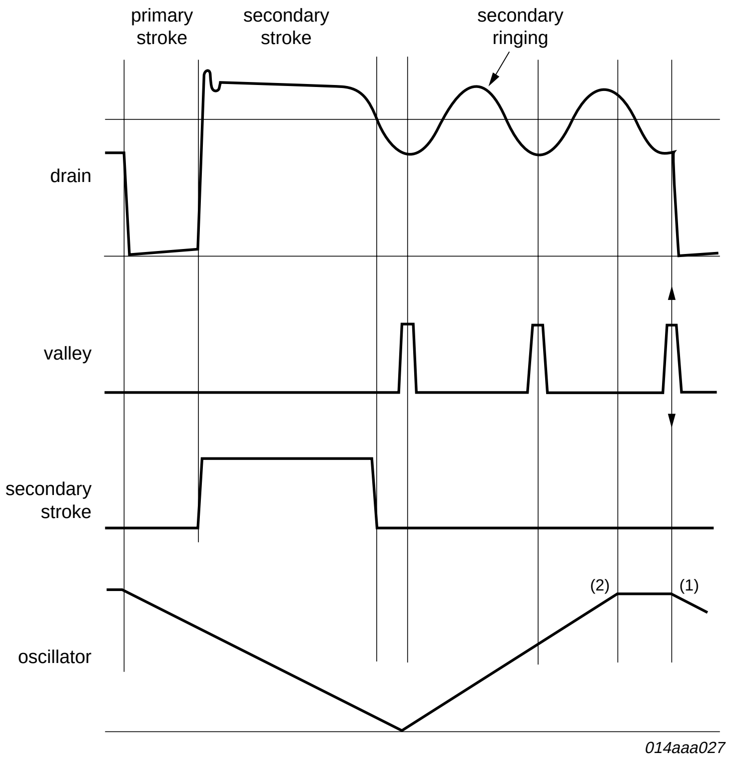
Refer to Figure 9. A new cycle starts when the external MOSFET is activated. After the on-time (determined by the FBSENSE voltage and the FBCTRL voltage), the MOSFET is switched off and the secondary stroke starts. After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)})}$

where L_p is the primary self inductance of the flyback transformer and C_d is the capacitance on the drain node.

As soon as the internal oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. Figure 9 shows the drain voltage, valley signal, secondary stroke signal and the internal oscillator signal.

Valley switching allows high frequency operation as capacitive switching losses are reduced, see Equation 1. High frequency operation makes small and cost-effective magnetics possible.

$$\left(P = \frac{1}{2} \times C_d \times V^2 \times f\right) \quad (1)$$



(1) Start of new cycle at lowest drain voltage.

(2) Start of new cycle in a classical Pulse Width Modulation (PWM) system without valley detection.

Fig 9. Signals for valley switching

7.3.3 Current mode control (FBSENSE pin)

Current mode control is used for the flyback converter for its good line regulation.

The primary current is sensed by the FBSENSE pin across an external resistor and compared with an internal control voltage.The internal control voltage is proportional to the FBCTRL pin voltage.

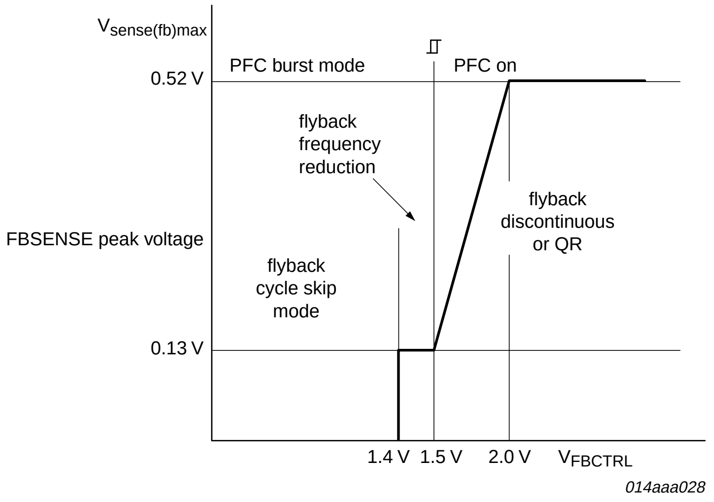


Fig 10. Frequency control of flyback part

The driver output is latched in the logic, preventing multiple switch-on.

7.3.4 Demagnetization (FBAUX pin)

The system is always in quasi-resonant or discontinuous conduction mode. The internal oscillator does not start a new primary stroke until the previous secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first $t_{sup(xfmr\_ring)}$ time (2 μs typ.). This suppression may be necessary at low output voltages and at start-up and in applications where the transformer has a large leakage inductance.

If pin FBAUX is open-circuit or not connected, a fault condition is assumed and the converter stops operating immediately. Operation restarts as soon as the fault condition is removed.

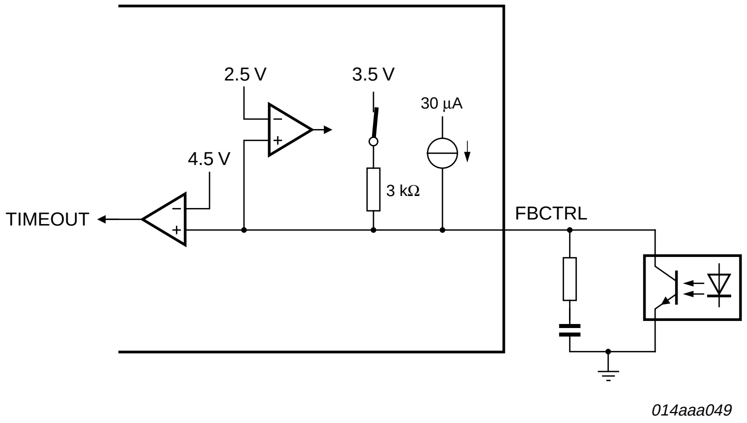
7.3.5 Flyback control / time-out (FBCTRL pin)

The pin FBCTRL is connected to an internal voltage source of 3.5 V via an internal resistor (typical resistance is 3 kΩ). As soon as the voltage on this pin is above 2.5 V (typ.), this connection is disabled. Above 2.5 V the pin is biased with a small current. When the voltage on this pin rises above 4.5 V (typ.), a fault is assumed and switching is inhibited.

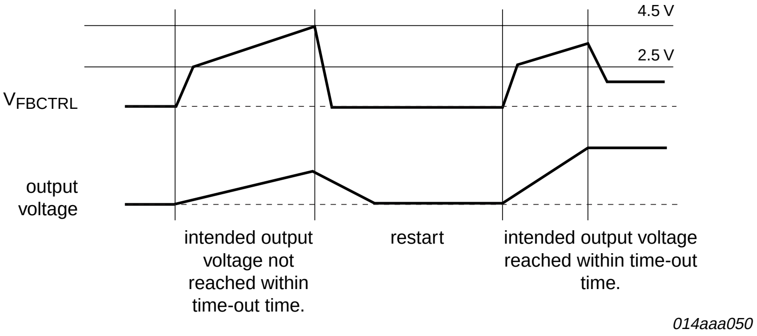
When a small capacitor is connected to this pin, a time-out function can be created to protect against an open control loop situation (see Figure 11 and Figure 12). The time-out function can be disabled by connecting a resistor (100 kΩ) to ground on the FBCTRL pin.

If the pin is shorted to ground, switching of the flyback controller is inhibited.

In normal operating conditions, when the converter is regulating the output voltage, the voltage on the FBCTRL pin is between 1.4 V and 2.0 V (typical values) from minimum to maximum output power.



a. Circuit diagram



b. Timing diagram

Fig 11. Time-out protection

7.3.6 Soft start-up (pin FBSENSE)

To prevent audible transformer noise during start-up, the transformer peak current, I_{DM} is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin FBSENSE and the current sense resistor.

An internal current source charges the capacitor to V = $I_{start(soft)(fb)}$ x R_{SS2}, with a maximum of approximately 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS2} and C_{SS2}.

$$\tau_{SoftStart} = 3 \times R_{SS2} \times C_{SS2}$$

The soft start current $I_{start(soft)(fb)}$ is switched on as soon as V_{CC} reaches $V_{startup}$. When the voltage on the VOSENSE pin reaches the $V_{start(fb)}$ level and the voltage on pin FBSENSE has reached 0.5 V, the flyback converter starts switching.

The soft start current flows as long as the voltage on pin FBSENSE is below approximately 0.5 V. If the voltage on pin FBSENSE exceeds 0.5 V, the soft start current source starts limiting the current. After the flyback converter has started, the soft start current source is switched off.

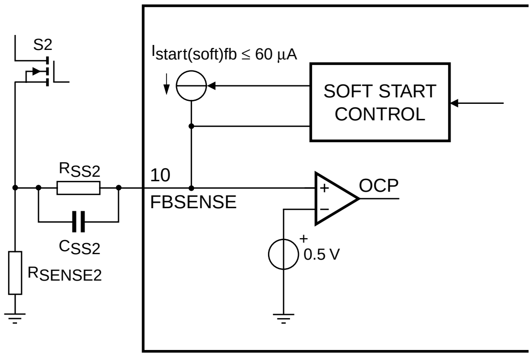


Fig 12. Soft start-up of flyback

7.3.7 Maximum on-time

The flyback controller limits the ‘on-time’ of the external MOSFET to 25 µs (typ.). When the ‘on-time’ is longer than 25 µs, the IC stops switching and enters the safe restart mode.

7.3.8 Overvoltage protection (FBAUX pin)

An output overvoltage protection is implemented in the GreenChip III series. This works for the TEA1750 by sensing the auxiliary voltage via the current flowing into pin FBAUX during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ElectroStatic Discharge (ESD) or lightning events. If the output voltage exceeds the OVP trip level a few times and not again in a subsequent cycle, the internal counter counts down at twice the speed it uses when counting up. However, when typically 8 cycles of subsequent OVP events are detected, the IC assumes a true OVP and the OVP circuit switches the power MOSFET off. As the protection is latched, the converter only restarts after the internal latch is reset. In a typical application the mains should be interrupted to reset the internal latch.

The output voltage $V_{ovp(FBAUX)}$ at which the OVP function trips, can be set by the demagnetization resistor, R_{FBAUX} :

$$V_{o(ovp)} = \frac{N_S}{N_{aux}}(I_{ovp(FBAUX)} \times R_{FBAUX} + V_{clamp(FBAUX)})$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer. Current $I_{ovp(FBAUX)}$ is internally trimmed.

The value of R_{FBAUX} can be adjusted to the turns ratio of the transformer, thus making an accurate OVP detection possible.

7.3.9 Overcurrent protection (FBSENSE pin)

The primary peak-current in the transformer is measured accurately cycle-by-cycle using the external sense resistor R_{SENSE2}. The OCP circuit limits the voltage on pin FBSENSE to an internal level (see also Section 7.3.3). The OCP detection is suppressed during the leading edge blanking period, t_{leb}, to prevent false triggering caused by switch-on spikes.

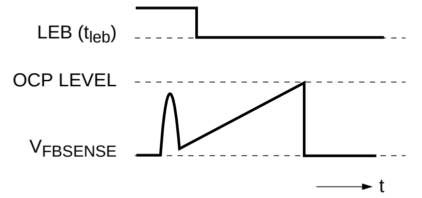


Fig 13. OCP leading edge blanking

7.3.10 Driver (pin FBDRIVER)

The driver circuit to the gate of the external power MOSFET has a current sourcing capability of typically 500 mA and a current sink capability of typically 1.2 A. This permits fast turn-on and turn-off of the power MOSFET for efficient operation.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{CC}	supply voltage		–0.4	+38	V
V_{LATCH}	voltage on pin LATCH	current limited	–0.4	+5	V
V_{FBCTRL}	voltage on pin FBCTRL		–0.4	+5	V
$V_{PFCCOMP}$	voltage on pin PFCCOMP		–0.4	+5	V
$V_{VINSENSE}$	voltage on pin VINSENSE		–0.4	+5	V
$V_{VOSENSE}$	voltage on pin VOSENSE		–0.4	+5	V
V_{PFCAUX}	voltage on pin PFCAUX		–25	+25	V
$V_{FBSENSE}$	voltage on pin FBSENSE	current limited	–0.4	+5	V
$V_{PFCSENSE}$	voltage on pin PFCSENSE	current limited	–0.4	+5	V
V_{HV}	voltage on pin HV		–0.4	+650	V
Currents					
I_{FBCTRL}	current on pin FBCTRL		–3	0	mA
I_{FBAUX}	current on pin FBAUX		–1	+1	mA
$I_{PFCSENSE}$	current on pin PFCSENSE		–1	+10	mA
$I_{FBSENSE}$	current on pin FBSENSE		–1	+10	mA
$I_{FBDRIVER}$	current on pin FBDRIVER	duty cycle < 10 %	–0.8	+2	A
$I_{PFCDRIVER}$	current on pin PFCDRIVER	duty cycle < 10 %	–0.8	+2	A
I_{HV}	current on pin HV		-	5	mA

Table 3. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
General					
P_{tot}	total power dissipation	$T_{amb} < 75$ °C	-	0.6	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
ESD					
V_{ESD}	electrostatic discharge voltage	class 1			
	human body model	pins 1 to 13 [1]	-	2000	V
		pin 16 (HV) [1]	-	1500	V
	machine model	[2]	-	200	V
	charged device model		-	500	V

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	124	K/W

10. Characteristics

Table 5. Characteristics

$T_{amb} = 25$ °C; $V_{CC} = 20$ V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin HV)						
I_{HV}	current on pin HV	$V_{HV} > 80$ V;				
		$V_{CC} < V_{trip}$; $V_{th(UVLO)} < V_{CC} < V_{startup}$	-	1	-	mA
		$V_{trip} < V_{CC} < V_{th(UVLO)}$	-	5.4	-	mA
		with auxiliary supply	8	20	40	µA
V_{BR}	breakdown voltage		650	-	-	V
Supply voltage management (pin V_{CC})						
V_{trip}	trip voltage		0.55	0.65	0.75	V
$V_{startup}$	start-up voltage		21	22	23	V
$V_{th(UVLO)}$	undervoltage lockout threshold voltage		14	15	16	V
$V_{start(hys)}$	hysteresis of start voltage	during start-up phase	-	300	-	mV
V_{hys}	hysteresis voltage	$V_{startup} - V_{th(UVLO)}$	6.3	7	7.7	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{ch(low)}$	low charging current	V_I on pin HV > 80 V; $V_{CC} < V_{trip}$ or $V_{th(UVLO)} < V_{CC} < V_{startup}$	−1.2	−1	−0.8	mA
$I_{ch(high)}$	high charging current	V_I on pin HV > 80 V; $V_{trip} < V_{CC} < V_{th(UVLO)}$	−6.3	−5.4	−4.6	mA
$I_{CC(oper)}$	operating supply current	no load on pin FBDRIVER and PFCDRIVER	2.25	3	3.75	mA
Input voltage sensing PFC (pin VINSENSE)						
$V_{stop(VINSENSE)}$	stop voltage on pin VINSENSE		0.86	0.89	0.92	V
$V_{start(VINSENSE)}$	start voltage on pin VINSENSE		1.11	1.15	1.19	V
$\Delta V_{pu(VINSENSE)}$	pull-up voltage difference on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	-	−100	-	mV
$I_{pu(VINSENSE)}$	pull-up current on pin VINSENSE	active after $V_{stop(VINSENSE)}$ is detected	−55	−47	−40	μA
$V_{mvc(VINSENSE)max}$	maximum mains voltage compensation voltage on pin VINSENSE		4.0	-	-	V
V_{flr}	fast latch reset voltage	active after $V_{th(UVLO)}$ is detected	-	0.75	-	V
$V_{flr(hys)}$	hysteresis of fast latch reset voltage		-	0.12	-	V
$I_{I(VINSENSE)}$	input current on pin VINSENSE	$V_{VINSENSE} > V_{stop(VINSENSE)}$ after $V_{start(VINSENSE)}$ is detected	5	33	100	nA
Loop compensation PFC(pin PFCCOMP)						
g_m	transconductance	$V_{VOSENSE}$ to $I_{O(PFCCOMP)}$	60	80	100	μA/V
$I_{O(PFCCOMP)}$	output current on pin PFCCOMP	$V_{VOSENSE}$ = 3.3 V	33	39	45	μA
		$V_{VOSENSE}$ = 2.0 V	−45	−39	−33	μA
$V_{clamp(PFCCOMP)}$	clamp voltage on pin PFCCOMP	low power mode, PFC in burst mode, lower clamp voltage [1]	2.5	2.7	2.9	V
		upper clamp voltage [1]	-	3.9	-	V
$V_{ton(PFCCOMP)zero}$	zero on-time voltage on pin PFCCOMP		3.4	3.5	3.6	V
$V_{ton(PFCCOMP)max}$	maximum on-time voltage on pin PFCCOMP		1.20	1.25	1.30	V
Pulse width modulator PFC						
$t_{on(PFC)}$	PFC on-time	$V_{VINSENSE}$ = 3.3 V, $V_{PFCCOMP} = V_{ton(max)(PFC)}$	3.6	4.5	5.0	μs
		$V_{VINSENSE}$ = 0.9 V, $V_{PFCCOMP} = V_{ton(max)(PFC)}$	30	40	53	μs

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output voltage sensing PFC (pin VOSENSE)						
$V_{th(ol)(VOSENSE)}$	open-loop threshold voltage on pin VOSENSE		0.35	0.40	0.45	V
$V_{start(fb)}$	flyback start voltage	[2]	-	1.72	-	V
$V_{stop(fb)}$	flyback stop voltage		1.55	1.60	1.65	V
$V_{burst(L)}$	LOW-level burst mode voltage		1.87	1.92	1.97	V
$V_{burst(H)}$	HIGH-level burst mode voltage		2.19	2.24	2.29	V
$V_{reg(VOSENSE)}$	regulation voltage on pin VOSENSE	$I_{O(PFCCOMP)} = 0$	2.475	2.500	2.525	V
$V_{ovp(VOSENSE)}$	overvoltage protection voltage on pin VOSENSE		2.60	2.63	2.67	V
$I_{I(VOSENSE)}$	input current on pin VOSENSE	$V_{VOSENSE}$ = 2.5 V	5	45	100	nA
Overcurrent protection PFC (pin PFCSENSE)						
$V_{sense(PFC)max}$	maximum PFC sense voltage	$\Delta V/\Delta t$ = 50 mV/µs	0.49	0.52	0.55	V
		$\Delta V/\Delta t$ = 200 mV/µs	0.51	0.54	0.57	V
$t_{leb(PFC)}$	PFC leading edge blanking time		250	310	370	ns
$I_{prot(PFCSENSE)}$	protection current on pin PFCSENSE		–50	-	–5	nA
Soft start, soft stop PFC (pin PFCSENSE)						
$I_{start(soft)PFC}$	PFC soft start current		–75	–60	–45	µA
$V_{start(soft)PFC}$	PFC soft start voltage		0.46	0.50	0.54	V
$V_{stop(soft)PFC}$	PFC soft stop voltage		0.42	0.45	0.48	V
$R_{start(soft)PFC}$	PFC soft start resistance		12	-	-	kΩ
Oscillator PFC						
$f_{sw(PFC)max}$	maximum PFC switching frequency		100	125	150	kHz
$t_{off(PFC)min}$	minimum PFC off-time		1.1	1.4	1.7	µs
Valley switching PFC (pin PFCAUX)						
$(\Delta V/\Delta t)_{vrec(PFC)}$	PFC valley recognition voltage change with time		-	-	1.7	V/µs
$t_{vrec(PFC)}$	PFC valley recognition time	V_{PFCAUX} = 1 V peak-peak [3]	-	-	300	ns
		demagnetization to $\Delta V/\Delta t = 0$ [4]	-	-	50	ns
$t_{to(vrec)PFC}$	PFC valley recognition time-out time		3	4	6	µs

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Demagnetization management PFC (pin PFCAUX)						
$V_{th(comp)PFCAUX}$	comparator threshold voltage on pin PFCAUX		–150	–100	–50	mV
$t_{to(demag)PFC}$	PFC demagnetization time-out time		40	50	60	µs
$I_{prot(PFCAUX)}$	protection current on pin PFCAUX	V_{PFCAUX} = 50 mV	–75	-	–5	nA
Driver (pin PFCDRIVER)						
$I_{src(PFCDRIVER)}$	source current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V	-	–0.5	-	A
$I_{sink(PFCDRIVER)}$	sink current on pin PFCDRIVER	$V_{PFCDRIVER}$ = 2 V	-	0.7	-	A
		$V_{PFCDRIVER}$ = 10 V	-	1.2	-	A
$V_{O(PFCDRIVER)max}$	maximum output voltage on pin PFCDRIVER		-	11	12	V
Overvoltage protection flyback (pin FBAUX)						
$I_{ovp(FBAUX)}$	overvoltage protection current on pin FBAUX		279	300	321	µA
$N_{cy(ovp)}$	number of overvoltage protection cycles		6	8	12	
Demagnetization management flyback (pin FBAUX)						
$V_{th(comp)FBAUX}$	comparator threshold voltage on pin FBAUX		60	80	110	mV
$I_{prot(FBAUX)}$	protection current on pin FBAUX	V_{FBAUX} = 50 mV	–50	-	–5	nA
$V_{clamp(FBAUX)}$	clamp voltage on pin FBAUX	I_{FBAUX} = –500 µA	–1.0	–0.8	–0.6	V
		I_{FBAUX} = 500 µA	0.5	0.7	0.9	V
$t_{sup(xfmr\_ring)}$	transformer ringing suppression time		1.5	2	2.5	µs
Pulse width modulator flyback						
$t_{on(fb)min}$	minimum flyback on-time		-	$t_{leb(fb)}$	-	ns
$t_{on(fb)max}$	maximum flyback on-time		20	25	30	µs
Oscillator flyback						
$f_{sw(fb)max}$	maximum flyback switching frequency		100	125	150	kHz
$V_{start(VCO)FBCTRL}$	VCO start voltage on pin FBCTRL		1.3	1.5	1.7	V
$V_{hys(FBCTRL)}$	hysteresis voltage on pin FBCTRL		-	60	-	mV
$\Delta V_{VCO(FBCTRL)}$	VCO voltage difference on pin FBCTRL		-	–0.1	-	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Peak current control flyback (pin FBCTRL)						
V_{FBCTRL}	voltage on pin FBCTRL	for maximum flyback peak current	1.85	2.0	2.15	V
$V_{to(FBCTRL)}$	time-out voltage on pin FBCTRL	enable voltage	-	2.5	-	V
		trip voltage	4.2	4.5	4.8	V
$R_{int(FBCTRL)}$	internal resistance on pin FBCTRL		-	3	-	kΩ
$I_{O(FBCTRL)}$	output current on pin FBCTRL	V_{FBCTRL} = 0 V	–1.4	–1.17	–0.93	mA
		V_{FBCTRL} = 2 V	–0.6	–0.5	–0.4	mA
$I_{to(FBCTRL)}$	time-out current on pin FBCTRL	V_{FBCTRL} = 2.6 V	–36	–30	–24	μA
		V_{FBCTRL} = 4.1 V	–34.5	–28.5	–22.5	μA
Valley switching flyback (pin HV)						
$(\Delta V/\Delta t)_{vrec(fb)}$	flyback valley recognition voltage change with time		–75	-	+75	V/μs
$t_{d(vrec-swon)}$	valley recognition to switch-on delay time	[5]	-	150	-	ns
Soft start flyback (pin FBSENSE)						
$I_{start(soft)fb}$	flyback soft start current		–75	–60	–45	μA
$V_{start(soft)fb}$	flyback soft start voltage		0.43	0.49	0.54	V
$R_{start(soft)fb}$	flyback soft start resistance		12	-	-	kΩ
Overcurrent protection flyback (pin FBSENSE)						
$V_{sense(fb)max}$	maximum flyback sense voltage	$\Delta V/\Delta t$ = 50 mV/μs	0.49	0.52	0.55	V
		$\Delta V/\Delta t$ = 200 mV/μs	0.52	0.55	0.58	V
$t_{leb(fb)}$	flyback leading edge blanking time		255	305	355	ns
Driver (pin FBDRIVER)						
$I_{src(FBDRIVER)}$	source current on pin FBDRIVER	$V_{FBDRIVER}$ = 2 V	-	–0.5	-	A
$I_{sink(FBDRIVER)}$	sink current on pin FBDRIVER	$V_{FBDRIVER}$ = 2 V	-	0.7	-	A
		$V_{FBDRIVER}$ = 10 V	-	1.2	-	A
$V_{O(FBDRIVER)(max)}$	maximum output voltage on pin FBDRIVER		-	11	12	V
Latch input (pin LATCH)						
$V_{prot(LATCH)}$	protection voltage on pin LATCH		1.23	1.25	1.27	V
$I_{O(LATCH)}$	output current on pin LATCH	$V_{prot(LATCH)} < V_{LATCH} < V_{oc(LATCH)}$	–85	–80	–75	μA
$V_{en(LATCH)}$	enable voltage on pin LATCH	at start-up	1.30	1.35	1.40	V
$V_{hys(LATCH)}$	hysteresis voltage on pin LATCH	$V_{en(LATCH)} - V_{prot(LATCH)}$	80	100	140	mV
$V_{oc(LATCH)}$	open-circuit voltage on pin LATCH		-	2.9	-	V

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
$T_{pl(IC)}$	IC protection level temperature		130	140	150	°C
$T_{pl(IC)hys}$	hysteresis of IC protection level temperature		-	10	-	°C

[1] For a typical application with a compensation network on pin PFCCOMP, like the example in Figure 3.

[2] Typically 120 mV above $V_{stop(fb)}$.

[3] Minimum required voltage change time for valley recognition on pin PFCAUX.

[4] Minimum required time between demagnetization recognition and ΔV/Δt end.

[5] Guaranteed by design.

11. Application information

A power supply with the TEA1750 consists of a power factor correction circuit followed by a flyback converter. See Figure 14.

Capacitor C_{VCC} buffers the IC supply voltage, which is powered via the high voltage rectified mains during start-up and via the auxiliary winding of the flyback converter during operation. Sense resistors R_{SENSE1} and R_{SENSE2} convert the current through the MOSFETs S1 and S2 into a voltage at pins PFCSENSE and FBSENSE. The values of R_{SENSE1} and R_{SENSE2} define the maximum primary peak current in MOSFETS S1 and S2. In the example given, the LATCH pin is connected to a Negative Temperature Coefficient (NTC) resistor. When the resistance drops below $\frac{V_{prot(LATCH)}}{I_{O(LATCH)}} = 15.6\ k\Omega$ (typ.), the protection is activated.

A capacitor $C_{TIMEOUT}$ is connected to the FBCTRL pin. For a 120 nF capacitor, typically after 10 ms the time-out protection is activated. R_{LOOP} is added so that the time-out capacitor does not interfere with the normal regulation loop.

R_{S1} and R_{S2} are added to prevent the soft-start capacitors from being charged during normal operation due to negative voltage spikes across the sense resistors.

Resistor R_{AUX1} is added to protect the IC from damage during lightning events. For applications with high transformer ringing frequencies (after the secondary stroke), the PFCAUX pin should be connected via a capacitor and a resistor to the auxiliary winding. A diode must than be placed from the ground connection to the PFCAUX pin.

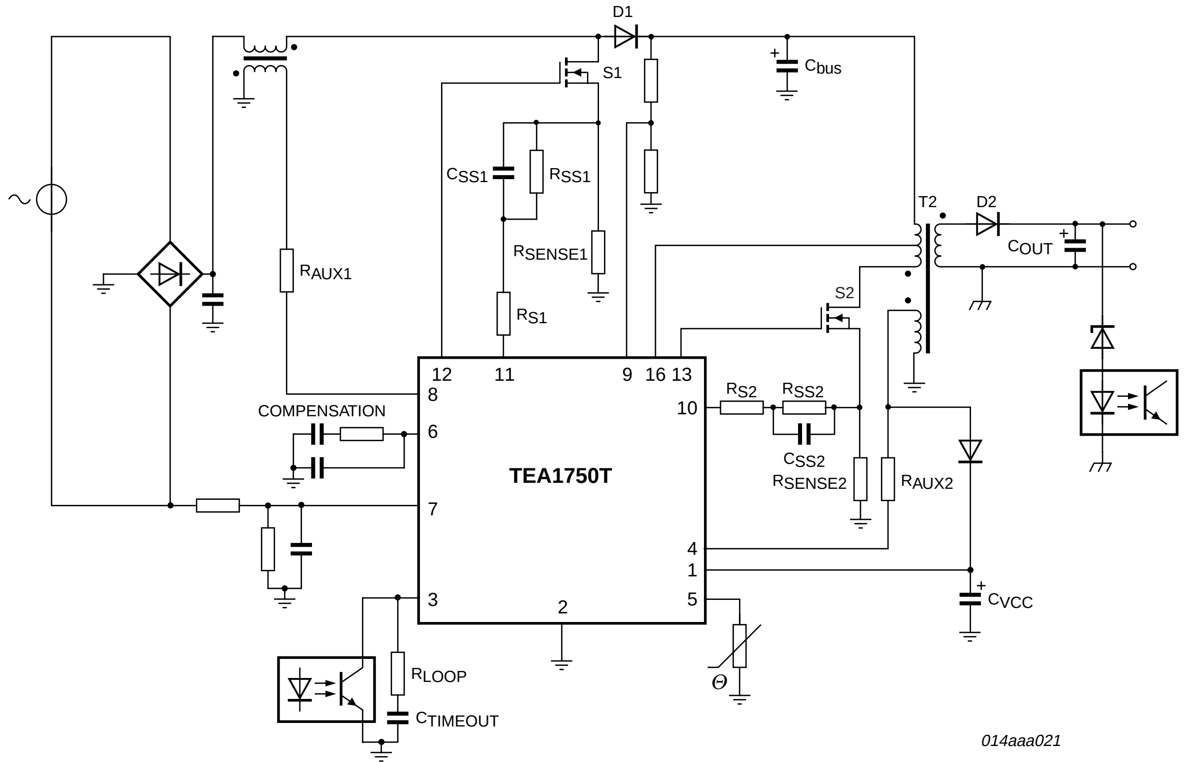


Fig 14. Typical application diagram of TEA1750

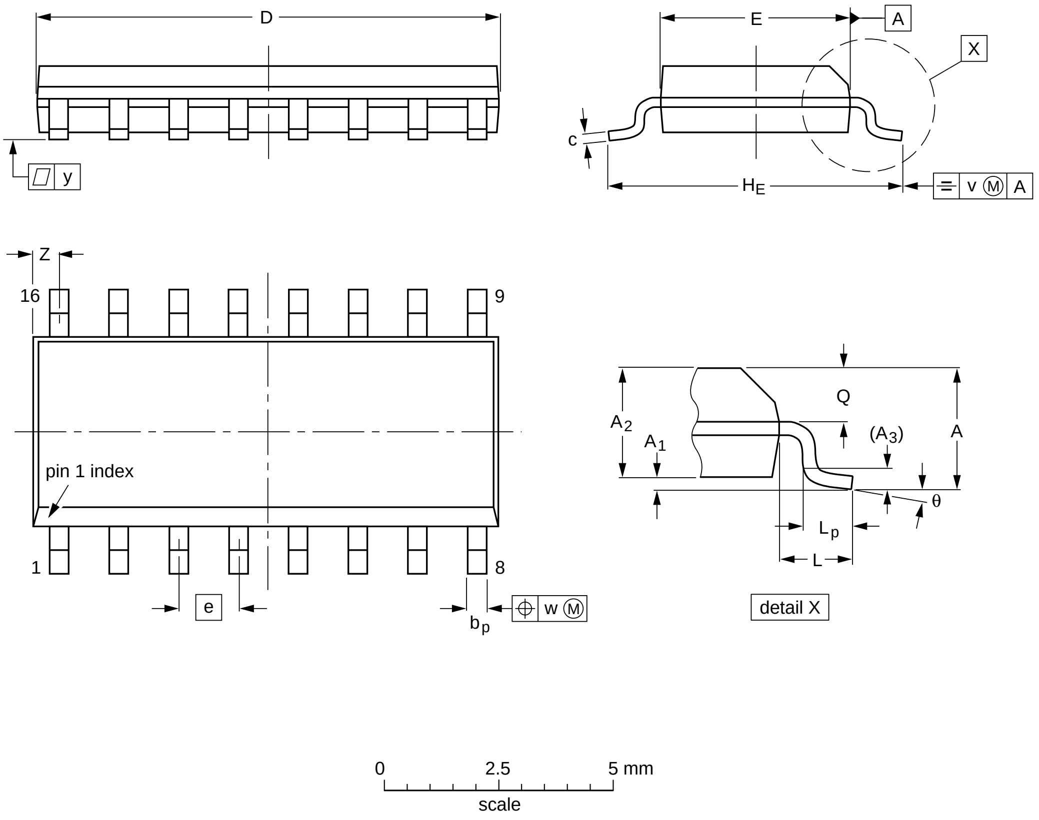
12. Test information

12.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT109-1 (SO16)

14. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1750_1	20070406	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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