# TEA1738T; TEA1738LT

GreenChip SMPS control IC

Rev. 2 — 14 January 2011 Product data sheet

## 1. General description

The TEA1738(L) is a low cost Switched Mode Power Supply (SMPS) controller IC intended for flyback topologies. The TEA1738(L) operates in peak current and frequency control mode. Frequency jitter has been implemented to reduce ElectroMagnetic Interference (EMI). Slope compensation is integrated for Continuous Conduction Mode (CCM) operation.

The TEA1738(L) IC includes OverPower Protection (OPP). This enables the controller to operate under overpower situations for a limited amount of time.

Two pins, VINSENSE and PROTECT, are reserved for protection purposes. Input UnderVoltage Protection (UVP), output OverVoltage Protection (OVP) and OverTemperature Protection (OTP) can be implemented using a minimal number of external components.

At low power levels the primary peak current is set to 25 % of the maximum peak current and the switching frequency is reduced to limit switching losses. The combination of fixed frequency operation at high output power and frequency reduction at low output power provides high efficiency over the total load range.

The TEA1738(L) enables low cost, highly efficient and reliable supplies for power requirements up to 75 W to be designed easily and with a minimum number of external components.

## 2. Features and benefits

### 2.1 Features

- SMPS controller IC enabling low-cost applications
- Large input voltage range (12 V to 30 V)
- Integrated OverVoltage Protection (OVP) on pin VCC
- Very low supply current during start-up and restart (10 μA typical)
- Low supply current during normal operation (0.55 mA typical without load)
- Overpower or high/low line compensation
- Adjustable overpower time-out
- Adjustable overpower restart timer
- Fixed switching frequency with frequency jitter to reduce EMI
- Frequency reduction at medium power operation to maintain high efficiency

- Frequency reduction with fixed minimum peak current at low power to maintain high efficiency at low output power levels
- Frequency increase at peak power operation
- Slope compensation for CCM operation
- Low and adjustable OverCurrent Protection (OCP) trip level
- Adjustable soft start
- Two protection inputs (e.g. for input UVP and OTP)
- IC overtemperature protection

## 3. Applications

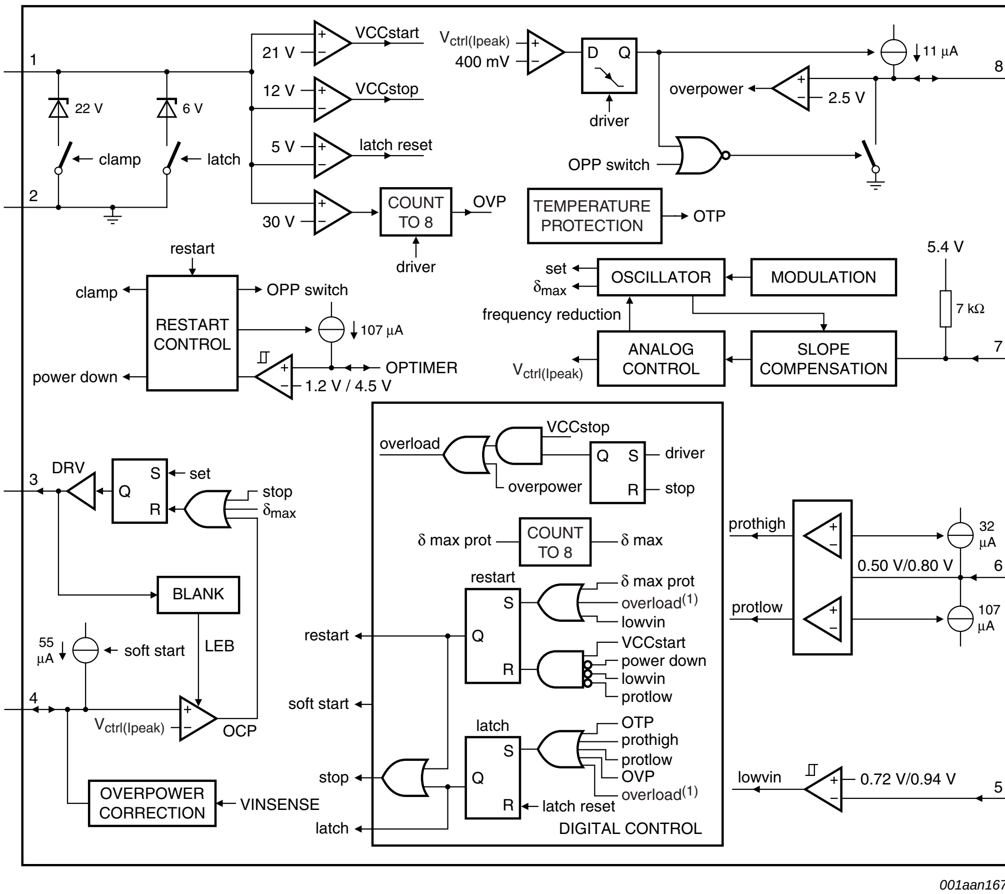
- All applications requiring efficient and cost-effective power supply solutions up to 75 W.

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TEA1738T | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| TEA1738LT | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |

# 5. Block diagram




(1) In the TEA1738LT the overload signal switches the IC to the latched-off state. In the TEA1738T the overload signal triggers the restart timer.

**Fig 1. Block diagram**

# 6. Pinning information

## 6.1 Pinning

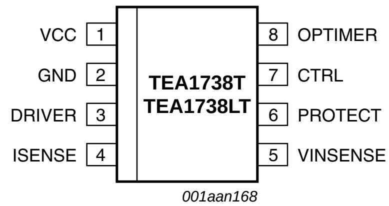



**Fig 2. Pin configuration: TEA1738(L) (SOT96-1)**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| VCC | 1 | supply voltage |
| GND | 2 | ground |
| DRIVER | 3 | gate driver output |
| ISENSE | 4 | current sense input |
| VINSENSE | 5 | input voltage protection input |
| PROTECT | 6 | general purpose protection input |
| CTRL | 7 | control input |
| OPTIMER | 8 | overpower and restart timer |

# 7. Functional description

## 7.1 General control

The TEA1738(L) contains a flyback circuit controller, a typical configuration of which is shown in Figure 3.

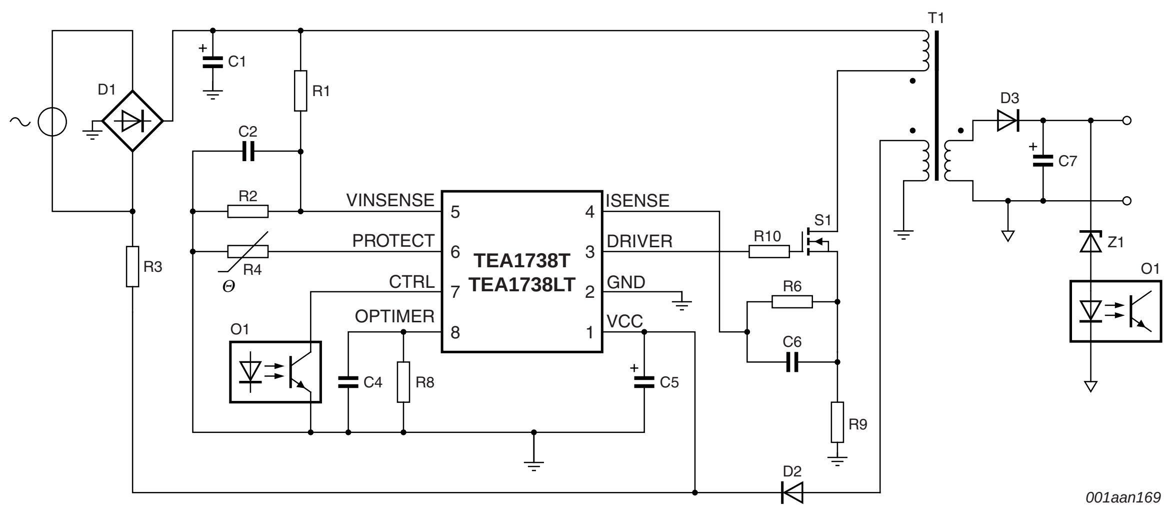



Fig 3. Typical configuration

## 7.2 Start-up and UnderVoltage LockOut (UVLO)

Initially, the capacitor on the VCC pin is charged from the high voltage mains via resistor R3.

If $V_{CC}$ is lower than $V_{startup}$, the IC current consumption is low (10 μA typical). When $V_{CC}$ reaches $V_{startup}$ the IC first waits for pin VINSENSE to reach the $V_{start(VINSENSE)}$ voltage and for pin PROTECT to reach the $V_{det(L)(PROTECT)}$ voltage. When both levels are reached, the IC charges the ISENSE pin to the $V_{start(soft)}$ level and starts switching. In a typical application the supply voltage is taken over by the auxiliary winding of the transformer.

If a protection is triggered the controller stops switching. Depending on the protection triggered it either causes a restart or latches the converter to an off-state.

A restart caused by a protection rapidly charges the OPTIMER pin to 4.5 V (typical). The TEA1738(L) enters Power-down mode until the OPTIMER pin discharges down to 1.2 V (typical). In Power-down mode, the IC consumes a very low supply current (10 μA typical) and the VCC pin is clamped at 22 V (typical) by an internal clamp circuit. When the voltage on pin OPTIMER drops below 1.2 V (typical) and the VCC pin voltage is above the VCC start-up voltage (see Figure 4), the IC restarts.

When a latched protection is triggered, the TEA1738(L) immediately enters Power-down mode. The VCC pin is clamped to a voltage just above the latch protection reset voltage ($V_{rst(latch)}$ + 1 V).

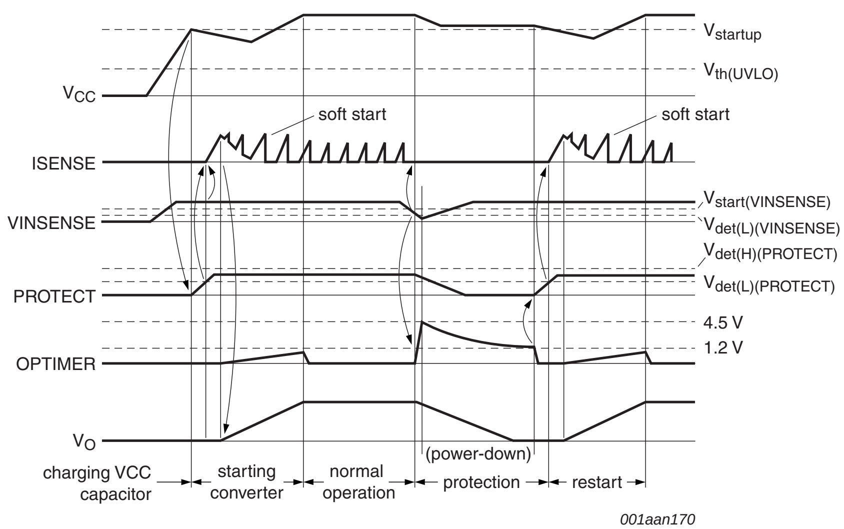



**Fig 4. Start-up sequence, normal operation and restart sequence**

When the voltage on pin VCC drops below the $V_{th(UVLO)}$ level during normal operation, the controller stops switching and the TEA1738T enters Restart mode. In Restart mode the driver output is disabled and the VCC pin voltage is recharged via resistor R3 to the rectified mains voltage. For the TEA1738LT a VCC undervoltage, which does not occur during a start-up event, latches the IC in an off-state.

## 7.3 Supply management

All internal reference voltages are derived from a temperature compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature compensated current reference circuit.

## 7.4 OverVoltage Protection (VCC pin)

An OVP circuit is connected to the VCC pin. After 8 consecutive OVP cycles the IC triggers the latched protection. When $V_{CC}$ drops below the $V_{th(OVP)}$ voltage before count=8 is reached, the counter is reset to zero.

If a lower overvoltage protection level is needed, a Zener diode can be connected between the VCC pin and the PROTECT pin.

## 7.5 Input voltage detection (VINSENSE pin)

In a typical application the mains input voltage can be detected by the VINSENSE pin. Switching does not take place until the voltage on VINSENSE has reached the $V_{start(VINSENSE)}$ voltage (0.94 V typical).

When during operation the VINSENSE voltage drops below $V_{det(L)(VINSENSE)}$ (0.72 V typical), the converter stops switching and performs a restart.

An internal clamp of 5.2 V (typical) protects this pin from excessive voltages.

## 7.6 Protection input (PROTECT PIN)

Pin PROTECT is a general purpose input pin, which can be used to switch off the converter (latched protection). The converter is stopped when the voltage on this pin is pulled above $V_{det(H)(PROTECT)}$ (0.8 V typical) or below $V_{det(L)(PROTECT)}$ (0.5 V typical). A current of 32 μA (typical) flows out of the chip when the pin voltage is at the $V_{det(L)(PROTECT)}$ level. A current of 107 μA (typical) flows into the chip when the pin voltage is at the $V_{det(H)(PROTECT)}$ level.

The PROTECT input can be used to create an overvoltage detection and OTP functions.

A small capacitor can be connected to the pin if the protections on this pin are not used.

An internal clamp of 4.1 V (typical) protects this pin from excessive voltages.

## 7.7 Duty cycle control (CTRL pin)

The output power of the converter is regulated by the CTRL pin. This pin is connected to an internal 5.4 V supply using an internal 7 kΩ resistor.

The CTRL pin voltage sets the peak current which is measured via pin ISENSE (see Section 7.11). At low and medium output power the switching frequency is reduced (see Section 7.13). The maximum duty cycle is limited to 80 % (typical).

After 8 consecutive converter strokes at maximum duty cycle the restart protection is activated. Typically this occurs when the mains input voltage is removed.

## 7.8 Slope compensation (CTRL pin)

A slope compensation circuit is integrated in the IC for CCM. Slope compensation guarantees stable operation for duty cycles greater than 50 %.

## 7.9 Overpower timer (OPTIMER pin)

If the OPTIMER pin is connected to capacitor C4 (see Figure 3), a temporary overload situation is allowed. $V_{ctrl(Ipeak)}$ (see Figure 1) is set by pin CTRL. When $V_{ctrl(Ipeak)}$ is above 400 mV, the $I_{IO(OPTIMER)}$ current (11 μA typical) is sourced from the OPTIMER pin. If the voltage on the OPTIMER pin reaches the $V_{prot(OPTIMER)}$ voltage (2.5 V typical) the OverPower Protection (OPP) is triggered (see Figure 5).

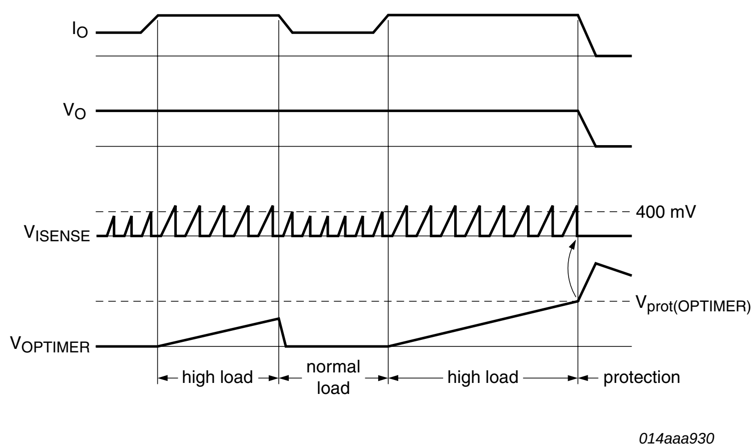



**Fig 5. Overpower delay (TEA1738T)**

In the TEA1738T when the $V_{prot(OPTIMER)}$ voltage is reached the device is restarted. The TEA1738LT is latched in an off state when the $V_{prot(OPTIMER)}$ voltage is reached.

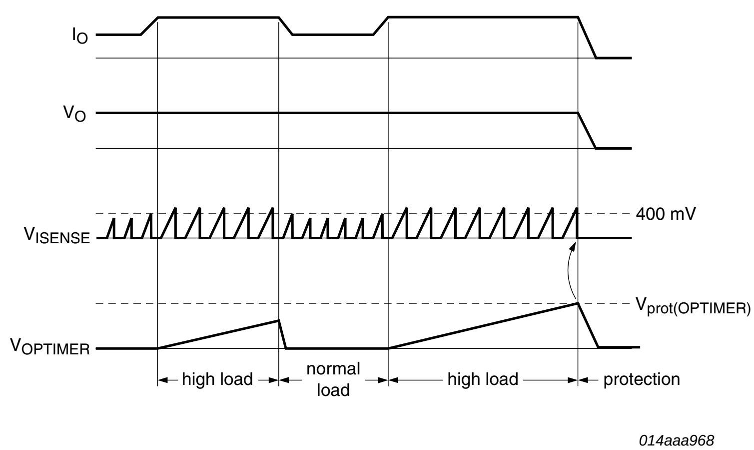



**Fig 6. Overpower delay: latched (TEA1738LT)**

## 7.10 Current mode control (ISENSE pin)

Current mode control is used for its good line regulation.

The primary current is sensed by the ISENSE pin across external resistor R9 (see Figure 3) and compared with an internal control voltage. The internal control voltage is proportional to the CTRL pin voltage (see Figure 7).

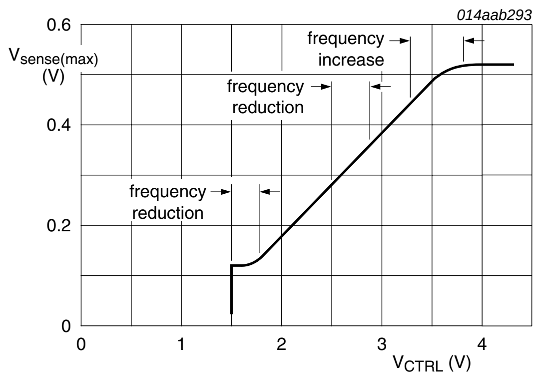



**Fig 7. Peak current control**

Leading edge blanking prevents false triggering due to capacitive discharge when switching on the external power switch (see Figure 8).

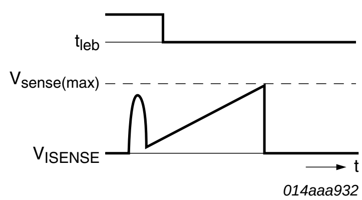



**Fig 8. Leading edge blanking**

## 7.11 Overpower or high/low line compensation (VINSENSE and ISENSE pins)

The overpower compensation function can be used to realize a maximum output power which is nearly constant over the full input mains.

The overpower compensation circuit measures the input voltage on the VINSENSE pin and outputs a proportionally dependent current on the ISENSE pin. The DC voltage across the soft start resistor limits the maximum peak current on the current sense resistor (see Figure 9).

At low output power levels the overpower compensation circuit is switched off.

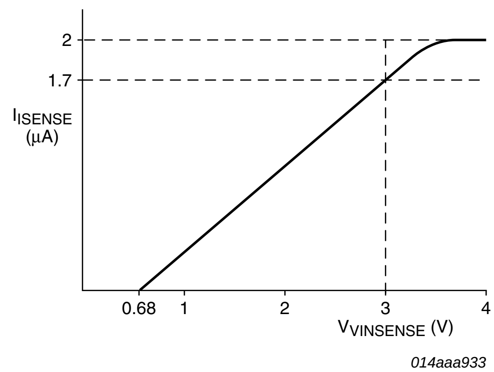



**Fig 9. Overpower compensation**

## 7.12 Soft start-up (ISENSE pin)

A soft start is performed to prevent audible noise during start-up or a restart condition. Before the converter (re)starts, soft start capacitor C6 (see Figure 3) on the ISENSE pin is charged. When the converter (re)starts switching, the primary peak current slowly increases as the soft start capacitor discharges through the soft start resistor (R6, see Figure 3).

The soft start time constant is set by the soft start capacitor value chosen. The soft start resistor value must also be taken into account, but this value is typically defined by the overpower compensation (see Section 7.11).

## 7.13 Peak power, medium power and low power operation

The switching frequency is increased for peak power operation. In medium power operation the switching losses are reduced by lowering the switching frequency. A second frequency reduction step is made when the output power is reduced to low power. In low power operation the converter switching frequency is reduced while the peak current is set to 25 % of the maximum peak current (see Figure 7 and Figure 10).

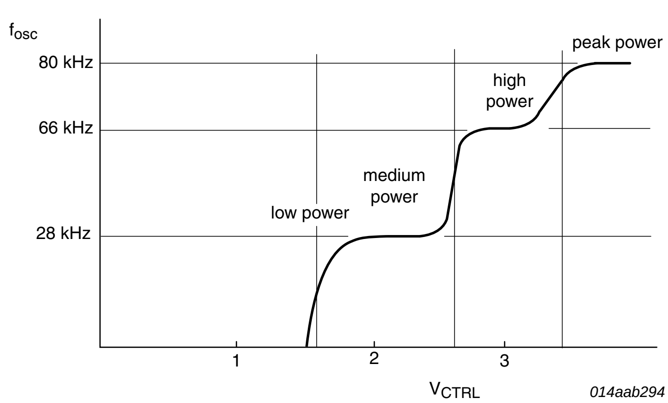



**Fig 10. Frequency control**

### 7.14 Driver (pin DRIVER)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 300 mA and a current sink capability of typically 750 mA. This allows for a fast turn-on and turn-off of the power MOSFET for efficient operation.

### 7.15 OverTemperature Protection (OTP)

Integrated temperature protection ensures the IC stops switching if the junction temperature exceeds the thermal shutdown temperature limit.

OTP is a latched protection. It can be reset by removing the voltage on pin VCC.

## 8. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Voltages** | | | | | |
| $V_{CC}$ | supply voltage | continuous | –0.4 | +30 | V |
| | | t < 100 ms | - | 35 | V |
| $V_{VINSENSE}$ | voltage on pin VINSENSE | current limited | –0.4 | +5.5 | V |
| $V_{PROTECT}$ | voltage on pin PROTECT | current limited | –0.4 | +5 | V |
| $V_{CTRL}$ | voltage on pin CTRL | | –0.4 | +5.5 | V |
| $V_{IO(OPTIMER)}$ | input/output voltage on pin OPTIMER | | –0.4 | +5 | V |
| $V_{ISENSE}$ | voltage on pin ISENSE | current limited | –0.4 | +5 | V |
| **Currents** | | | | | |
| $I_{CC}$ | supply current | $\delta < 10$ % | - | 0.4 | A |
| $I_{I(VINSENSE)}$ | input current on pin VINSENSE | | –1 | +1 | mA |
| $I_{I(PROTECT)}$ | input current on pin PROTECT | | –1 | +1 | mA |
| $I_{CTRL}$ | current on pin CTRL | | –3 | 0 | mA |
| $I_{ISENSE}$ | current on pin ISENSE | | –10 | +1 | mA |
| $I_{DRIVER}$ | current on pin DRIVER | $\delta < 10$ % | –0.4 | +1 | A |
| **General** | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} < 75$ °C | - | 0.5 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –40 | +150 | °C |

**Table 3. Limiting values** *…continued*
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **ESD** | | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | class 1 | | | | |
| | | human body model | [1] | - | 4000 | V |
| | | machine model | [2] | - | 300 | V |
| | | charged device model | | - | 750 | V |

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[2] Equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω resistor.

# 9. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; JEDEC test board | 150 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | in free air; JEDEC test board | 79 | K/W |

# 10. Characteristics

**Table 5. Characteristics**
*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply voltage management (pin VCC)** | | | | | | |
| $V_{startup}$ | start-up voltage | | 18.6 | 20.6 | 22.6 | V |
| $V_{th(UVLO)}$ | undervoltage lockout threshold voltage | | 11.2 | 12.2 | 13.2 | V |
| $V_{th(ovp)}$ | overvoltage protection threshold voltage | | 29 | 30 | 31 | V |
| $N_{cy(ovp)}$ | number of overvoltage protection cycles | | 7 | - | 8 | |
| $V_{clamp(VCC)}$ | clamp voltage on pin VCC | activated during restart; $I_{CC}$ = 100 μA | - | $V_{startup}$ + 1 | - | V |
| | | activated during latched protection; $I_{CC}$ = 100 μA | - | $V_{rst(latch)}$ + 1 | - | V |
| | | activated during latched protection; $I_{CC}$ = 500 μA | - | - | $V_{rst(latch)}$ + 4 | V |
| $I_{clamp(VCC)}$ | clamp current on pin VCC | activated during restart; $V_{CC}$ = 25 V | 730 | - | - | μA |
| $V_{hys}$ | hysteresis voltage | $V_{startup} - V_{th(UVLO)}$ | 7.5 | 9 | 10.5 | V |
| $I_{CC(startup)}$ | start-up supply current | $V_{CC} < V_{startup}$ | 5 | 10 | 15 | μA |

**Table 5. Characteristics** *...continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CC(oper)}$ | operating supply current | no load on pin DRIVER; δ = 2 % | | - | 0.55 | - | mA |
| | | no load on pin DRIVER; δ = 25 % | | - | 0.59 | - | mA |
| $V_{rst(latch)}$ | latched reset voltage | | | 4 | 5 | 6 | V |
| **Input voltage sensing (pin VINSENSE)** | | | | | | | |
| $V_{start(VINSENSE)}$ | start voltage on pin VINSENSE | detection level | | 0.89 | 0.94 | 0.99 | V |
| $V_{det(L)(VINSENSE)}$ | LOW-level detection voltage on pin VINSENSE | | | 0.68 | 0.72 | 0.76 | V |
| $I_{O(VINSENSE)}$ | output current on pin VINSENSE | | | - | −9 | - | nA |
| $V_{clamp(VINSENSE)}$ | clamp voltage on pin VINSENSE | $I_{I(VINSENSE)}$ = 50 μA | | - | 5.2 | - | V |
| **Protection input (pin PROTECT)** | | | | | | | |
| $V_{det(L)(PROTECT)}$ | LOW-level detection voltage on pin PROTECT | | | 0.47 | 0.50 | 0.53 | V |
| $V_{det(H)(PROTECT)}$ | HIGH-level detection voltage on pin PROTECT | | | 0.75 | 0.8 | 0.85 | V |
| $I_{O(PROTECT)}$ | output current on pin PROTECT | $V_{PROTECT} = V_{low(PROTECT)}$ | | −34 | −32 | −30 | μA |
| | | $V_{PROTECT} = V_{high(PROTECT)}$ | | 87 | 107 | 127 | μA |
| $V_{clamp(PROTECT)}$ | clamp voltage on pin PROTECT | $I_{I(PROTECT)}$ = 200 μA | [1] | 3.5 | 4.1 | 4.7 | V |
| **Peak current control (pin CTRL)** | | | | | | | |
| $V_{CTRL}$ | voltage on pin CTRL | for minimum flyback peak current | | 1.5 | 1.8 | 2.1 | V |
| | | for maximum flyback peak current | | 3.4 | 3.9 | 4.3 | V |
| $R_{int(CTRL)}$ | internal resistance on pin CTRL | | | 5 | 7 | 9 | kΩ |
| $I_{O(CTRL)}$ | output current on pin CTRL | $V_{CTRL}$ = 1.4 V | | −0.7 | −0.5 | −0.3 | mA |
| | | $V_{CTRL}$ = 3.7 V | | −0.28 | −0.2 | −0.12 | mA |
| **Pulse width modulator** | | | | | | | |
| $f_{osc}$ | oscillator frequency | peak power | | - | 78 | - | kHz |
| | | high power | | - | 63 | - | kHz |
| | | medium power | | - | 26.5 | - | kHz |
| $f_{mod}$ | modulation frequency | | | 210 | 280 | 350 | Hz |
| $\Delta f_{mod}$ | modulation frequency variation | high power | | ± 3 | ± 4 | ± 5 | kHz |
| $\delta_{max}$ | maximum duty cycle | | | - | 80 | - | % |

**Table 5. Characteristics** *...continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{cy(sw)\delta max}$ | Number of switching cycles with maximum duty cycle | | 7 | - | 8 | |
| $V_{start(red)f}$ | frequency reduction start voltage | pin CTRL transfer between high and medium power | - | 2.7 | - | V |
| | | pin CTRL going to low power | 1.5 | 1.8 | 2.1 | V |
| $V_{\delta(zero)}$ | zero duty cycle voltage | pin CTRL | 1.25 | 1.55 | 1.85 | V |
| **Overpower protection (pin OPTIMER)** | | | | | | |
| $V_{prot(OPTIMER)}$ | protection voltage on pin OPTIMER | | 2.4 | 2.5 | 2.6 | V |
| $I_{prot(OPTIMER)}$ | protection current on pin OPTIMER | no overpower situation | 100 | 150 | 200 | μA |
| | | overpower situation | −12.2 | −10.7 | −9.2 | μA |
| **Restart timer (pin OPTIMER)** | | | | | | |
| $V_{restart(OPTIMER)}$ | restart voltage on pin OPTIMER | low level | 0.8 | 1.2 | 1.6 | V |
| | | high level | 4.1 | 4.5 | 4.9 | V |
| $I_{restart(OPTIMER)}$ | restart current on pin OPTIMER | charging OPTIMER capacitor | −127 | −107 | −87 | μA |
| | | discharging OPTIMER capacitor | −0.1 | 0 | 0.1 | μA |
| **Current sense (pin ISENSE)** | | | | | | |
| $V_{sense(max)}$ | maximum sense voltage | $\Delta V/\Delta t$ = 50 mV/μs; $V_{VINSENSE}$ = 0.78 V | 0.48 | 0.51 | 0.54 | V |
| | | $\Delta V/\Delta t$ = 200 mV/μs; $V_{VINSENSE}$ = 0.78 V | 0.50 | 0.53 | 0.56 | V |
| $V_{th(sense)opp}$ | overpower protection sense threshold voltage | | 370 | 400 | 430 | mV |
| $\Delta V_{ISENSE}/\Delta t$ | slope compensation voltage on pin ISENSE | $\Delta V/\Delta t$ = 50 mV/μs, high power mode | - | 19 | - | mV/μs |
| $t_{leb}$ | leading edge blanking time | | 250 | 300 | 350 | ns |
| **Overpower compensation (pin VINSENSE and pin ISENSE)** | | | | | | |
| $I_{opc(ISENSE)}$ | overpower compensation current on pin ISENSE | $V_{VINSENSE}$ = 1 V; $V_{sense(max)}$ > 400 mV | - | 0.28 | - | μA |
| | | $V_{VINSENSE}$=3 V; $V_{sense(max)}$ > 400 mV | - | 1.7 | - | μA |
| **Soft start (pin ISENSE)** | | | | | | |
| $I_{start(soft)}$ | soft start current | | −63 | −55 | −47 | μA |
| $V_{start(soft)}$ | soft start voltage | $V_{CTRL}$ = 4 V; enable voltage | - | $V_{sense(max)}$ | - | V |
| $R_{start(soft)}$ | soft start resistance | | 12 | - | - | kΩ |
| **Driver (pin DRIVER)** | | | | | | |

**Table 5. Characteristics** *...continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{source(DRIVER)}$ | source current on pin DRIVER | $V_{DRIVER}$ = 2 V | - | –0.3 | -0.25 | A |
| $I_{sink(DRIVER)}$ | sink current on pin DRIVER | $V_{DRIVER}$ = 2 V | 0.25 | 0.3 | - | A |
| | | $V_{DRIVER}$ = 10 V | 0.6 | 0.75 | - | A |
| $V_{O(DRIVER)max}$ | maximum output voltage on pin DRIVER | | 9 | 10.5 | 12 | V |
| **Temperature protection** | | | | | | |
| $T_{pl(IC)}$ | IC protection level temperature | | 130 | 140 | 150 | °C |

[1] The clamp voltage on the PROTECT pin is lowered when the IC is in Power-down mode (latched or restart protection).

## 11. Application information

A power supply with the TEA1738(L) is a flyback converter operating in Continuous conduction mode (see Figure 11).

Capacitor C5 buffers the IC supply voltage, which is powered via resistor R3 at start-up and via the auxiliary winding during normal operation. Sense resistor R9 converts the current through the MOSFET S1 into a voltage on pin ISENSE. The value of resistor R9 defines the maximum primary peak current in MOSFET S1. Resistor R7 reduces the peak current to capacitor C5.

In the example shown in Figure 11, the PROTECT pin is used for OTP. The OTP level is set by Negative Temperature Coefficient (NTC) resistor R4. If an (additional) external OVP is required, a Zener diode can be connected between the VCC pin and the PROTECT pin.

The VINSENSE pin is used for mains voltage detection and resistors R1 and R2 set the start voltage to about 80 V (AC).

The overpower protection time, defined by capacitor C4, is set to 60 ms.

The restart time is defined by capacitor C4 and resistor R8 at 0.5 s.

Resistor R6 and capacitor C6 define the soft start time. Resistor R5 prevents the soft start capacitor C6 from being charged during normal operation due to negative voltage spikes across the current sense resistor R9.

Capacitor C3 reduces the noise on the CTRL pin. Resistor R7 reduces the peak current to capacitor C5.

Resistor R10 is required to limit the current spikes to the DRIVER pin due to parasitic inductance of the current sense resistor R9.

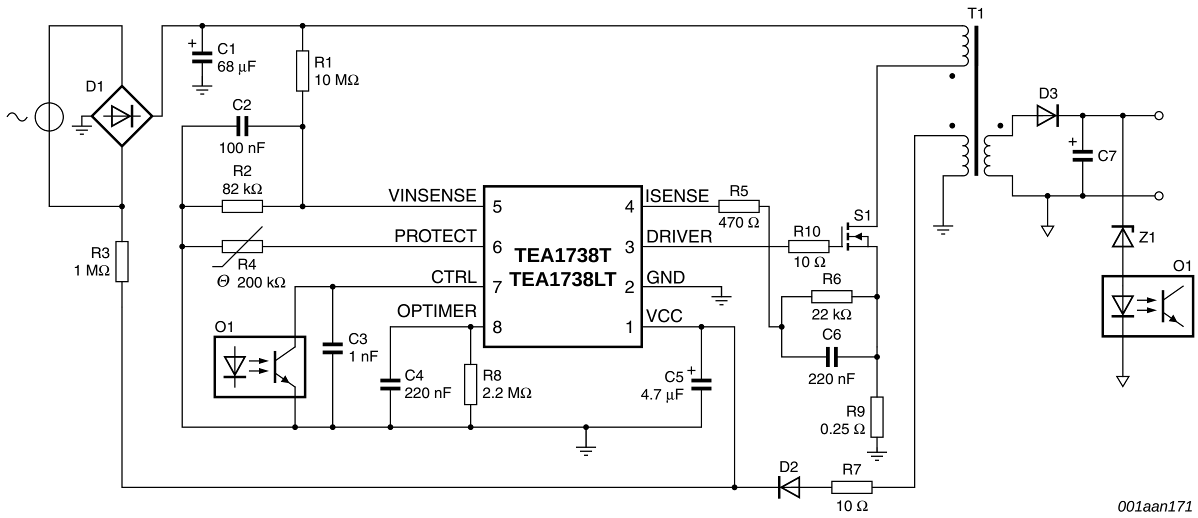
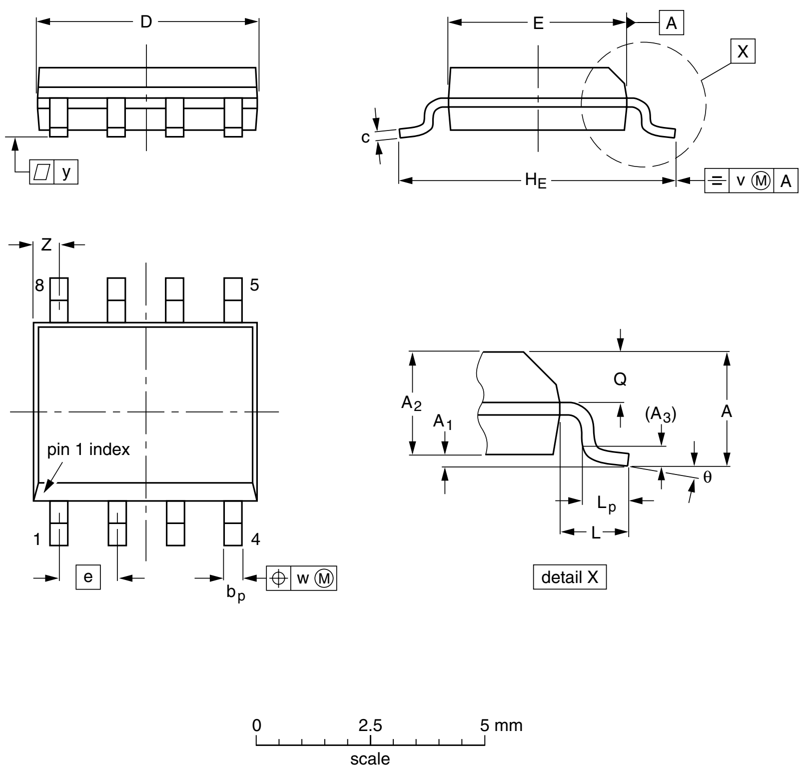



**Fig 11. Typical application**

## 12. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

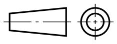
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | |  | ~~99-12-27~~<br>03-02-18 |

**Fig 12. Package outline SOT96-1 (SO8)**

# 13. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TEA1738T_TEA1738LT v.2 | 20110114 | Product data sheet | - | TEA1738T_TEA1738LT v.1 |
| TEA1738T_TEA1738LT v.1 | 20101231 | Preliminary data sheet | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 14.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 14.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**GreenChip —** is a trademark of NXP B.V.

## 15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 16. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 14 January 2011**

**Document identifier: TEA1738T_TEA1738LT**