Filterless, High Efficiency, Mono 3 W Class-D Audio Amplifier

SSM2315

FEATURES

Filterless Class-D amplifier with Σ-Δ modulation
No sync necessary when using multiple Class-D amplifiers from Analog Devices, Inc.
3 W into 3 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with <1% total harmonic distortion (THD + N)
93% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
>103 dB signal-to-noise ratio (SNR)
Single-supply operation from 2.5 V to 5.5 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Available in 9-ball, 1.5 mm × 1.5 mm WLCSP
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 6 dB or user adjustable gain setting

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2315 is a fully integrated, high efficiency, Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with <1% THD + N driving a 3 Ω load from a 5.0 V supply.

The SSM2315 features a high efficiency, low noise modulation scheme that requires no external LC output filters. The modulation continues to provide high efficiency even at low output power. It operates with 93% efficiency at 1.4 W into 8 Ω or 85% efficiency at 3 W into 3 Ω from a 5.0 V supply and has an SNR of >103 dB. Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2315 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The device also includes pop-and-click suppression circuitry. This suppression circuitry minimizes voltage glitches at the output during turn-on and turn-off, reducing audible noise on activation and deactivation.

The fully differential input of the SSM2315 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The default gain of the SSM2315 is 6 dB, but users can reduce the gain by using a pair of external resistors (see the Gain section).

The SSM2315 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 9-ball, 1.5 mm × 1.5 mm wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

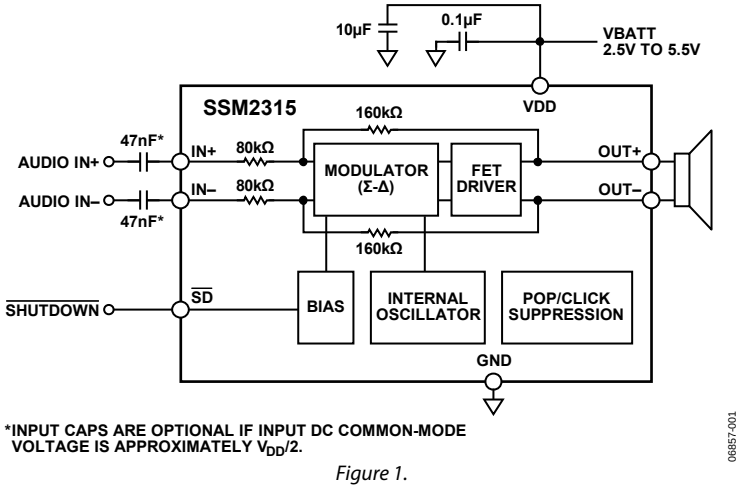

Figure 1.

Rev. A

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2/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω + 33 µH, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions[1]	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.48		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.75		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.84		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.94		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.72		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.38		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.40[2]		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.72		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.43		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.72		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		4.28[2]		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		2.14		W
Efficiency	η	P_O = 1.4 W, R_L = 8 Ω + 33 µH, V_{DD} = 5.0 V		93		%
Total Harmonic Distortion + Noise	THD + N	P_O = 1 W, R_L = 8 Ω + 33 µH, f = 1 kHz, V_{DD} = 5.0 V		0.004		%
		P_O = 0.5 W, R_L = 8 Ω + 33 µH, f = 1 kHz, V_{DD} = 3.6 V		0.004		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1.0	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz, output referred		55		dB
Average Switching Frequency	f_{SW}			280		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 6 dB		2.0		mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.5	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF		60		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		3.2		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		2.8		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		2.4		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 5.0 V		3.3		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 3.6 V		2.9		mA
		V_{IN} = 0 V, load = 8 Ω + 33 µH, V_{DD} = 2.5 V		2.4		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Gain			6		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = V_{DD}		80		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		7		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac-grounded, gain = 6 dB, A-weighted		21		µV rms
Signal-to-Noise Ratio	SNR	P_O = 1.4 W, R_L = 8 Ω		103		dB

[1] Note that although the SSM2315 has good audio quality above 3 W, continuous output power beyond 3 W must be avoided due to device packaging limitations.
[2] This value represents measured performance; packaging limitations must not be exceeded.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Continuous Output Power	3 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-ball, 1.5 mm × 1.5 mm WLCSP	1S0P	162	39	°C/W
	2S0P	76	21	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

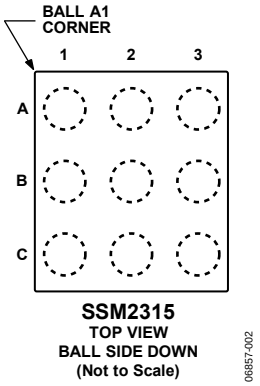

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
2C	$\overline{SD}$	Shutdown Input. Active low digital input.
2A	GND	Ground.
1A	IN+	Noninverting Input.
1C	IN–	Inverting Input.
3C	OUT+	Noninverting Output.
1B	VDD	Power Supply.
3B	GND	Ground.
3A	OUT–	Inverting Output.
2B	PVDD	Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

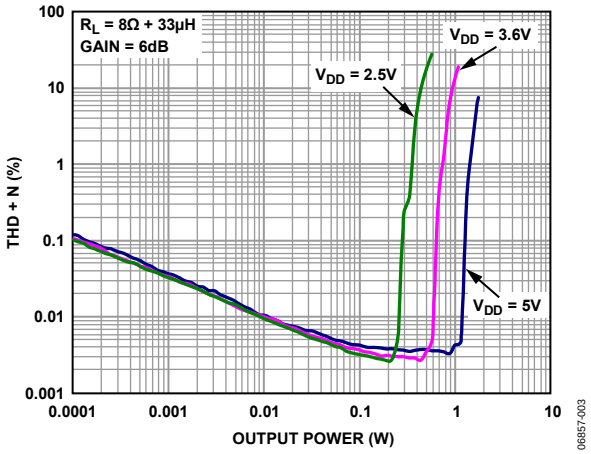

Figure 3. THD + N vs. Output Power, R_L = 8 Ω + 33 µH, Gain = 6 dB

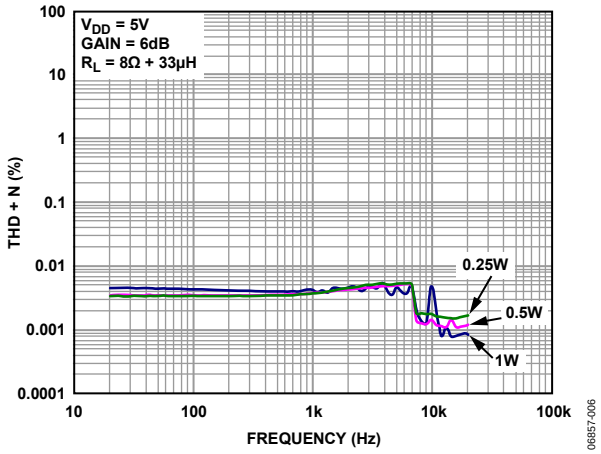

Figure 6. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 8 Ω + 33 µH, Gain = 6 dB

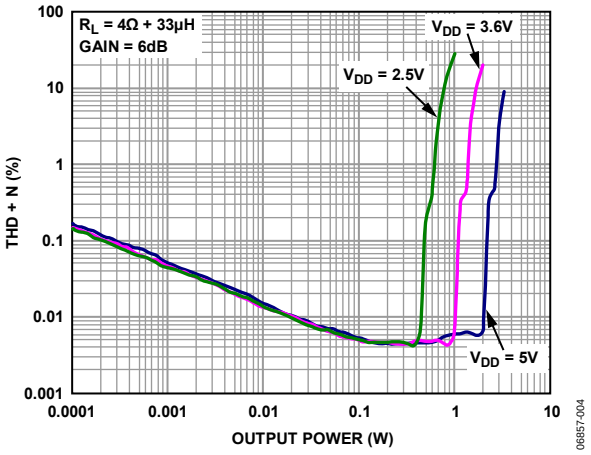

Figure 4. THD + N vs. Output Power, R_L = 4 Ω + 33 µH, Gain = 6 dB

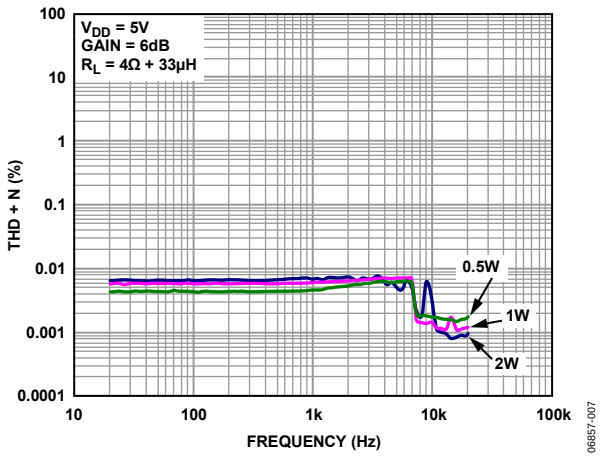

Figure 7. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 4 Ω + 33 µH, Gain = 6 dB

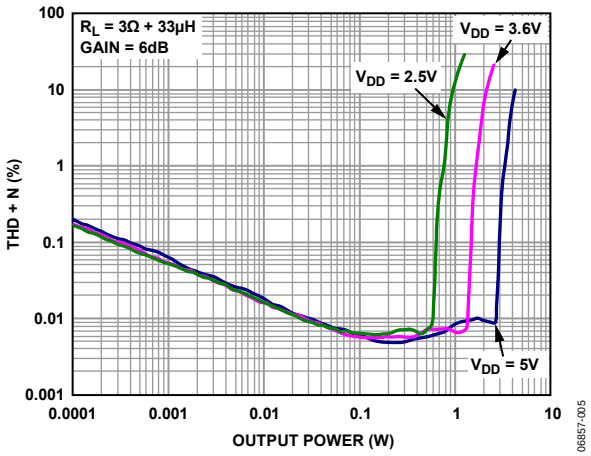

Figure 5. THD + N vs. Output Power, R_L = 3 Ω + 33 µH, Gain = 6 dB

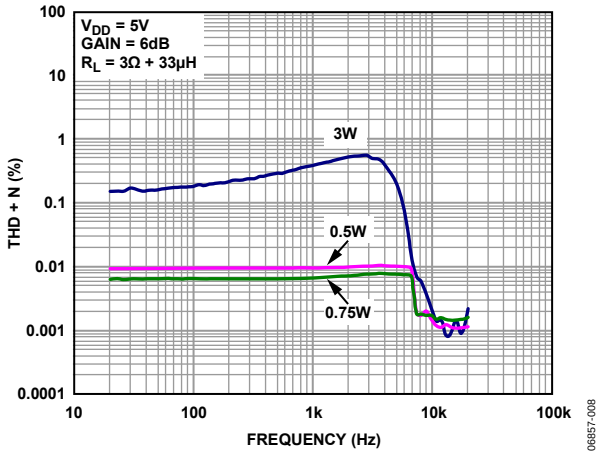

Figure 8. THD + N vs. Frequency, V_{DD} = 5 V, R_L = 3 Ω + 33 µH, Gain = 6 dB

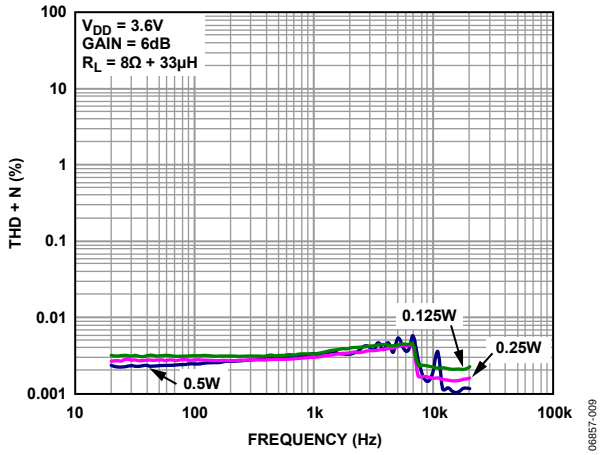

Figure 9. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω + 33 µH, Gain = 6 dB

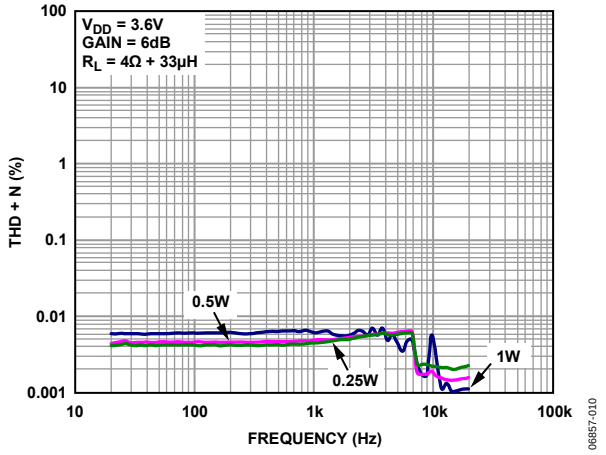

Figure 10. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω + 33 µH, Gain = 6 dB

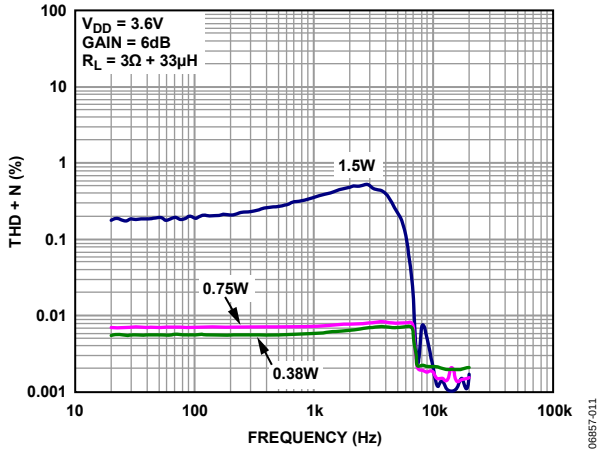

Figure 11. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 3 Ω + 33 µH, Gain = 6 dB

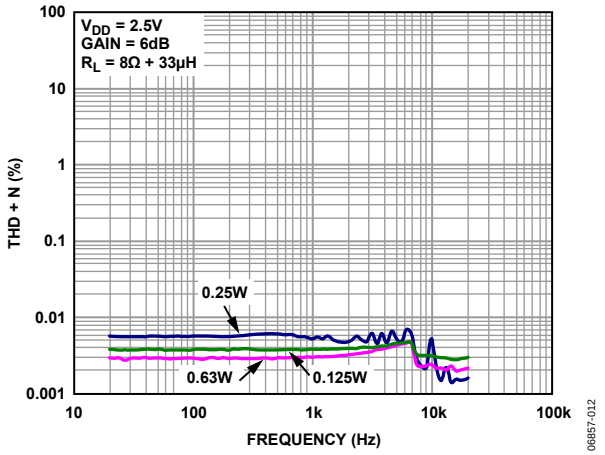

Figure 12. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω + 33 µH, Gain = 6 dB

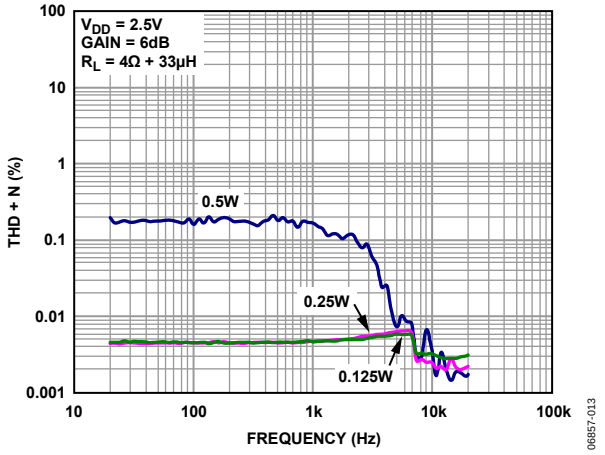

Figure 13. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω + 33 µH, Gain = 6 dB

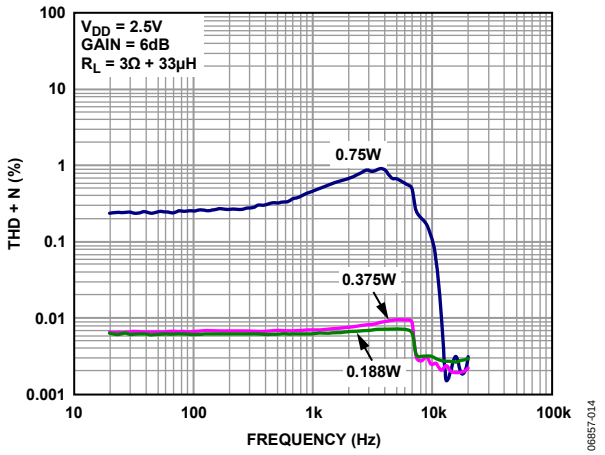

Figure 14. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 3 Ω + 33 µH, Gain = 6 dB

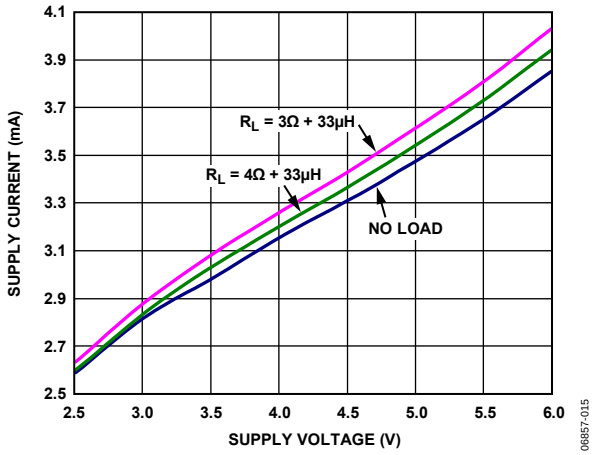

Figure 15. Supply Current vs. Supply Voltage

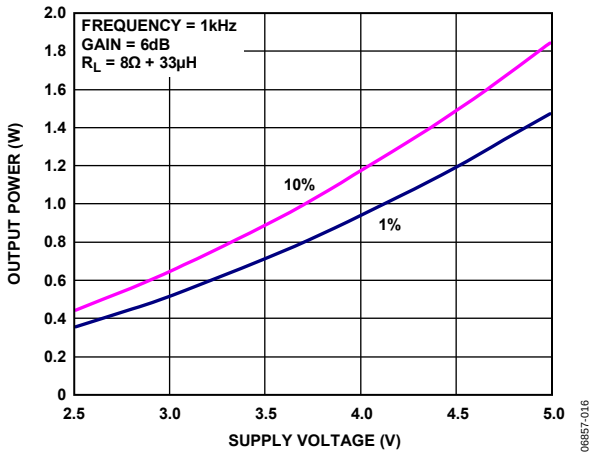

Figure 16. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω + 33 µH, Gain = 6 dB

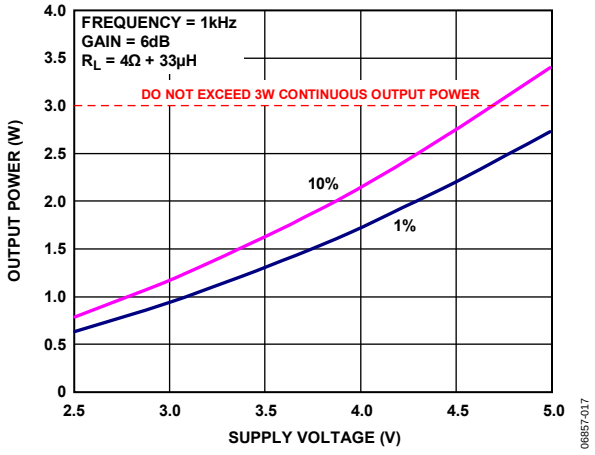

Figure 17. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω + 33 µH, Gain = 6 dB

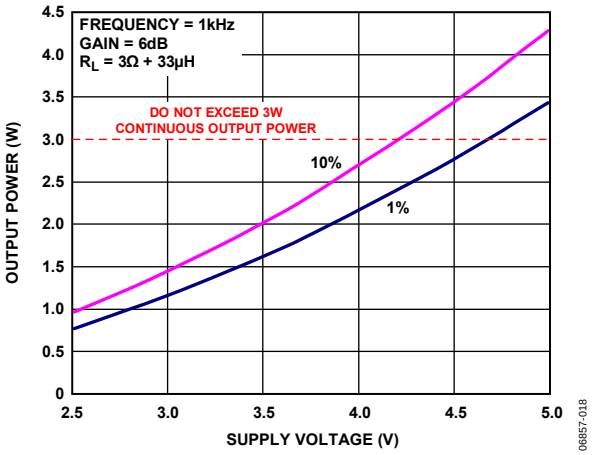

Figure 18. Maximum Output Power vs. Supply Voltage, R_L = 3 Ω + 33 µH, Gain = 6 dB

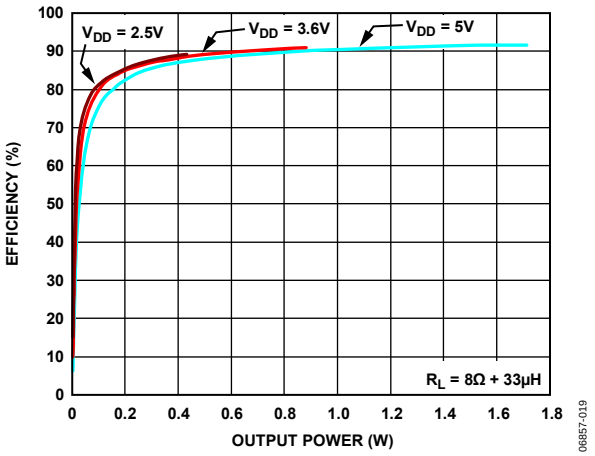

Figure 19. Efficiency vs. Output Power, R_L = 8 Ω + 33 µH

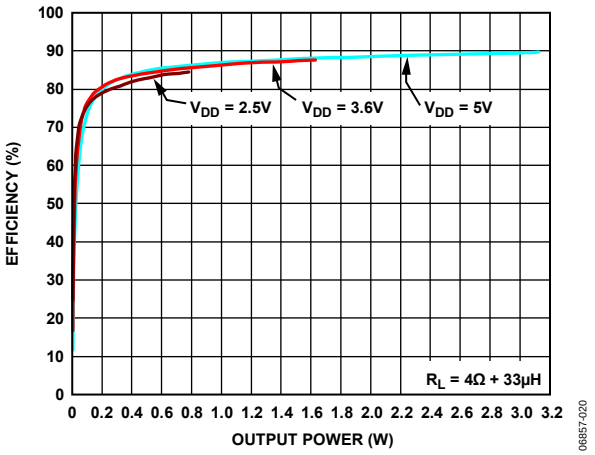

Figure 20. Efficiency vs. Output Power, R_L = 4 Ω + 33 µH

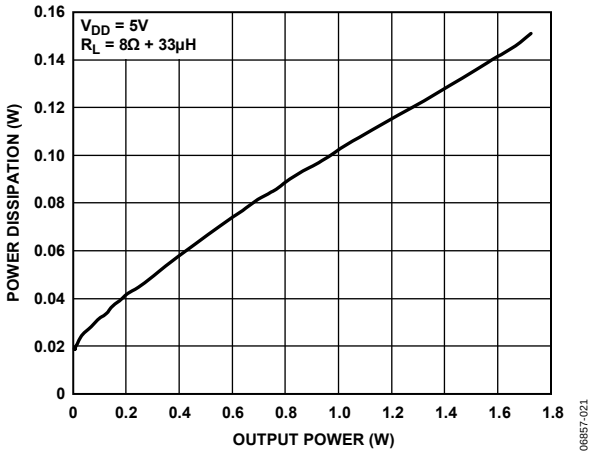

Figure 21. Power Dissipation vs. Output Power, R_L = 8 Ω + 33 µH at V_{DD} = 5.0 V

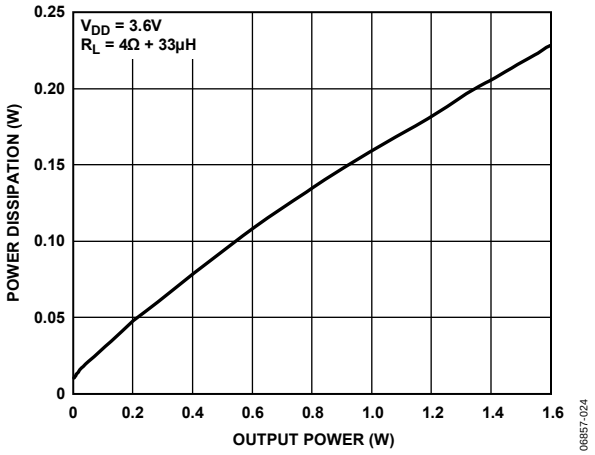

Figure 24. Power Dissipation vs. Output Power, R_L = 4 Ω + 33 µH at V_{DD} = 3.6 V

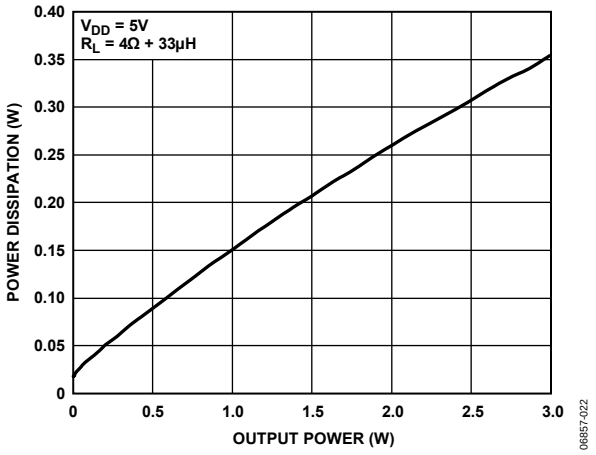

Figure 22. Power Dissipation vs. Output Power, R_L = 4 Ω + 33 µH at V_{DD} = 5.0 V

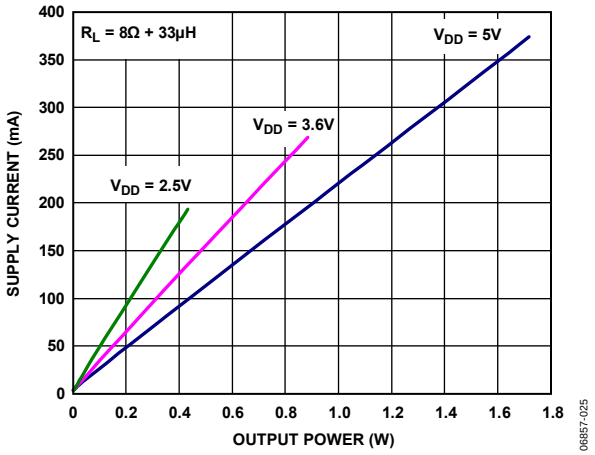

Figure 25. Supply Current vs. Output Power, R_L = 8 Ω + 33 µH

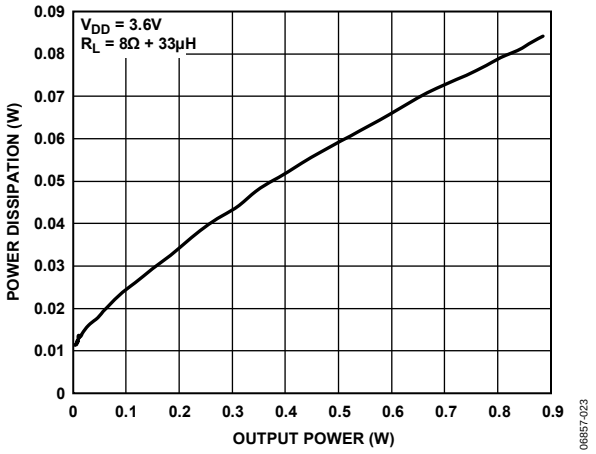

Figure 23. Power Dissipation vs. Output Power, R_L = 8 Ω + 33 µH at V_{DD} = 3.6 V

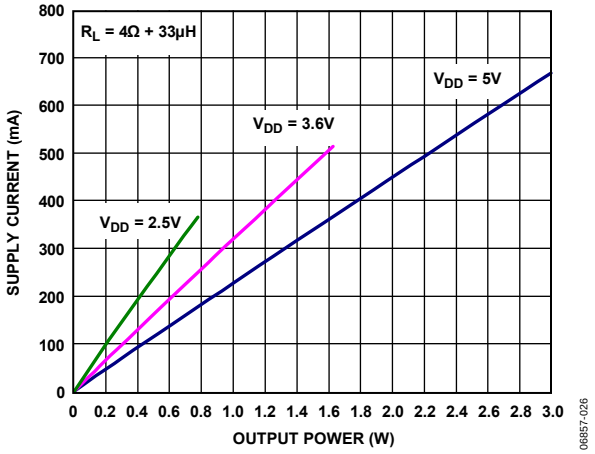

Figure 26. Supply Current vs. Output Power, R_L = 4 Ω + 33 µH

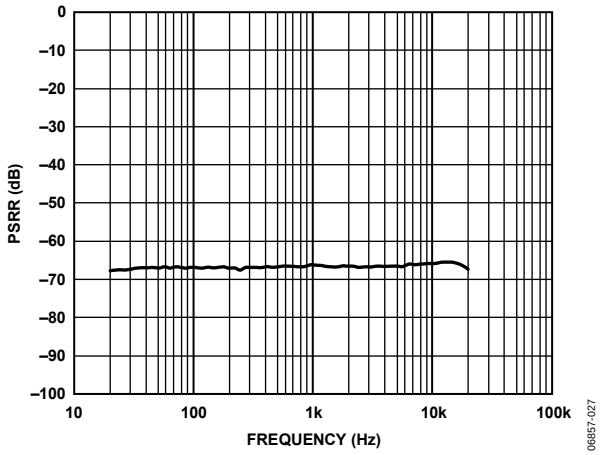

Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency

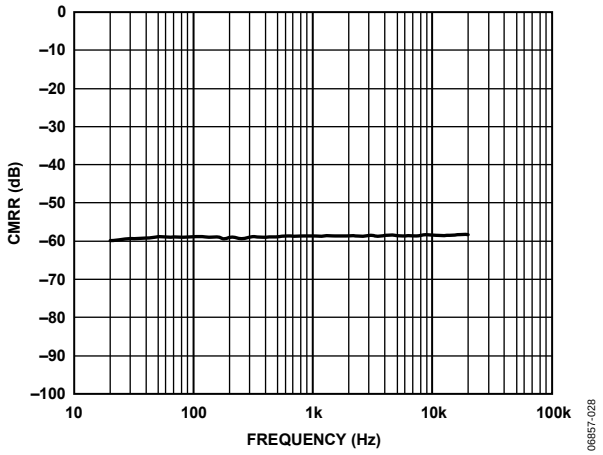

Figure 28. Common-Mode Rejection Ratio (CMRR) vs. Frequency

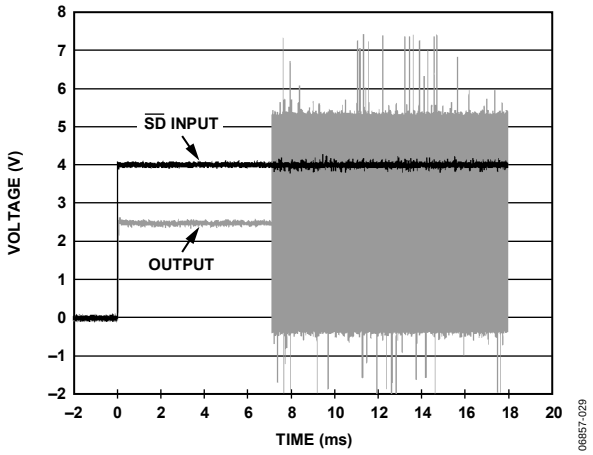

Figure 29. Turn-On Response

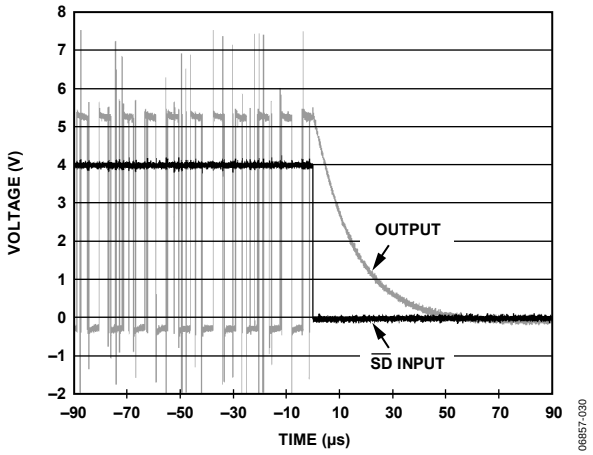

Figure 30. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

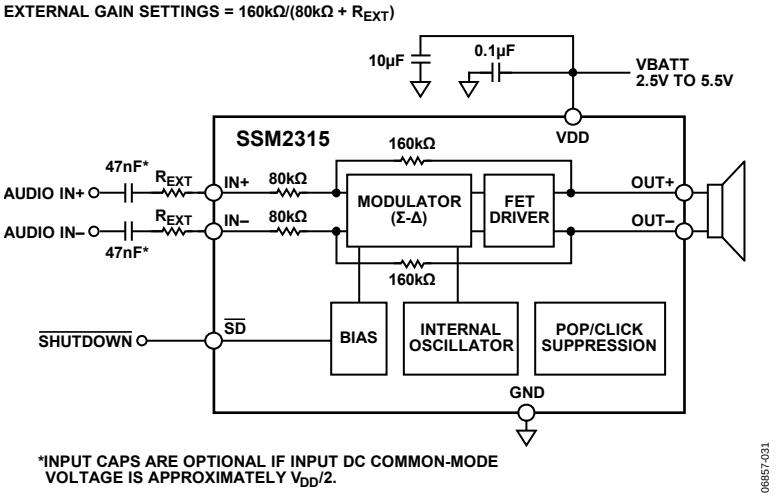

Figure 31. Differential Input Configuration, User-Adjustable Gain

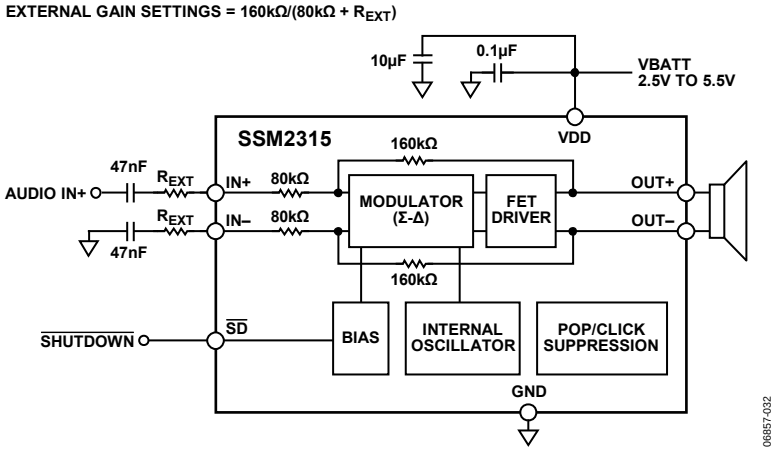

Figure 32. Single-Ended Input Configuration, User-Adjustable Gain

THEORY OF OPERATION

OVERVIEW

The SSM2315 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing systems cost. The SSM2315 does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output. Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the SSM2315 uses a Σ-Δ modulation to determine the switching pattern of the output devices, resulting in a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emission that may otherwise be radiated by speakers and long cable traces. The SSM2315 does not require external EMI filtering for twisted speaker cable lengths shorter than 10 cm. Due to the inherent spread spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2315 amplifiers.

The SSM2315 also offers protection circuits for overcurrent and temperature protection.

GAIN

The SSM2315 has a default gain of 6 dB that can be reduced by using a pair of external resistors with a value calculated as follows:

$$External\ Gain\ Settings = 160\ k\Omega/(80\ k\Omega + R_{EXT})$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers may occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients may be generated when the amplifier system changes its operating mode. For example, the following may be sources of audible transients: system power-up and power-down, mute and unmute, input source change, and sample rate change. The SSM2315 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

OUTPUT MODULATION DESCRIPTION

The SSM2315 uses three-level, Σ-Δ output modulation. Each output can swing from GND to VDD and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real world situation, there are always noise sources present.

Due to this constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

However, most of the time, output differential voltage is 0 V, due to the Analog Devices patented, three-level, Σ-Δ output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 33 depicts three-level, Σ-Δ output modulation with and without input stimulus.

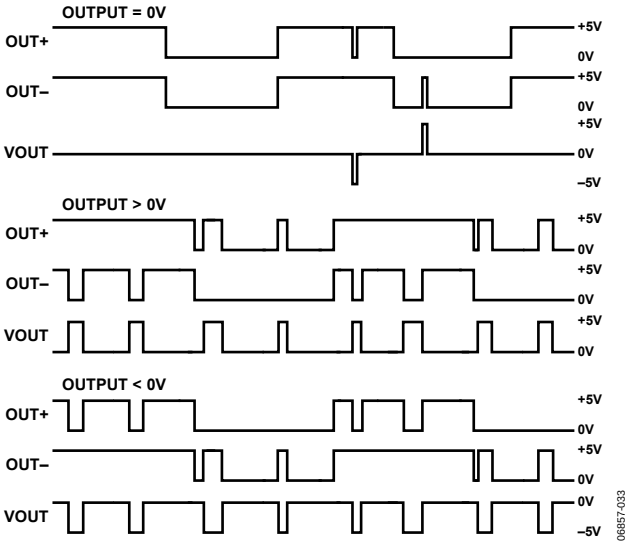

Figure 33. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

LAYOUT

As output power continues to increase, care must be taken to lay out PCB traces and wires properly among the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and to minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances.

In addition, good PCB layouts isolate critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer printed circuit boards can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane. Similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

INPUT CAPACITOR SELECTION

The SSM2315 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed, or if a single-ended source is used. If high-pass filtering is needed at the input, the input capacitor and the input resistor of the SSM2315 form a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the dc PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low total harmonic distortion (THD), and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality, low ESL, low ESR capacitor, usually of around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2315 helps maintain efficient performance.

OUTLINE DIMENSIONS

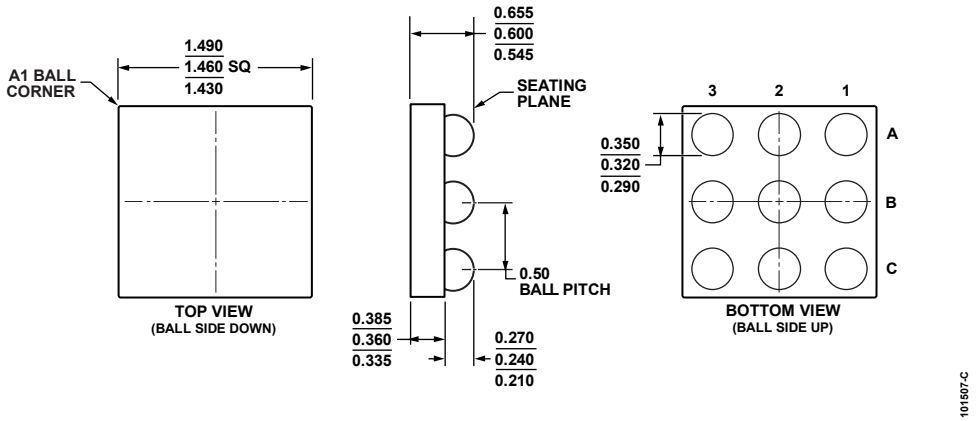

Figure 34. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CP-9-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2315CBZ-R2[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2	Y0P
SSM2315CBZ-REEL[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2	Y0P
SSM2315CBZ-REEL7[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-2	Y0P
SSM2315-EVALZ[1]		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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