

NLAS7222A

High-Speed USB 2.0 (480 Mbps) DPDT Switch

ON Semiconductor's NLAS7222A series of analog switch circuits are produced using the company's advanced sub-micron CMOS technology, achieving industry-leading performance.

The NLAS7222A is a 2- to 1-port analog switch. Its wide bandwidth and low bit-to-bit skew allow it to pass high-speed differential signals with good signal integrity. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. Industry-leading advantages include a propagation delay of less than 250 ps, resulting from its low channel resistance and low I/O capacitance. Its high channel-to-channel crosstalk rejection results in minimal noise interference. Its bandwidth is wide enough to pass High-Speed USB 2.0 differential signals (480 Mb/s).

Features

- R_{ON} is Typically 6.5Ω at $V_{CC} = 3 V$
- Low Bit-to-Bit Skew: Typically 50 ps
- OVT on D+ and D- up to 3.6 V
- Power OFF Protection:
When $V_{CC} = 0 V$, D+ and D- Can Tolerate up to 3.6 V
- Low Crosstalk: $-45 \text{ dB @ } 250 \text{ MHz}$
- Low Current Consumption: $1 \mu A$
- Near-Zero Propagation Delay: 250 ps
- Channel On-Capacitance: 6.5 pF (Typical)
- V_{CC} Operating Range: +3.0 V to +3.6 V
- > 700 MHz Bandwidth (or Data Frequency)
- This is a Pb-Free Device

Typical Applications

- Differential Signal Data Routing
- USB 2.0 Signal Routing

Important Information

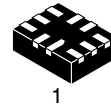
- Continuous Current Rating Through Each Switch $\pm 50 \text{ mA}$
- 8 kV I/O to GND ESD Protection



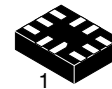
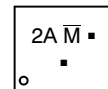
ON Semiconductor®

<http://onsemi.com>

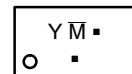
MARKING DIAGRAM



WQFN10
CASE 488AQ



UQFN10
CASE 488AT



XX = Specific Device Code
XX = 2A or Y

M = Date Code

■ = Pb-Free Device

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NLAS7222A

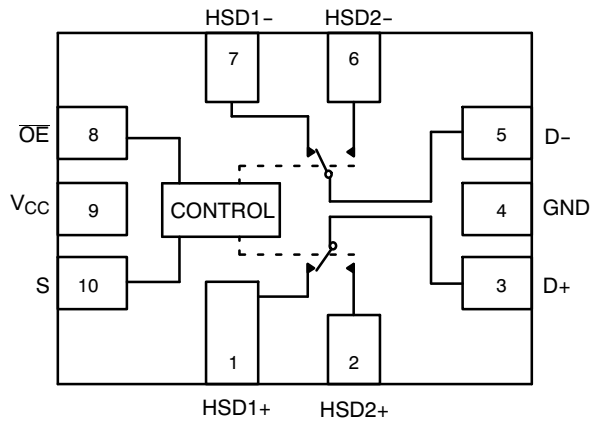


Figure 1. Pin Connections and Logic Diagram
(Top View)

Table 1. PIN DESCRIPTION

Pin	Function
S	Select Input
\overline{OE}	Output Enable
HSD1+, HSD1-, HSD2+, HSD2-, D+, D-	Data Ports

Table 2. TRUTH TABLE

\overline{OE}	S	HSD1+, HSD1-	HSD2+, HSD2-
1	X	OFF	OFF
0	0	ON	OFF
0	1	OFF	ON

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Positive DC Supply Voltage	-0.5 to +4.6	V
V_{IS}	Analog Switch Input Voltage HSD1+, HSD1-, HSD2+, HSD2- D+, D-	-0.5 to $V_{CC} + 0.3$ -0.5 to +4.6	V
V_{IN}	Digital Select Input Voltage	-0.5 to +4.6	V
I_D	Continuous DC Current (Through Analog Switch)	50	mA
P_D	Power Dissipation	0.5	W
T_S	Storage Temperature	-65 to +150	°C
ESD	Human Body Model I/O to GND All Pins	8 2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	3.0	3.6	V
V_{IS}	Analog I/O Voltage (HSD1+, HSD1-, HSD2+, HSD2-)	GND	V_{CC}	V
V_{OS}	Analog Common Output Voltage (D+, D-)	GND	3.6	V
V_{IN}	Digital Select Input Voltage	GND	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C
t_r, t_f	Input Rise or Fall Time $V_{CC} = 3.3 V \pm 0.3 V$	0	15	ns

NLAS7222A

DC ELECTRICAL CHARACTERISTICS FOR USB 2.0 SWITCHING OVER OPERATIONAL RANGE

Symbol	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
				Min	Typ (Note 1)	Max	
V _{IH}	Input HIGH Voltage (V _{IN})		3.0 to 3.6	1.3	-	-	V
V _{IL}	Input LOW Voltage (V _{IN})		3.0 to 3.6	-	-	0.5	V
V _{IK}	Clamp Diode Voltage	I _S = -18 mA	3.0	-	-	-1.2	V
I _{CC}	Quiescent Supply Current	V _{IS} = V _{CC} or GND; I _D = 0 A	3.6	-	-	1.0	μA
I _{CC(T)}	Increase in I _{CC} per Control Voltage	V _{IN} = 2.6 V	3.6	-	-	10.0	μA
I _I	Input Leakage Current	0 ≤ V _{IS} ≤ V _{CC}	3.6	-	-	±1.0	μA
I _{OZ}	OFF State Leakage	0 ≤ V _{IS} ; V _{OS} ≤ V _{CC}	3.6	-	-	±1.0	μA
I _{OFF}	Power OFF Leakage Current (D+, D-)	0 ≤ V _{IS} ; V _{OS} ≤ V _{CC}	0	-	-	±1.0	μA
R _{ON}	Switch On-Resistance	V _{IS} = 0 to 0.4 V; I _D = 8 mA	3.0	-	6.5	9.0	Ω
R _{FLAT(ON)}	On-Resistance Flatness	V _{IS} = 0 to 1.0 V; I _D = 8 mA	3.0	-	2.0	-	Ω
ΔR _{ON}	On-Resistance match from center ports to any other ports	V _{IS} = 0 to 0.4 V; I _D = 8 mA	3.0	-	0.35	-	Ω

1. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} (V)	-40°C to +85°C			Unit
				Min	Typ (Note 2)	Max	
t _{ON}	Turn-ON Time	V _{IS} = 0.8 V	3.0 to 3.6	-	13.0	30.0	ns
t _{OFF}	Turn-OFF Time	V _{IS} = 0.8 V	3.0 to 3.6	-	12.0	25.0	ns
t _{BBM}	Break-Before-Make Delay	V _{IS} = 0.8 V	3.0 to 3.6	2.0	4.7	6.5	ns
t _{PD}	Propagation Delay	C _L = 10 pF	3.0 to 3.6	-	0.25	-	ns
O _{IRR}	OFF-Isolation	f = 250 MHz; R _L = 50 Ω	3.0 to 3.6	-	-28	-	dB
X _{TALK}	Non-Adjacent Channel Crosstalk	f = 250 MHz; R _L = 50 Ω	3.0 to 3.6	-	-45	-	dB
BW	-3 dB Bandwidth	R _L = 50 Ω; C _L = 0 pF	3.0 to 3.6	-	700	-	MHz
		R _L = 50 Ω; C _L = 5 pF		-	500	-	

AC ELECTRICAL CHARACTERISTICS FOR USB 2.0 SWITCHING OVER OPERATIONAL RANGE

t _{SK(O)}	Channel-to-Channel Skew	C _L = 10 pF	3.0 to 3.6	-	0.05	-	ns
T _{JITTER}	Total Jitter	R _L = 50 Ω; C _L = 10 pF t _r = t _f = 500 ps at 480 Mbps	3.0 to 3.6	-	0.2	-	ns

2. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

CAPACITANCE

Symbol	Parameter	Test Conditions	-40°C to +85°C			Unit
			Min	Typ (Note 3)	Max	
C _{IN}	Control Pin Input Capacitance	V _{CC} = 0 V	-	2.5	-	pF
C _{ON}	HSD+, HSD- ON Capacitance	V _{CC} = 3.3 V; \overline{OE} = 0 V	-	7.0	-	pF
C _{OFF}	HSD+, HSD- OFF Capacitance	V _{CC} = V _{IS} = 3.3 V; \overline{OE} = 3.3 V	-	4.5	-	pF

3. Typical values are at V_{CC} = 3.3 V and T_A = +25°C

NLAS7222A

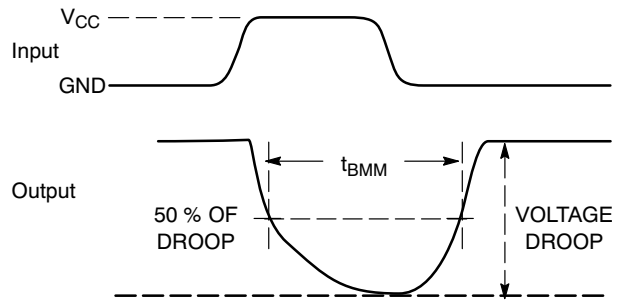
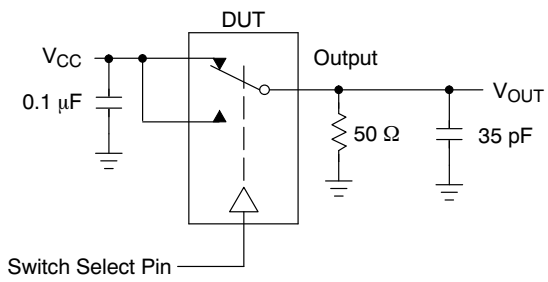


Figure 2. t_{BMM} (Time Break-Before-Make)

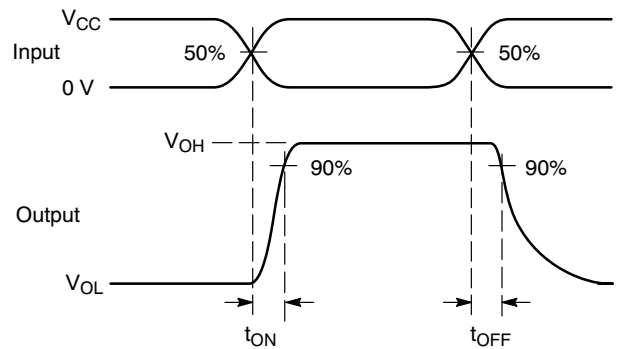
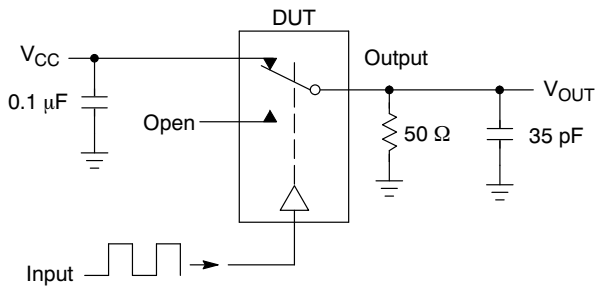


Figure 3. $t_{\text{ON}}/t_{\text{OFF}}$

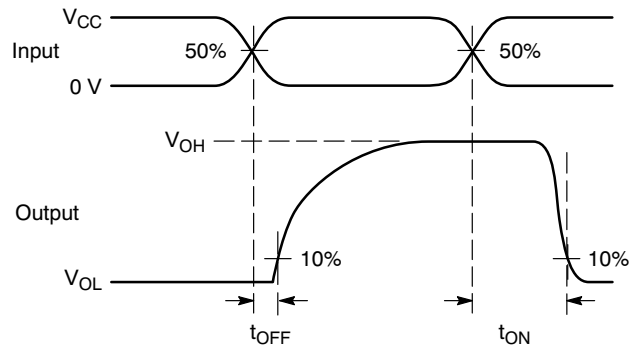
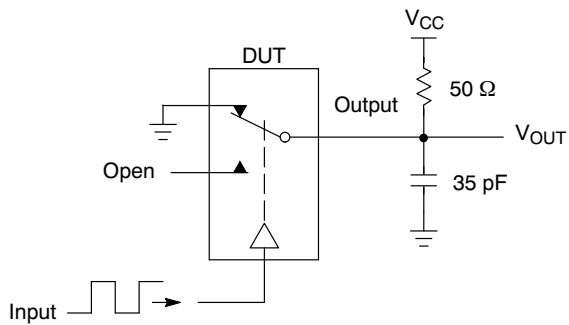
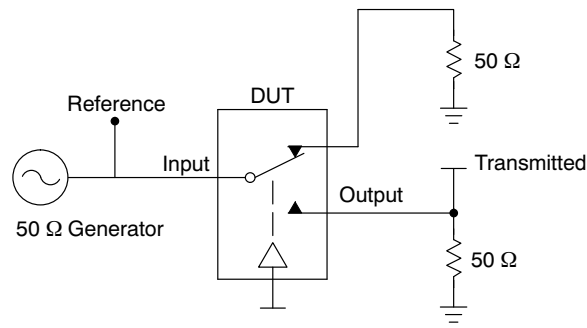


Figure 4. $t_{\text{ON}}/t_{\text{OFF}}$

NLAS7222A



Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 5. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

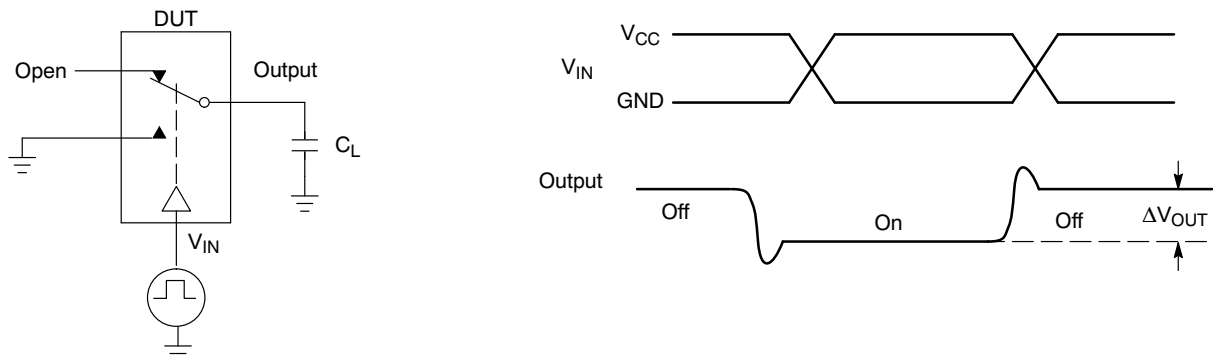


Figure 6. Charge Injection: (Q)

NLAS7222A

APPLICATIONS INFORMATION

The low on resistance and capacitance of the NLAS7222A provides for a high bandwidth analog switch suitable for applications such as USB data switching. Results for the USB 2.0 signal quality tests will be shown in this section, along with a description of the evaluation test board. The data for the eye diagram signal quality and jitter tests verifies that the NLAS7222A can be used as a data switch in low, full and high speed USB 2.0 systems.

Figures 7, 8 and 9 provide a description of the test evaluation board. The USB tests were conducted per the procedures provided by the USB Implementers Forum

(www.usb.org), the industry group responsible for defining the USB certification requirements. The test patterns were generated by a PC and MATLAB software, and were inputted to the analog switch through USB connectors J1 (HSD1) or J2 (HSD2). A USB certified device was plugged into connector J4 to function as a data transceiver. The high speed and full speed tests used a flash memory device, while the low speed tests used a mouse. Test connectors J3 and J5 provide a direct connection of the USB device and were used to verify that the analog switch does not distort the data signals.

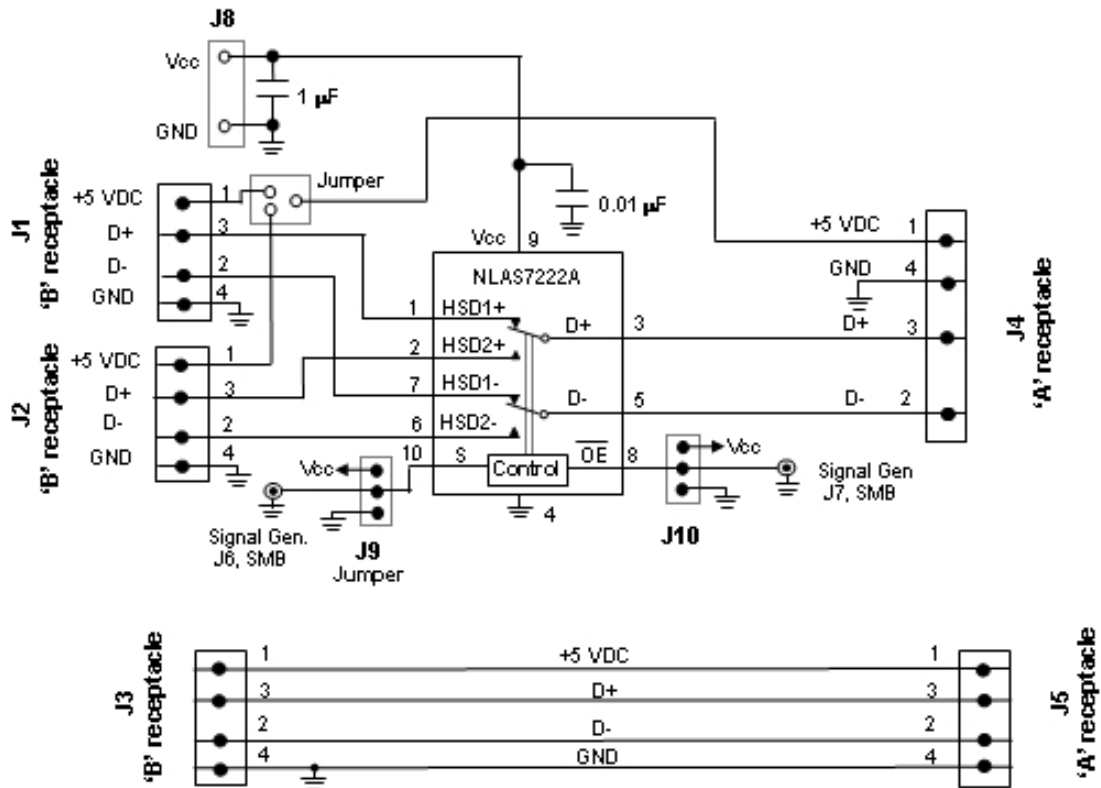


Figure 7. Schematic of the NLAS7222A USB Demo Board

NLAS7222A

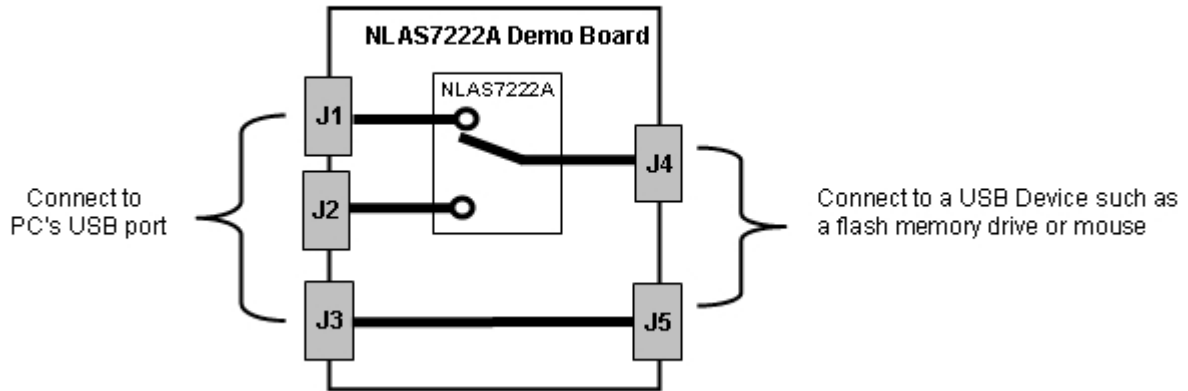


Figure 8. Block Diagram of the NLAS7222A USB Demo Board

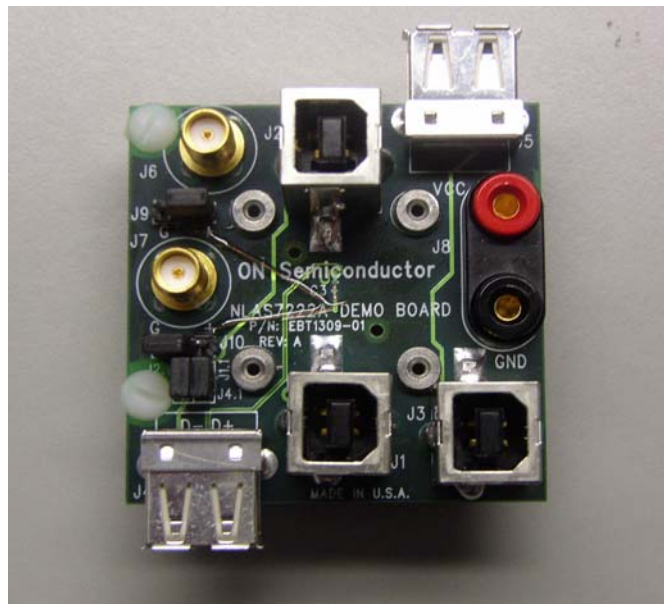


Figure 9. Photograph of the NLAS7222A USB Demo Board

NLAS7222A

AND8267/D – NLAS7222A USB 2.0 Signal Quality Compliance Tests

Figures 10, 11 and 12 show the test results for USB eye diagram tests. A summary of the USB tests is provided in Table 3. The NLAS7222A passes the low, full and high

speed signal quality, eye diagram and jitter tests. Application note AND8267/D provides a detailed description of the USB 2.0 test results.

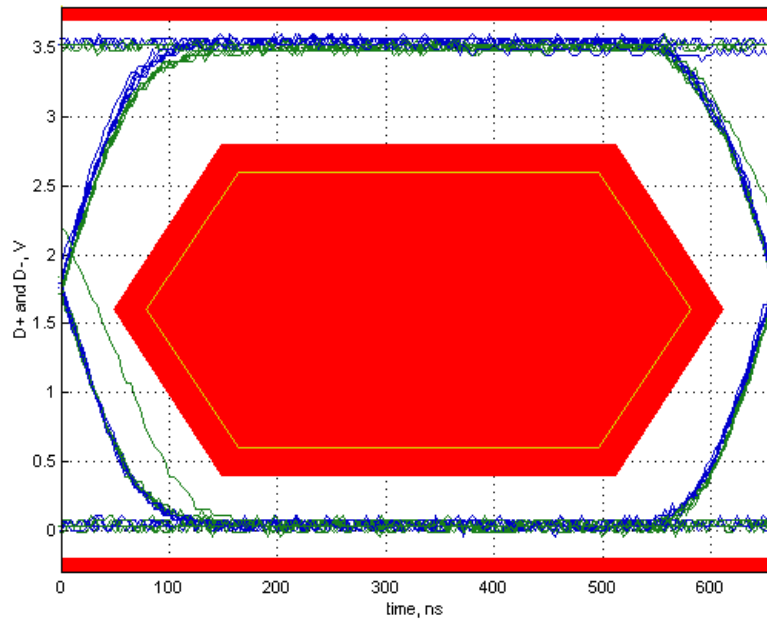


Figure 10. Low Speed Signal Quality Eye Diagram Test (NLA7222A with $V_{CC} = 3.6\text{ V}$)

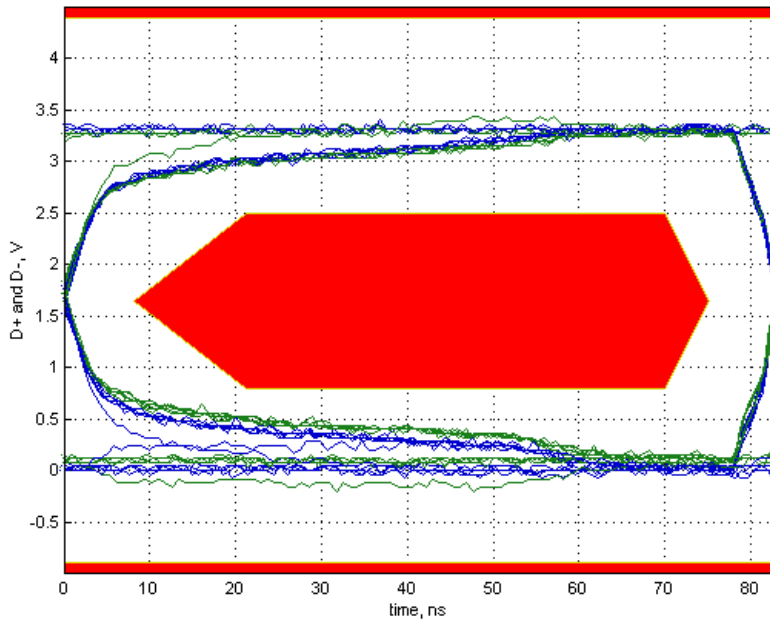


Figure 11. Full Speed Signal Quality Eye Diagram Test (NLA7222A with $V_{CC} = 3.6\text{ V}$)

NLAS7222A

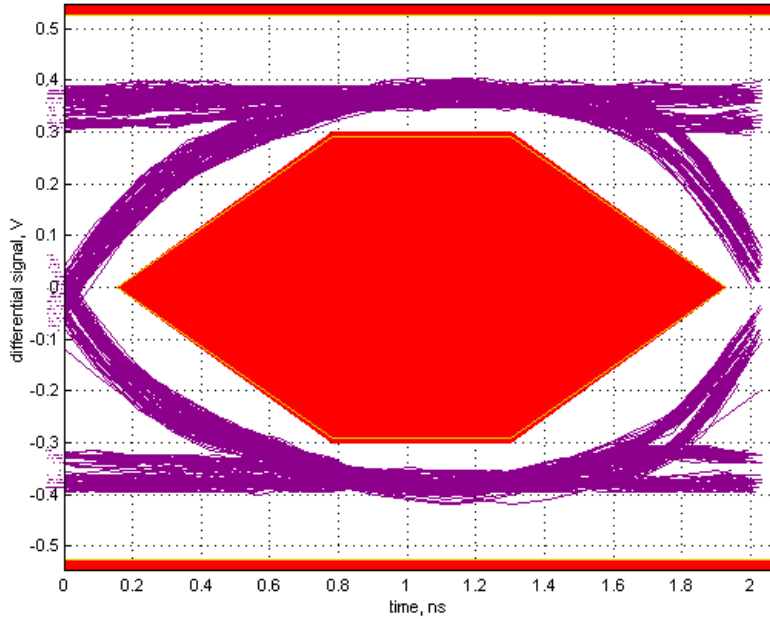


Figure 12. High Speed Signal Quality Eye Diagram Test (NLA7222A with $V_{CC} = 3.0\text{ V}$)

Table 3. Summary of the USB 2.0 Signal Quality Tests Results

Compliance Test	Low Speed	Full Speed	High Speed
Signal Quality Test	Pass	Pass	Pass
Signal Eye Test	Pass	Pass	Pass
EOP Width	1.29 ms	166.86 ns	7.98 bits
Measured Signal Rate	1.5140 MHz	12.0016 MHz	480.0685 MHz
Crossover Voltage Range	1.75 to 1.83 V, mean crossover = 1.78 V	1.70 to 1.73 V, mean crossover = 1.71 V	N/A
Connective Jitter Range	-2.2 to 2.2 ns, RMS jitter = 1.3 ns	-0.2 to 0.2 ns, RMS jitter = 0.1 ns	-79.4 to 77.4 ps, RMS jitter = 35.0 ps
Paired JK Jitter Range	-1.4 to 2.7 ns, RMS jitter = 1.3 ns	-0.1 to 0.1 ns, RMS jitter = 0.1 ns	-93.2 to 78.7 ps, RMS jitter = 24.4 ps
Paired KJ Jitter Range	-1.9 to 1.1 ns, RMS jitter = 1.0 ns	-0.2 to 0.1 ns, RMS jitter = 0.1 ns	-72.8 to 50.9 ps, RMS jitter = 15.6 ps

ORDERING INFORMATION

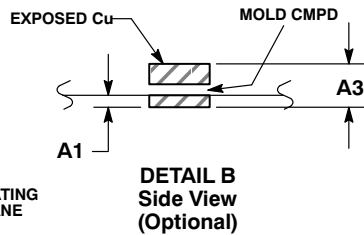
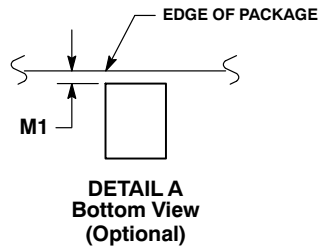
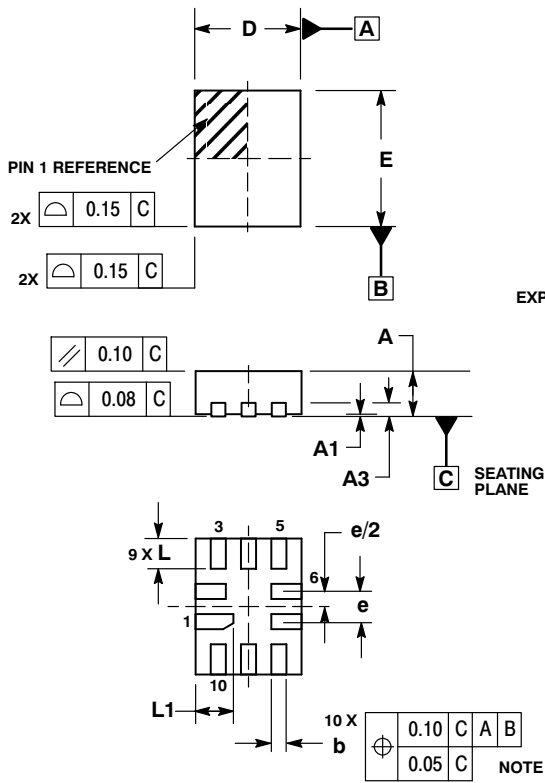
Device	Package	Shipping†
NLAS7222AMTR2G	WQFN10 (Pb-Free)	3000 / Tape & Reel
NLAS7222AMUR2G	UQFN10 (Pb-Free)	
NLAS7222AMUTAG		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NLAS7222A

PACKAGE DIMENSIONS

WQFN10, 1.4x1.8x0.4P
CASE 488AQ-01
ISSUE C

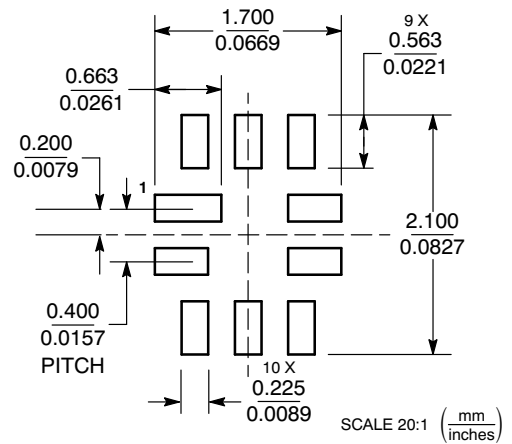


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. EXPOSED PADS CONNECTED TO DIE FLAG. USED AS TEST CONTACTS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.050
A3	0.20	REF
b	0.15	0.25
D	1.40	BSC
E	1.80	BSC
e	0.40	BSC
L	0.30	0.50
L1	0.40	0.60
M1	0.00	0.05

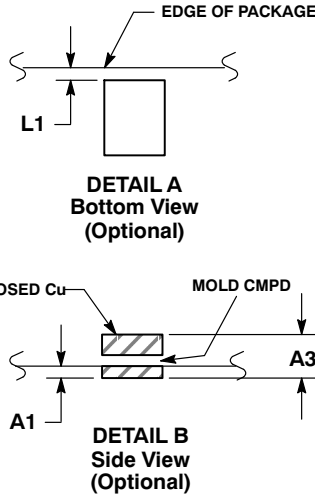
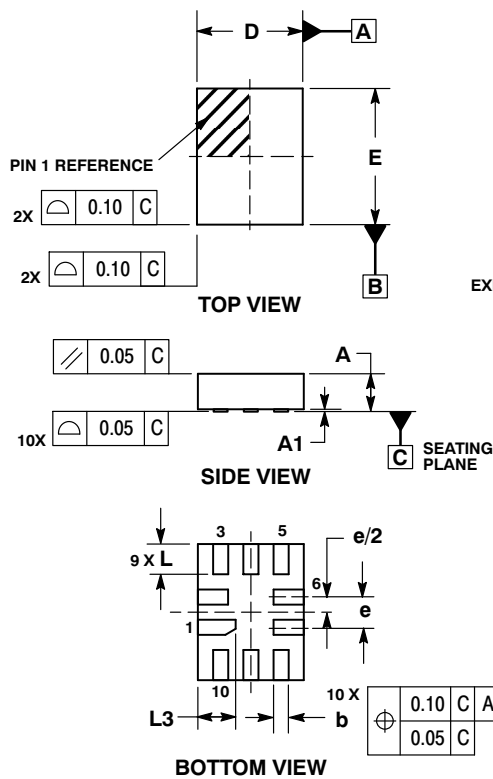
MOUNTING FOOTPRINT



NLAS7222A

PACKAGE DIMENSIONS

UQFN10, 1.4x1.8, 0.4P
CASE 488AT-01
ISSUE A

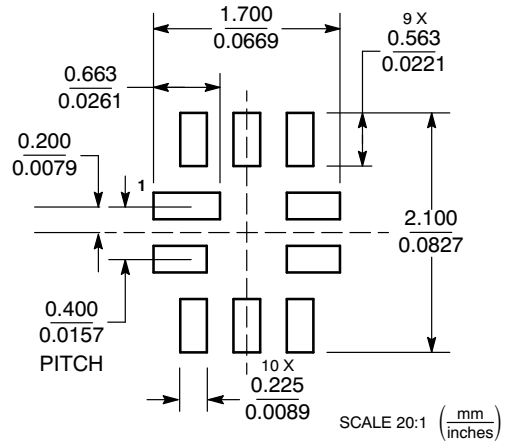


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.80 BSC	
e	0.40 BSC	
L	0.30	0.50
L1	0.00	0.15
L3	0.40	0.60

MOUNTING FOOTPRINT



ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910
Japan Customer Focus Center
 Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NLAS7222A/D