TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX74F,TC74LCX74FN,TC74LCX74FT

Low-Voltage Dual D-Type Flip-Flop with 5-V Tolerant Inputs and Outputs

The TC74LCX74F/FN/FT is a high-performance CMOS D-type flip-flop. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3 V) $V_{\rm CC}$ applications, but it could be used to interface to 5-V supply environment for inputs

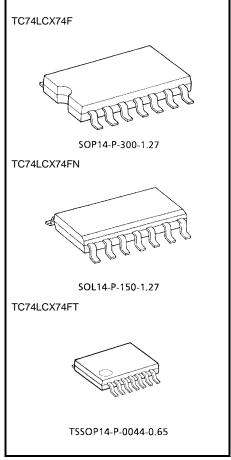
The signal level applied to the D input is transferred to Q output during the positive going transition of the CK pulse. $\overline{\text{CLR}}$ and $\overline{\text{PR}}$ are independent of the CK and are accomplished by setting the appropriate input low.

All inputs are equipped with protection circuits against static discharge.

Features

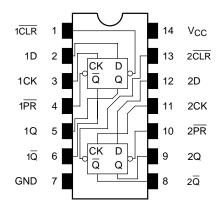
- Low-voltage operation: VCC = 2.0 to 3.6 V
- High-speed operation: $t_{pd} = 7.0 \text{ ns (max) (VCC} = 3.0 \text{ to } 3.6 \text{ V)}$
- Output current: $|I_{OH}|/I_{OL} = 24 \text{ mA (min)} (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: ±500 mA
- Available in JEDEC SOP, JEITA SOP and TSSOP
- · Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 74 type

Note: xxxFN (JEDEC SOP) is not available in Japan.

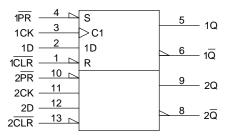


Weight SOP14-P-300-1.27: 0.18 g (typ.) SOL14-P-150-1.27: 0.12 g (typ.) TSSOP14-P-0044-0.65: 0.06 g (typ.)

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs			Outputs		Function	
CLR	PR	D	СК	Q	IQ	1 unction
L	Н	Χ	Χ	L	Н	Clear
Н	L	Х	Х	Ι	L	Preset
L	L	Х	Х	Н	Н	_
Н	Н	L	<u>_</u>	L	Н	_
Н	Н	Н	 	Н	L	_
Н	Н	Х		Qn	Qn	No change

X: Don't care

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage	Vcc	-0.5 to 7.0	V
DC input voltage	V _{IN}	−0.5 to 7.0	V
		-0.5 to 7.0 (Note 1)	
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
		(Note 2)	
Input diode current	I _{IK}	-50	mA
Output diode current	I _{OK}	±50 (Note 3)	mA
DC output current	lout	±50	mA
Power dissipation	P _D	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: $V_{CC} = 0 V$

Note 2: High or low state. IOUT absolute maximum rating must be observed.

Note 3: $V_{OUT} < GND, V_{OUT} > V_{CC}$



Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V _{CC}	2.0 to 3.6	V	
Tower supply voltage	VCC	1.5 to 3.6 (Note 4)	V	
Input voltage	V _{IN}	0 to 5.5	V	
Output voltage	Vout	0 to 5.5 (Note 5)	V	
Output voltage	VO01	0 to V _{CC} (Note 6)	V	
Output current	I _{OH} /I _{OI}	±24 (Note 7)	mA	
Output current	IOH/IOL	±12 (Note 8)	ША	
Operating temperature	T _{opr}	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 9)	ns/V	

Note 4: Data retention only

Note 5: $V_{CC} = 0 V$

Note 6: High or low state

Note 7: $V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$

Note 8: $V_{CC} = 2.7 \text{ to } 3.0 \text{ V}$

Note 9: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics ($Ta = -40 \text{ to } 85^{\circ}\text{C}$)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage Output voltage Input leakage curren	H-level	V _{IH}	_		2.7 to 3.6	2.0	_	V
	L-level	V _{IL}	_		2.7 to 3.6		0.8	٧
		Vон	$V_{IN} = V_{IH}$ or V_{IL}	I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	_	V
	H-level			I _{OH} = -12 mA	2.7	2.2	_	
				$I_{OH} = -18 \text{ mA}$	3.0	2.4		
Output voltage				$I_{OH} = -24 \text{ mA}$	3.0	2.2	_	
	L-level	V _{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100 \ \mu A$	2.7 to 3.6		0.2	
				$I_{OL} = 12 \text{ mA}$	2.7		0.4	
				$I_{OL} = 16 \text{ mA}$	3.0		0.4	
				$I_{OL} = 24 \text{ mA}$	3.0	_	0.55	
Input leakage curre	Input leakage current		V _{IN} = 0 to 5.5 V		2.7 to 3.6		±5.0	μΑ
Power-off leakage current		I _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0		10.0	μΑ
Quioccont cupply current		Lan	$V_{IN} = V_{CC}$ or GND		2.7 to 3.6		10.0	
Quiescerit supply c	unciii	Icc	V _{IN} = 3.6 to 5.5 V		2.7 to 3.6	_	±10.0	μΑ
Increase in I _{CC} per input		Δl _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	_	500	



AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition		Min	Max	Unit
Ondidotoristics	Cymbol	rest condition	V _{CC} (V)	IVIIII		
Maximum clock frequency	f	Figure 1, Figure 2	2.7	_	_	MHz
iviaximum clock frequency	f _{max}	Figure 1, Figure 2	3.3 ± 0.3	150	_	
Propagation delay time	t _{pLH}	Figure 1, Figure 2	2.7	_	8.0	
$(CK-Q, \overline{Q})$	t _{pHL}	Figure 1, Figure 2	3.3 ± 0.3	1.5	7.0	ns
Propagation delay time	t _{pLH}	Figure 1 Figure 4	2.7	_	8.0	- ns
$(\overline{CLR},\overline{PR}-Q,\overline{Q})$	t _{pHL}	Figure 1, Figure 4	3.3 ± 0.3	1.5	7.0	
Minimum pulse width	t _W (H)	Figure 4 Figure 2	2.7	3.3	_	ns ns
(CK)	t _W (L)	Figure 1, Figure 2	3.3 ± 0.3	3.3	_	
Minimum pulse width	4 (1)		2.7	3.6	_	- ns
(CLR , PR)	t _W (L)	Figure 1, Figure 4	3.3 ± 0.3	3.3	_	
Minimum actual time	4	Figure 1, Figure 2	2.7	2.5	_	20
Minimum setup time	t _s	Figure 1, Figure 2	3.3 ± 0.3	2.5	_	ns
Minimum hold time		Figure 1, Figure 2	2.7	1.5	_	ns
IVIII III TIOIA IIITIE	t _h		3.3 ± 0.3	1.5	_	
Minimum removal time	t _{rem}	Figure 4 Figure 0	2.7	3.0	_	ns
Minimum removal time		Figure 1, Figure 3	3.3 ± 0.3	2.5	_	
Output to output alcow	t _{osLH}	4142	2.7	_	_	no
Output to output skew	t _{osHL}	(Note 10)	3.3 ± 0.3	_	1.0	ns

Note 10: Parameter guaranteed by design. $(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, \, t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$

Dynamic Switching Characteristics

 $(Ta = 25^{\circ}C, input: t_r = t_f = 2.5 \text{ ns}, C_L = 50 \text{ pF}, R_L = 500 \Omega)$

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	٧
Quiet output minimum dynamic V _{OL}	V _{OLV}	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Тур.	Unit
Input capacitance	C _{IN}	_	3.3	7	pF
Output capacitance	C _{OUT}	_	0	8	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note 11)	3.3	25	pF

Note 11: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

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Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$

AC Test Circuit

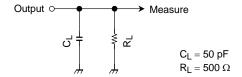


Figure 1

AC Waveform

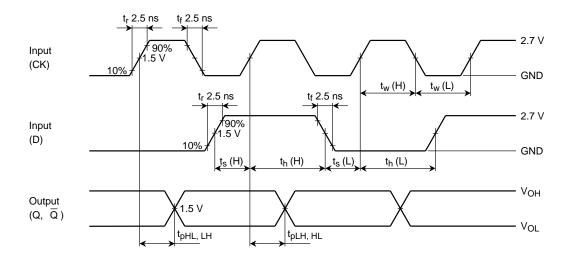


Figure 2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

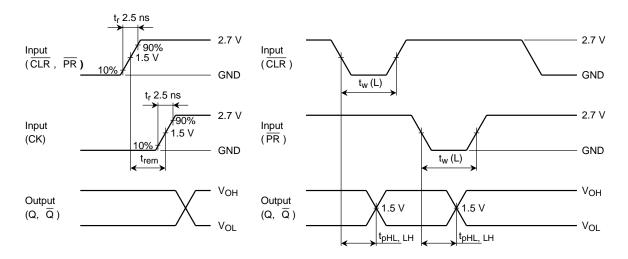
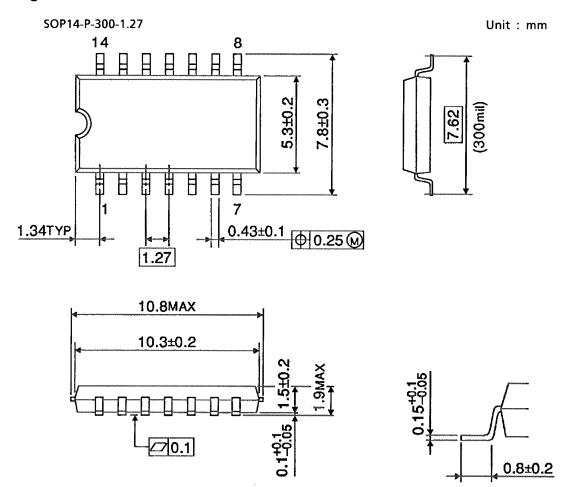


Figure 3 t_{rem}

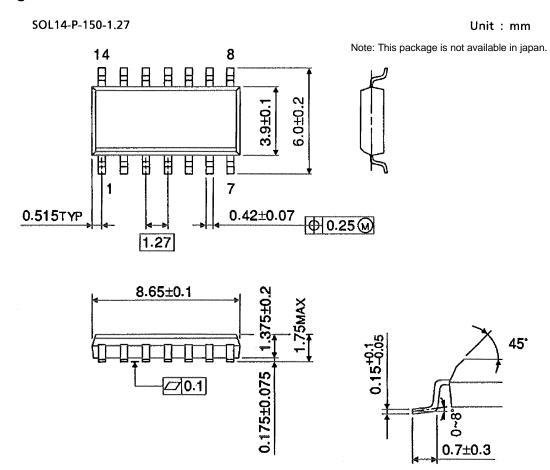
Figure 4 t_{pLH}, t_{pHL}

Package Dimensions



Weight: 0.18 g (typ.)

Package Dimensions

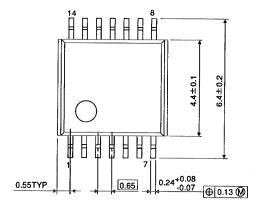


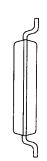
Weight: 0.12 g (typ.)

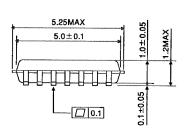
Unit: mm

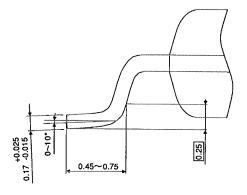
Package Dimensions

TSSOP14-P-0044-0.65









Weight: 0.06 g (typ.)

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