

# TC74HC237AP, TC74HC237AF

## 3-to-8 Line Decoder/Latch

The TC74HC237A is a high speed CMOS 3-to-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is composed of a 3-bit input latches with a common  $\overline{GL}$  enable input and 3-to-8 line decoder with enable inputs  $G1$  and  $\overline{G2}$ . The 3-bit binary data is stored into the input latch on the high level of  $\overline{GL}$ . The value of this data determines which one of the outputs will go low.

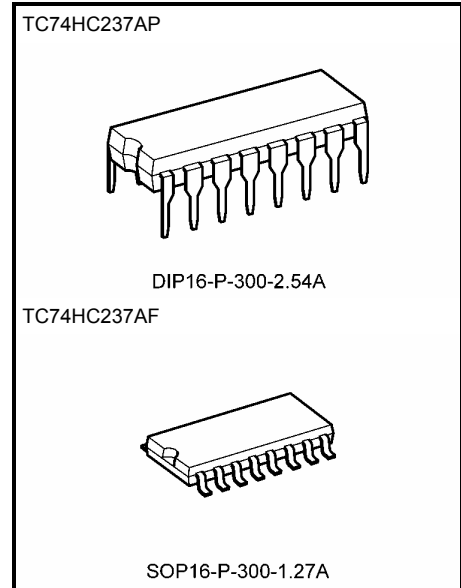
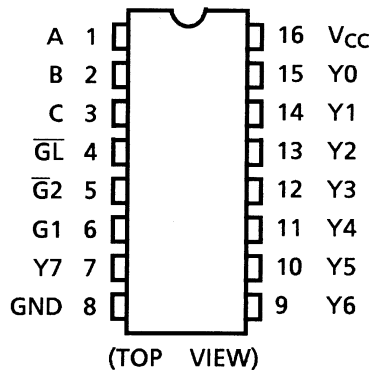
When the enable input  $G1$  is held low or  $\overline{G2}$  is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application address decoder for memory system.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $t_{pd} = 12 \text{ ns}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2\sim 6 \text{ V}$
- Pin and function compatible with 74LS237

### Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

## IEC Logic Symbol

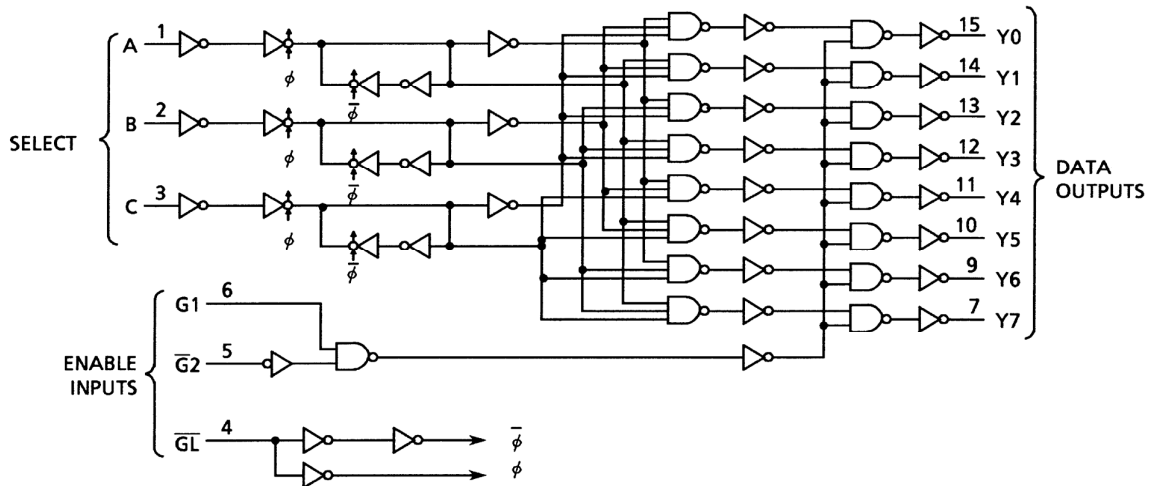


## Truth Table

Inputs						Outputs							
Enable			Address			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
$\overline{G1}$	$\overline{G2}$	G1	C	B	A								
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	H	L	L	L	L	H	L	L	L
L	L	H	H	H	L	L	L	L	L	L	H	L	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	Depends upon the address previously applied while $\overline{G1}$ was at a low level							

X: Don't care

## System Diagram



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5~7	V
DC input voltage	$V_{IN}$	-0.5~ $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5~ $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65~150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}C$ . From  $T_a = 65$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2~6	V
Input voltage	$V_{IN}$	0~ $V_{CC}$	V
Output voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating temperature	$T_{opr}$	-40~85	$^{\circ}C$
Input rise and fall time	$t_r, t_f$	0~1000 ( $V_{CC} = 2.0$ V) 0~500 ( $V_{CC} = 4.5$ V) 0~400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

**Electrical Characteristics**

**DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V <sub>IL</sub>	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
			I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -5.2 mA	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
			I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 5.2 mA	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	—	—	4.0	—	40.0	μA

**Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)**

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40~85°C	Unit	
				V <sub>CC</sub> (V)	Typ.	Limit		Limit
Minimum pulse width ( $\overline{GL}$ )	t <sub>w</sub> (L)	—		2.0	—	75	95	ns
				4.5	—	15	19	
				6.0	—	13	16	
Minimum set-up time (A, B, C- $\overline{GL}$ )	t <sub>s</sub>	—		2.0	—	50	65	ns
				4.5	—	10	13	
				6.0	—	9	11	
Minimum hold time (A, B, C- $\overline{GL}$ )	t <sub>h</sub>	—		2.0	—	25	30	ns
				4.5	—	5	6	
				6.0	—	5	5	

### AC Characteristics ( $C_L = 15 \text{ pF}$ , $V_{CC} = 5 \text{ V}$ , $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	4	8	ns
Propagation delay time (G1-Y)	$t_{pLH}$ $t_{pHL}$	—	—	12	24	ns
Propagation delay time ( $\overline{G2}$ -Y)	$t_{pLH}$ $t_{pHL}$	—	—	12	24	ns
Propagation delay time ( $\overline{GL}$ -Y)	$t_{pLH}$ $t_{pHL}$	—	—	17	33	ns
Propagation delay time (A, B, C-Y)	$t_{pLH}$ $t_{pHL}$	—	—	15	31	ns

### AC Characteristics ( $C_L = 50 \text{ pF}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		Unit	
			$V_{CC} \text{ (V)}$	Min	Typ.	Max	Min		Max
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (G1-Y)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	45	140	—	175	ns
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Propagation delay time ( $\overline{G2}$ -Y)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	45	140	—	175	ns
			4.5	—	15	28	—	35	
			6.0	—	13	24	—	30	
Propagation delay time ( $\overline{GL}$ -Y)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	65	190	—	240	ns
			4.5	—	21	38	—	48	
			6.0	—	18	32	—	41	
Propagation delay time (A, B, C-Y)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	60	180	—	225	ns
			4.5	—	19	36	—	45	
			6.0	—	16	31	—	38	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	52	—	—	—	pF	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

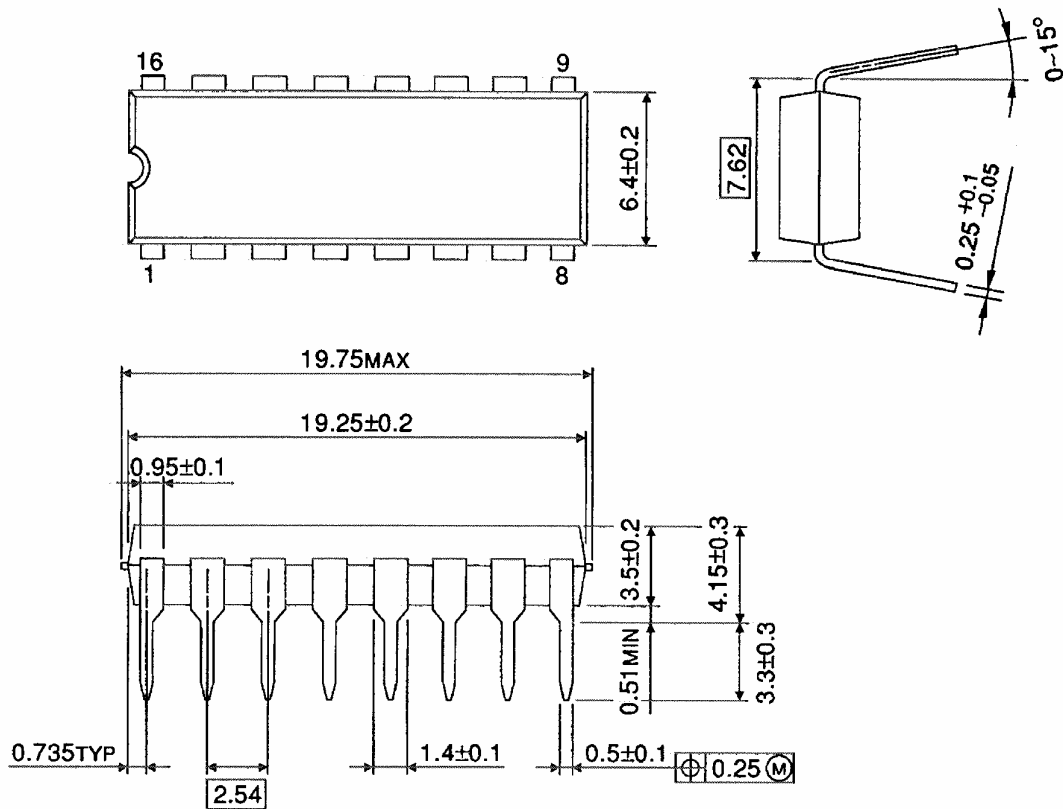
$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

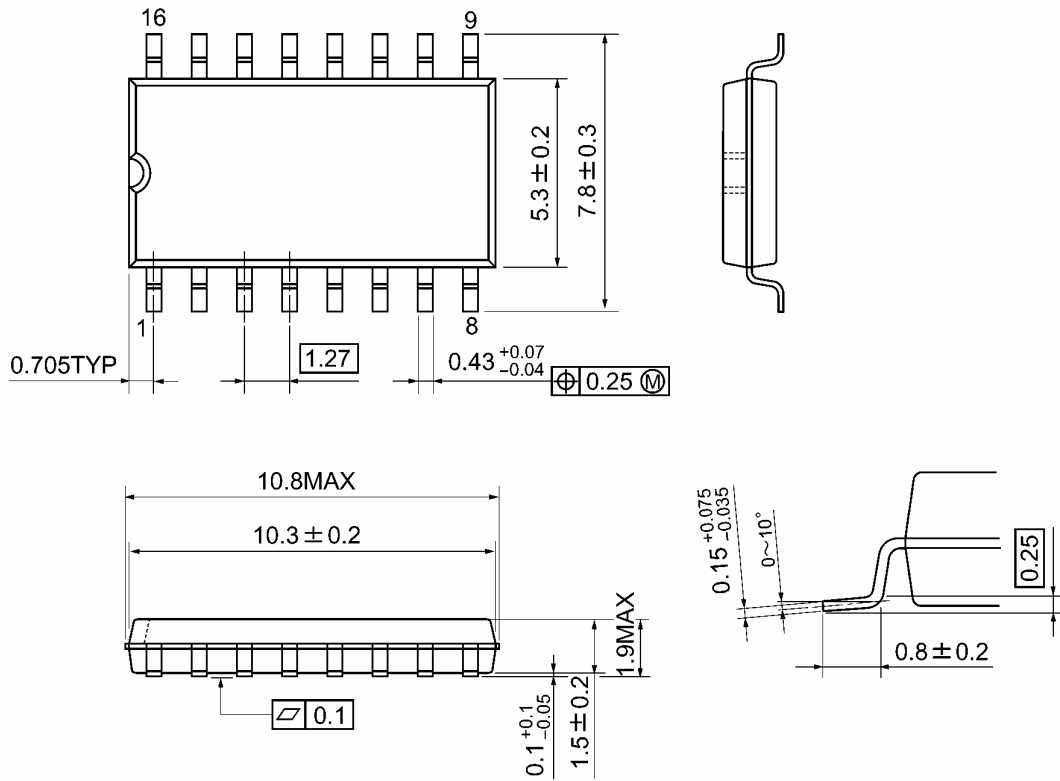


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)



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20070701-EN GENERAL

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