TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HCT646AP

Octal Bus Transceiver/Register (3-state)

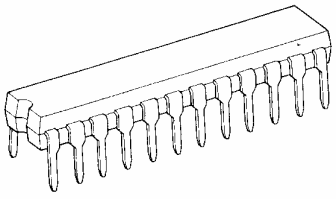
The TC74HCT646A is high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Its inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24-P-300-2.54

Weight: 1.50 g (typ.)

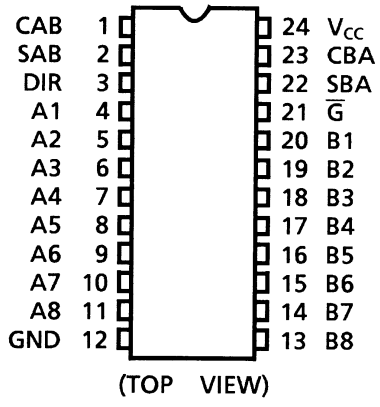
Features (Note 1)(Note 2)

- High speed: f_{max} = 60 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- Compatible with TTL output: V_{IH} = 2.0 V (min)
  V_{IL} = 0.8 V (max)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74LS646

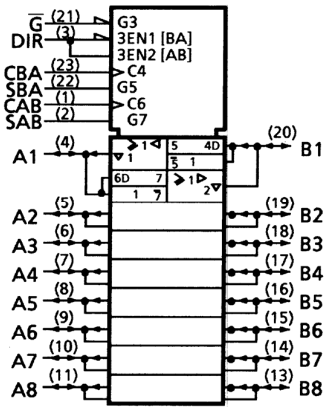
Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment



IEC Logic Symbol



Truth Table

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X (Note)	X (Note)	X	X	Inputs Z	Inputs Z	The output functions of A and B busses are disabled.
		↑	↑	X	X	X	X	Both A and B busses are used as inputs to the internal flip-flops. Data on the bus will be stored on the rising edge of the clock.
L	H	X (Note)	X (Note)	L	X	Inputs L H	Outputs L H	The data on the A bus are displayed on the B bus.
		↑	X (Note)	L	X	L H	L H	The data on the A bus are displayed on the B bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X (Note)	X (Note)	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B bus.
		↑	X (Note)	H	X	L H	L H	The data on the A bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B bus.
L	L	X (Note)	X (Note)	X	L	Outputs L H	Inputs L H	The data on the B bus are displayed on the A bus.
		X (Note)	↑	X	L	L H	L H	The data on the B bus are displayed on the A bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X (Note)	X (Note)	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A bus.
		X (Note)	↑	X	H	L H	L H	The data on the B bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A bus.

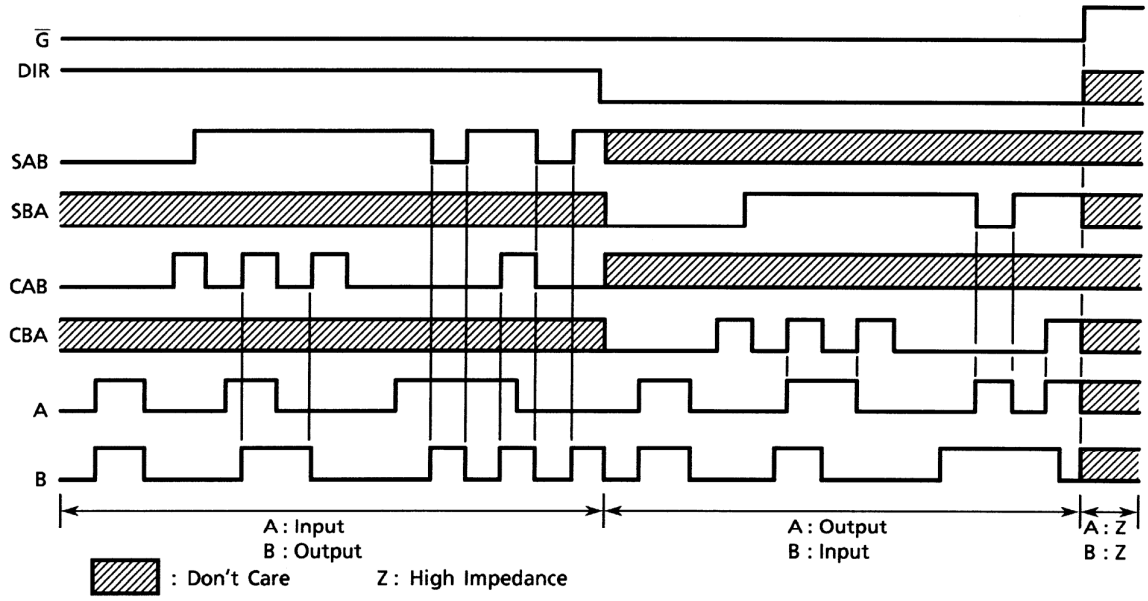
X: Don't care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

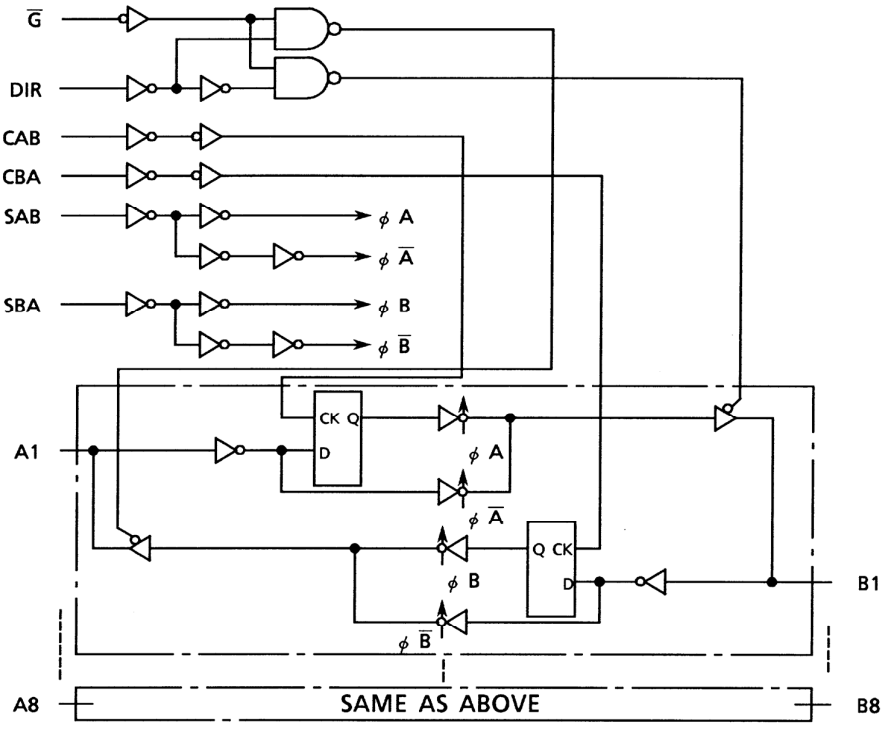
Z: High impedance

Note: The clock are not internally gated with either $\overline{G}$ or DIR. Therefore, data on the A and/or B busses may be clocked into the storage flip-flops at any time.

Timing Chart



System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7.0	V
DC input voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)	mW
Storage temperature	T_{stg}	−65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~V_{CC}	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	t_r, t_f	0~500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = –40~85°C Min	Ta = –40~85°C Max	Unit
High-level input voltage	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –20 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = –6 mA	4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
3-state output off state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_C	Per input: V_{IN} = 0.5 V or 2.4 V Other input: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = –40 ~85°C Limit	Unit
Minimum pulse width (CK)	$t_{W(L)}$	—	4.5	—	15	19	ns
	$t_{W(H)}$		5.5	—	14	17	
Minimum set-up time	t_s	—	4.5	—	10	13	ns
			5.5	—	9	12	
Minimum hold time	t_h	—	4.5	—	5	5	ns
			5.5	—	5	5	
Clock frequency	f	—	4.5	—	31	25	MHz
			5.5	—	37	30	

AC Characteristics (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	4.5	—	7	12	—	15	ns
				5.5	—	6	11	—	14	
Propagation delay time (BUS-bus)	t_{pLH} t_{pHL}	—	50	4.5	—	20	30	—	38	ns
				5.5	—	17	27	—	34	
			150	4.5	—	25	38	—	48	
				5.5	—	22	34	—	43	
Propagation delay time (CAB, CBA-bus)	t_{pLH} t_{pHL}	—	50	4.5	—	29	44	—	55	ns
				5.5	—	26	40	—	50	
			150	4.5	—	34	52	—	65	
				5.5	—	31	47	—	59	
Propagation delay time (SAB, SBA-bus)	t_{pLH} t_{pHL}	—	50	4.5	—	24	34	—	43	ns
				5.5	—	21	31	—	39	
			150	4.5	—	29	42	—	53	
				5.5	—	26	38	—	46	
Output enable time ($\overline{G}$-bus)	t_{pZL} t_{pZH}	$R_L = 1$ kΩ	50	4.5	—	26	38	—	48	ns
				5.5	—	23	34	—	43	
			150	4.5	—	31	46	—	58	
				5.5	—	28	41	—	52	
Output disable time ($\overline{G}$-bus)	t_{pLZ} t_{pHZ}	$R_L = 1$ kΩ	50	4.5	—	26	35	—	44	ns
				5.5	—	23	32	—	40	
Maximum clock frequency	f_{max}	—	50	4.5	31	55	—	25	—	MHz
				5.5	37	61	—	30	—	
Input capacitance	C_{IN}	DIR, $\overline{G}$, SAB, SBA, CAB, CBA			—	5	10	—	10	pF
Output capacitance	$C_{I/O}$	An, Bn			—	13	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	40	—	—	—	pF

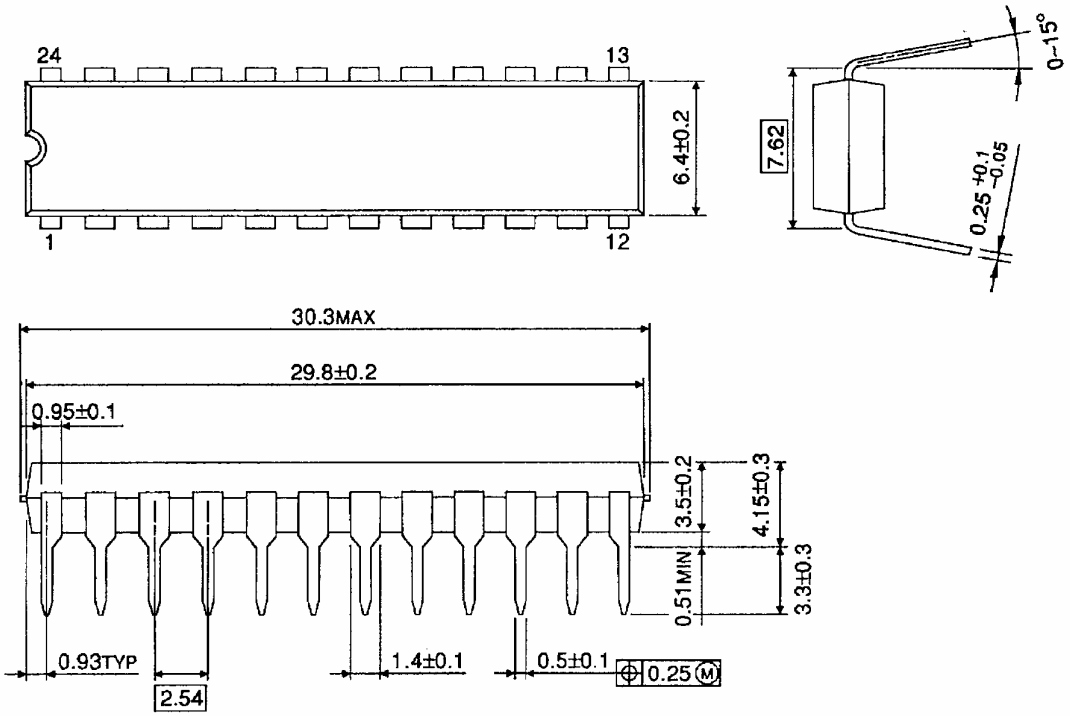
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8\ (per\ bit)$$

Package Dimensions

DIP24-P-300-2.54 Unit : mm



Weight: 1.50 g (typ.)

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20070701-EN GENERAL

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