

**TC74ACT74P,TC74ACT74F,TC74ACT74FN,TC74ACT74FT**

Dual D-Type Flip Flop with Preset and Clear

The TC74ACT74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

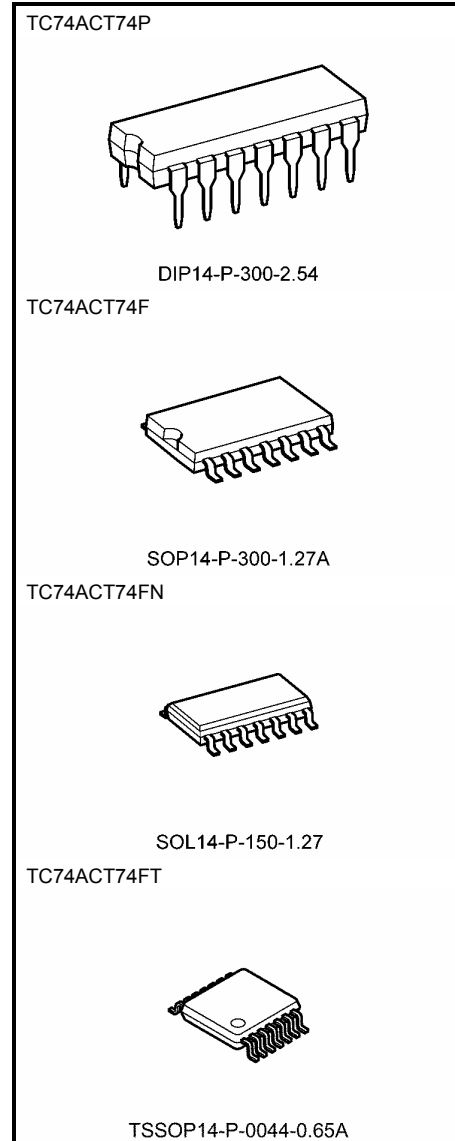
CLR and PR are independent of the CK and are accomplished by setting the appropriate input to an "L" level.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**Features**

- High speed:  $f_{max} = 180 \text{ MHz (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs:  $V_{IL} = 0.8 \text{ V (max)}$   
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$   
Capability of driving  $50 \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F74

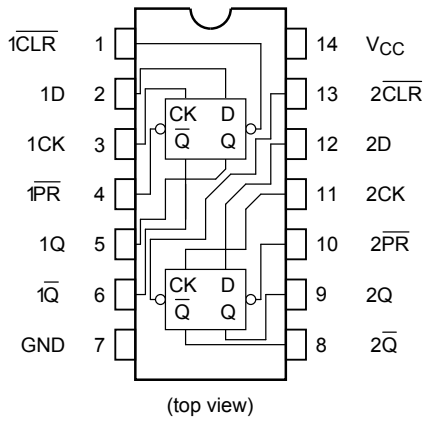
Note: xxxFN (JEDEC SOP) is not available in Japan.



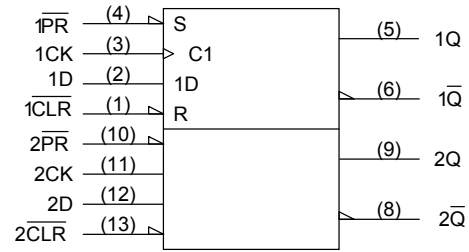
Weight

DIP14-P-300-2.54	: 0.96 g (typ.)
SOP14-P-300-1.27A	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

## Pin Assignment



## IEC Logic Symbol

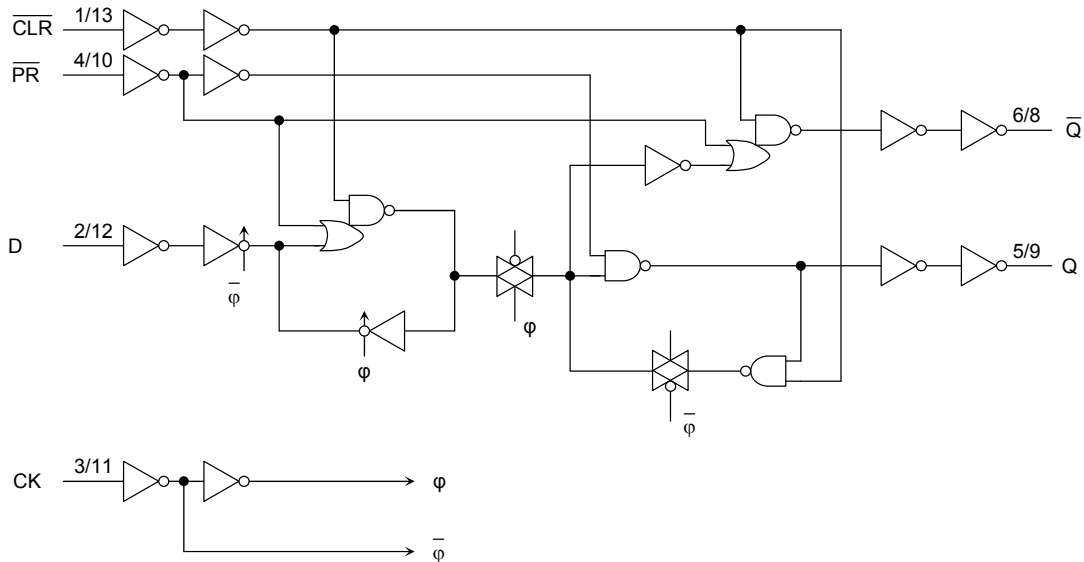


## Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q-bar	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q <sub>n</sub> -bar	No Change

X: Don't care

## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 50$	mA
DC output current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $T_a = -40^{\circ}C$  to  $65^{\circ}C$ . From  $T_a = 65^{\circ}C$  to  $85^{\circ}C$  a derating factor of  $-10$  mW/ $^{\circ}C$  should be applied up to 300 mW.

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	4.5 to 5.5	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V <sub>IL</sub>	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	4.5	4.4	4.5	—	4.4	—	V
			I <sub>OH</sub> = -24 mA	4.5	3.94	—	—	3.80	—	
			I <sub>OH</sub> = -75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 24 mA	4.5	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 75 mA (Note)	5.5	—	—	—	—	1.65	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA
	I <sub>C</sub>	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Limit	
Minimum pulse width (CK)	t <sub>w</sub> (L)	—		5.0 ± 0.5	5.0	5.0
	t <sub>w</sub> (H)	—				
Minimum pulse width ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	t <sub>w</sub> (L)	—		5.0 ± 0.5	5.7	6.5
Minimum set-up time	t <sub>s</sub>	—		5.0 ± 0.5	3.5	3.5
Minimum hold time	t <sub>h</sub>	—		5.0 ± 0.5	1.5	1.5
Minimum removal time ( $\overline{\text{CLR}}$ , $\overline{\text{PR}}$ )	t <sub>rem</sub>	—		5.0 ± 0.5	2.0	2.0

## AC Characteristics ( $C_L = 50 \text{ pF}$ , $R_L = 500 \text{ } \Omega$ , input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
Propagation delay time (CK-Q, $\bar{Q}$ )	t <sub>pLH</sub>	—	5.0 ± 0.5	—	6.1	9.2	1.0	10.5	ns
	t <sub>pHL</sub>	—	5.0 ± 0.5	—	6.5	10.1	1.0	11.5	
Propagation delay time ( $\bar{\text{CLR}}$ , $\bar{\text{PR}}$ -Q, $\bar{Q}$ )	t <sub>pLH</sub>	—	5.0 ± 0.5	—	6.5	10.1	1.0	11.5	ns
	t <sub>pHL</sub>	—	5.0 ± 0.5	—	6.5	10.1	1.0	11.5	
Maximum clock frequency	f <sub>max</sub>	—	5.0 ± 0.5	95	160	—	95	—	MHz
Input capacitance	C <sub>IN</sub>	—	—	5	10	—	10	—	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note)	—	35	—	—	—	—	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

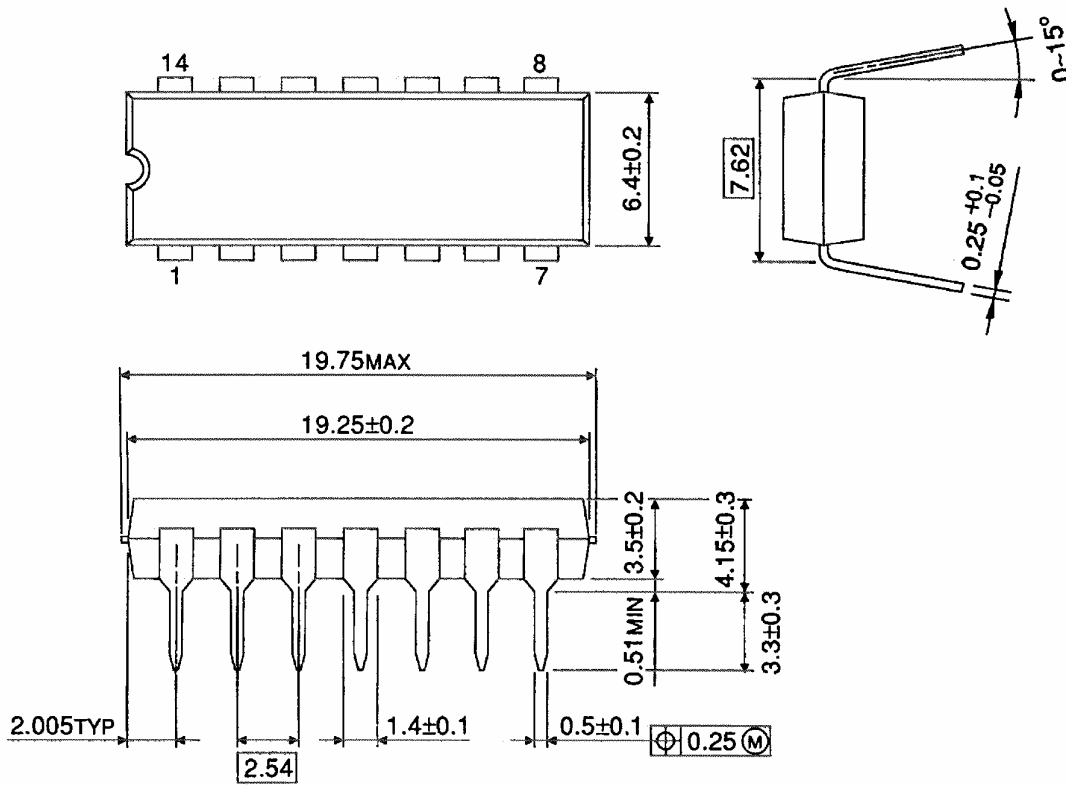
Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

## Package Dimensions

DIP14-P-300-2.54

Unit : mm

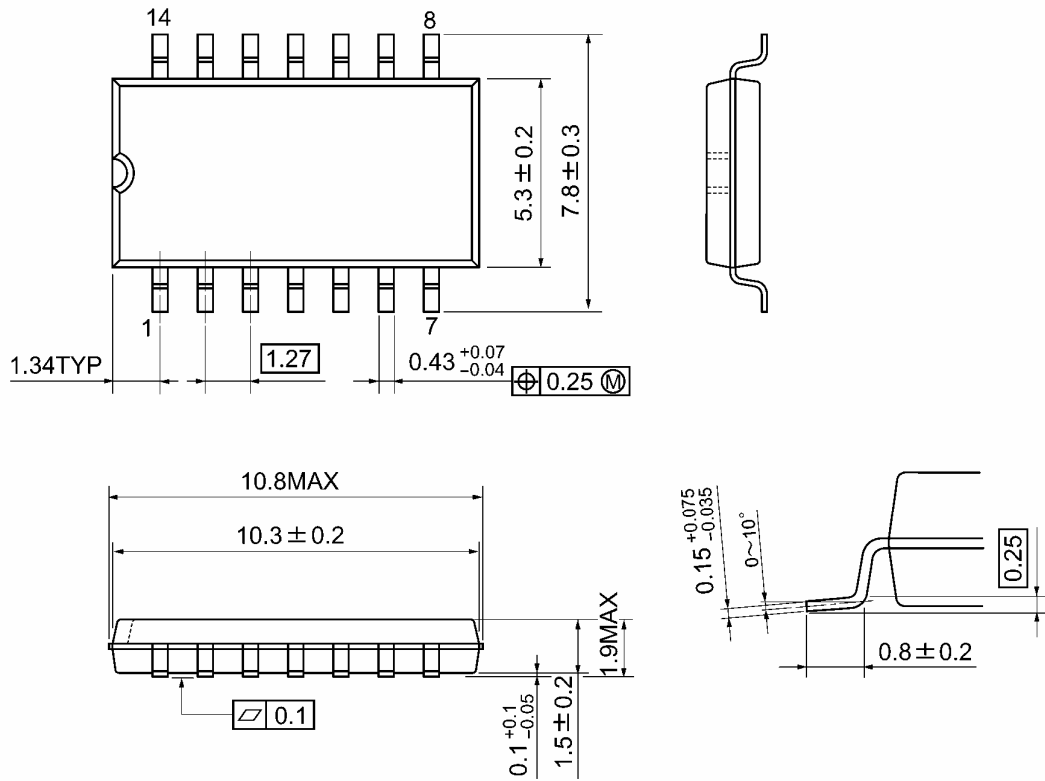


Weight: 0.96 g (typ.)

## Package Dimensions

SOP14-P-300-1.27A

Unit: mm

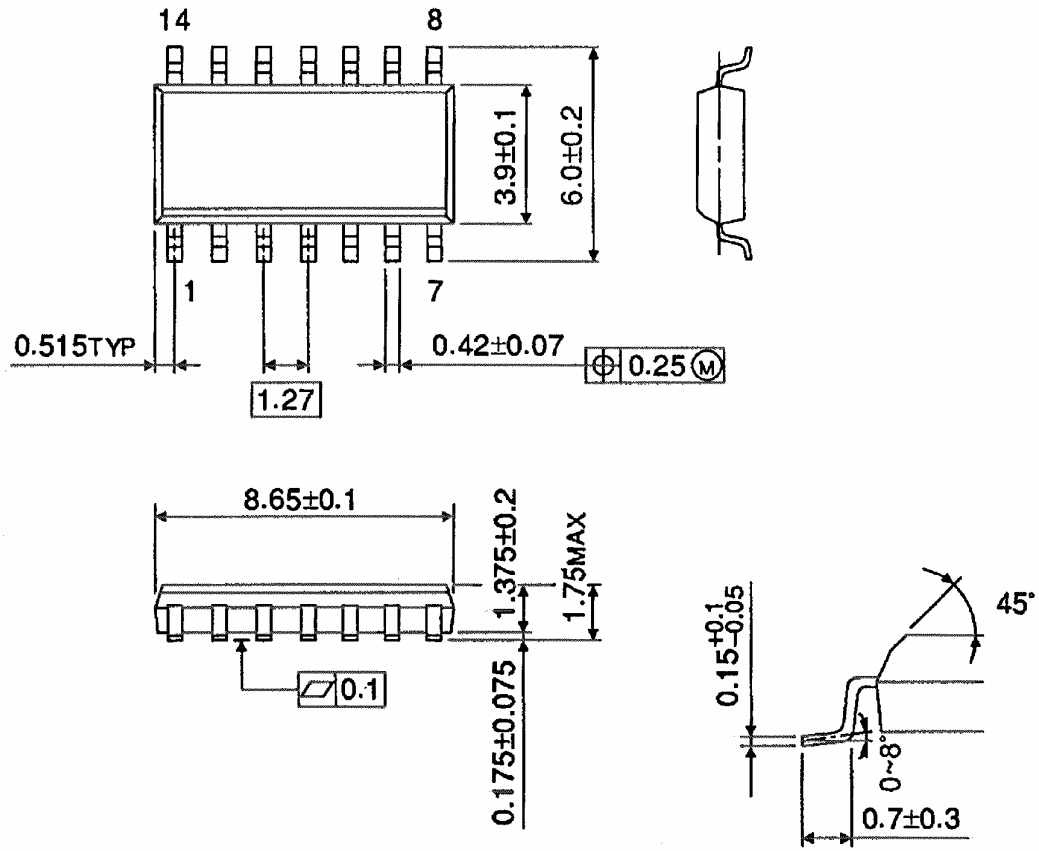


Weight: 0.18 g (typ.)

## Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

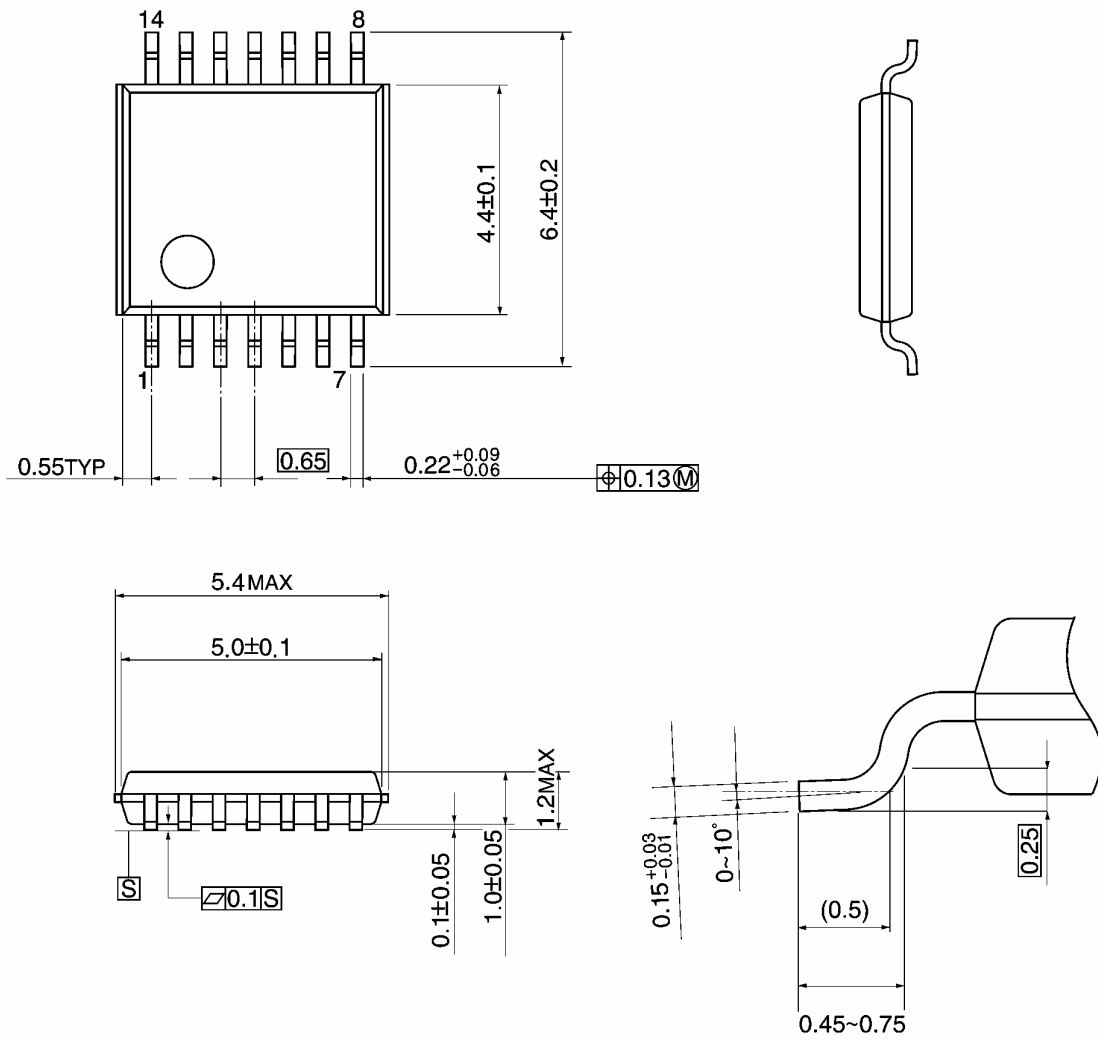
Weight: 0.12 g (typ.)



## Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



Weight: 0.06 g (typ.)

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20070701-EN GENERAL

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