TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74ACT574P,TC74ACT574F,TC74ACT574FT

### Octal D-Type Flip-Flop with 3-State Output

The TC74ACT574 is an advanced high speed CMOS OCTAL FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

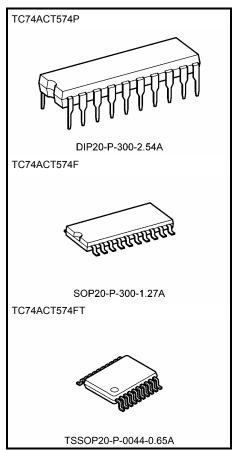
These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

#### **Features**

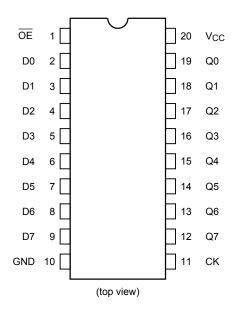
- High speed:  $f_{max} = 180 \text{ MHz}$  (typ.) at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $ICC = 8 \mu A$  (max) at Ta = 25°C
- Compatible with TTL outputs: VIL = 0.8 V (max), VIH = 2.0 V (min)
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 24 \text{ mA (min) Capability of driving 50 } \Omega$  transmission lines.
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74F574



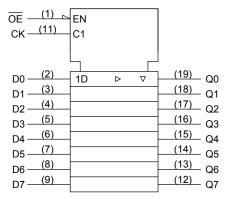
Weight

DIP20-P-300-2.54A : 1.30 g (typ.) SOP20-P-300-1.27A : 0.22 g (typ.) TSSOP20-P-0044-0.65A : 0.08 g (typ.)

## **Pin Assignment**



## **IEC Logic Symbol**



### **Truth Table**

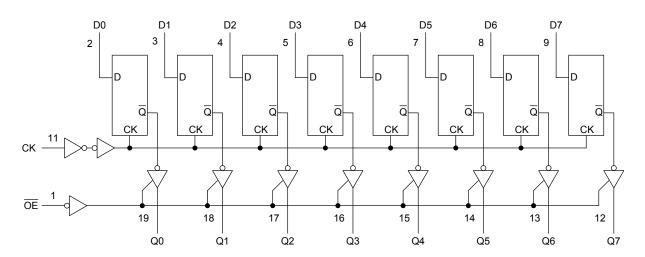
	Inputs	Output				
ŌE	CK	D	Q			
Н	Х	Х	Z			
L	$\neg$	Х	Qn			
L		L	L			
L		Н	Н			

X: Don't care

Z: High impedance

Q<sub>n</sub>: No change

### **System Diagram**



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### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	−0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	−0.5 to V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±50	mA
DC output current	lout	±50	mA
DC V <sub>CC</sub> /ground current	Icc	±200	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T <sub>stg</sub>	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

### **Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	4.5 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.



#### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics Symbol		Test Condition				Ta = 25°C				Ta = -40 to 85°C	
				V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Unit	
High-level input voltage	V <sub>IH</sub>		_			2.0	_	_	2.0	_	V
Low-level input voltage	V <sub>IL</sub>	_		4.5 to 5.5	_	_	0.8	_	0.8	V	
	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA		4.5	4.4	4.5	_	4.4	_	
High-level output voltage			I <sub>OH</sub> = −24 mA		4.5	3.94	_	_	3.80	_	V
			I <sub>OH</sub> = −75 mA	(Note)	5.5	_	_	_	3.85	_	
	VoL	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA		4.5	_	0.0	0.1	_	0.1	
Low-level output voltage			I <sub>OL</sub> = 24 mA		4.5	_	_	0.36	_	0.44	V
voltage			I <sub>OL</sub> = 75 mA	(Note)	5.5	_	_	_	_	1.65	
3-state output off-state current	loz	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	_	_	±0.5	_	±5.0	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_	_	±0.1	_	±1.0	μΑ	
Quiescent supply current	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_	_	8.0	_	80.0	μA	
	IC	Per input: V <sub>IN</sub> = 3.4 V Other input: V <sub>CC</sub> or GND		5.5	_	_	1.35	_	1.5	mA	

Note: This spec indicates the capability of driving 50  $\Omega$  transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

## Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Test Condition		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Limit	Limit	
Minimum pulse width	t <sub>w (H)</sub>	_	5.0 ± 0.5	5.0	5.0	ns
(CK)	t <sub>w (L)</sub>	_	5.0 1 0.5	5.0	5.0	2
Minimum set-up time	ts	_	$5.0 \pm 0.5$	3.0	3.0	ns
Minimum hold time	t <sub>h</sub>	_	5.0 ± 0.5	2.0	2.0	ns



### AC Characteristics ( $C_L = 50 \text{ pF}, R_L = 500 \Omega, \text{ input: } t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
	.,		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	
Propagation delay time (CK-Q)	t <sub>pLH</sub>	-	5.0 ± 0.5	_	6.2	10.1	1.0	11.5	ns
Output enable time	t <sub>pZL</sub> t <sub>pZH</sub>	_	5.0 ± 0.5	_	6.3	10.5	1.0	12.0	ns
Output disable time	<sup>t</sup> pLZ t <sub>pHZ</sub>	_	5.0 ± 0.5	_	6.6	9.6	1.0	11.0	ns
Maximum clock frequency	f <sub>max</sub>	_	5.0 ± 0.5	85	160	_	85	_	MHz
Input capacitance	C <sub>IN</sub>	_		_	5	10	_	10	pF
Output capacitance	C <sub>OUT</sub>	_		_	10	_	_	_	pF
Power dissipation capacitance	C <sub>PD</sub>		(Note)	_	33	_	_	_	pF

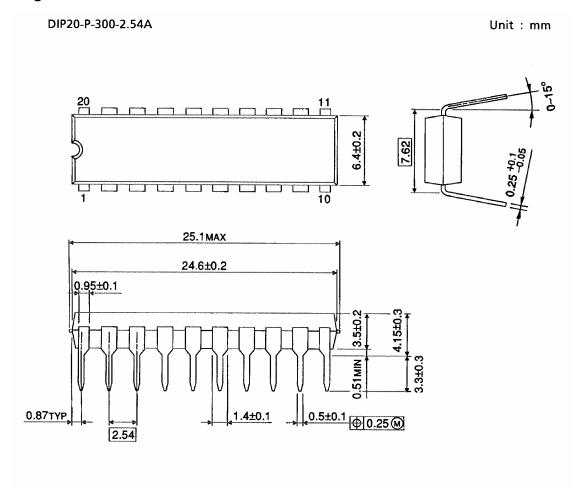
Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 (per F/F)$$

And the total C<sub>PD</sub> when n pcs. of F/F operate can be gained by the following equation:

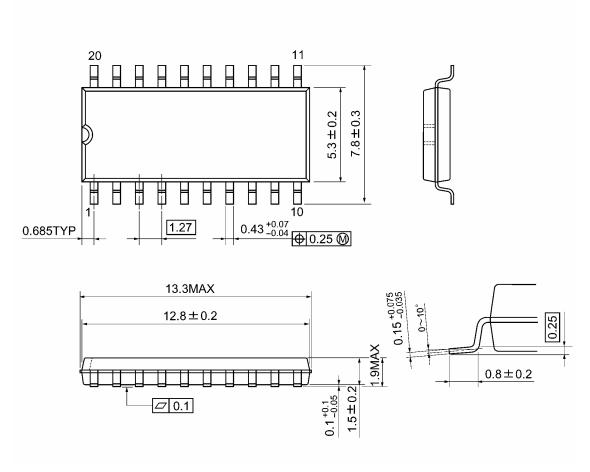
# **Package Dimensions**



Weight: 1.30 g (typ.)

# **Package Dimensions**

SOP20-P-300-1.27A Unit: mm



Weight: 0.22 g (typ.)

## **Package Dimensions**

TSSOP20-P-0044-0.65A Unit: mm  $6.4 \pm 0.2$  $0.22\substack{+0.09 \\ -0.06}$ 0.325TYP 0.65 <del>♦</del>0.13**M** 6.9MAX 6.5±0.1 1.2MAX 0.15 +0.03 0~10 1.0±0.05  $0.1\pm0.05$ S Ø.1S (0.5)0.45~0.75

Weight: 0.08 g (typ.)

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20070701-EN GENERAL

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