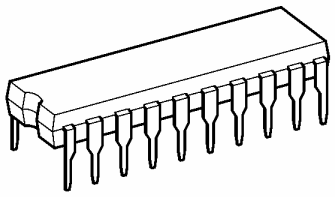
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74ACT299P,TC74ACT299F

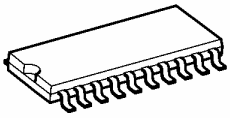
## 8-Bit PIPO Shift Register with Asynchronous Clear

TC74ACT299P



DIP20-P-300-2.54A

TC74ACT299F



SOP20-P-300-1.27A

Weight
DIP20-P-300-2.54A : 1.30 g (typ.)
SOP20-P-300-1.27A : 0.22 g (typ.)

The TC74ACT299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TLL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$ , $\overline{G2}$ ) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

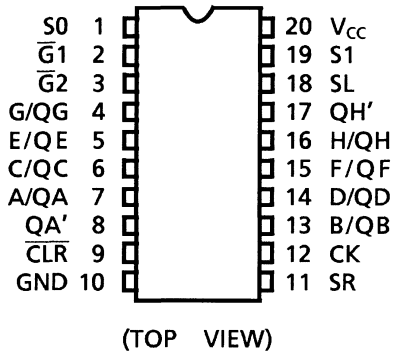
### Features (Note 1)(Note 2)

- High speed: $f_{max}$ = 130 MHz (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 8 μA (max) at Ta = 25°C
- Compatible with TTL outputs: $V_{IL}$ = 0.8 V (max)
  $V_{IH}$ = 2.0 V (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 24 mA (min)
  Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74F299

Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

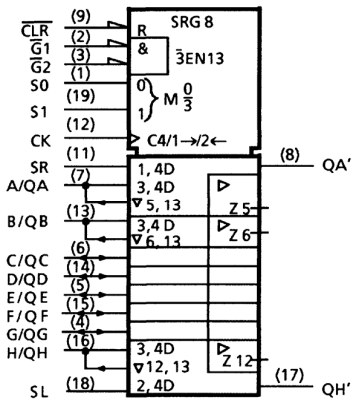
Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

### Pin Assignment




(TOP VIEW)

## IEC Logic Symbol




## Truth Table

| Mode | Inputs | | | | | | | | Inputs/ Outputs | | Outputs | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{CLR}$ | Function Select | | Outputs Control | | CK | Serial | | A/QA | H/QH | QA' | QH' |
| | | S1 | S0 | $\overline{G1}$ (Note) | $\overline{G2}$ (Note) | | SL | SR | | | | |
| Z | L | H | H | X | X | X | X | X | Z | Z | L | L |
| Clear | L | L | X | L | L | X | X | X | L | L | L | L |
| | L | X | L | L | L | X | X | X | L | L | L | L |
| Hold | H | L | L | L | L | X | X | X | QA0 | QH0 | QA0 | QH0 |
| Shift Right | H | L | H | L | L | ↑ | X | H | H | QGn | H | QGn |
| | H | L | H | L | L | ↑ | X | L | L | QGn | L | QGn |
| Shift Left | H | H | L | L | L | ↑ | H | X | QBn | H | QBn | H |
| | H | H | L | L | L | ↑ | L | X | QBn | L | QBn | L |
| Load | H | H | H | X | X | ↑ | X | X | a | h | a | h |

Note: When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z: High impedance

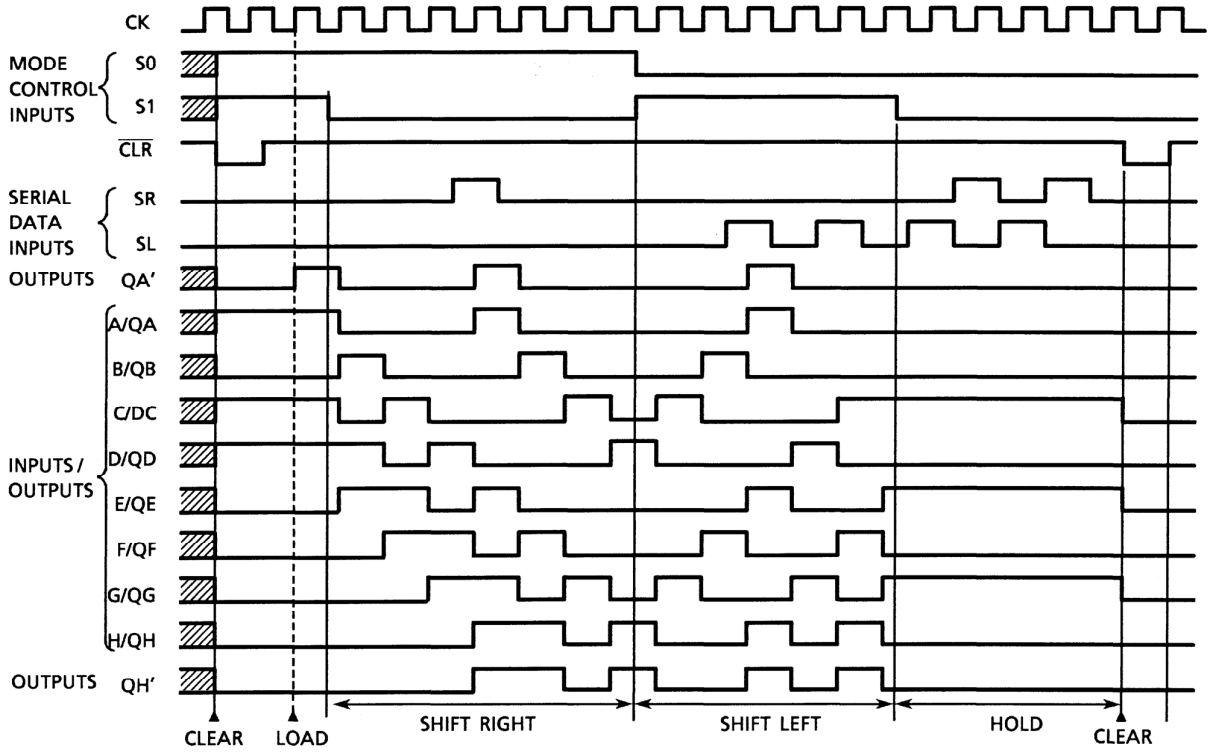
Qn0: The level of Qn before the indicated steady-state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by ↓ or ↑.

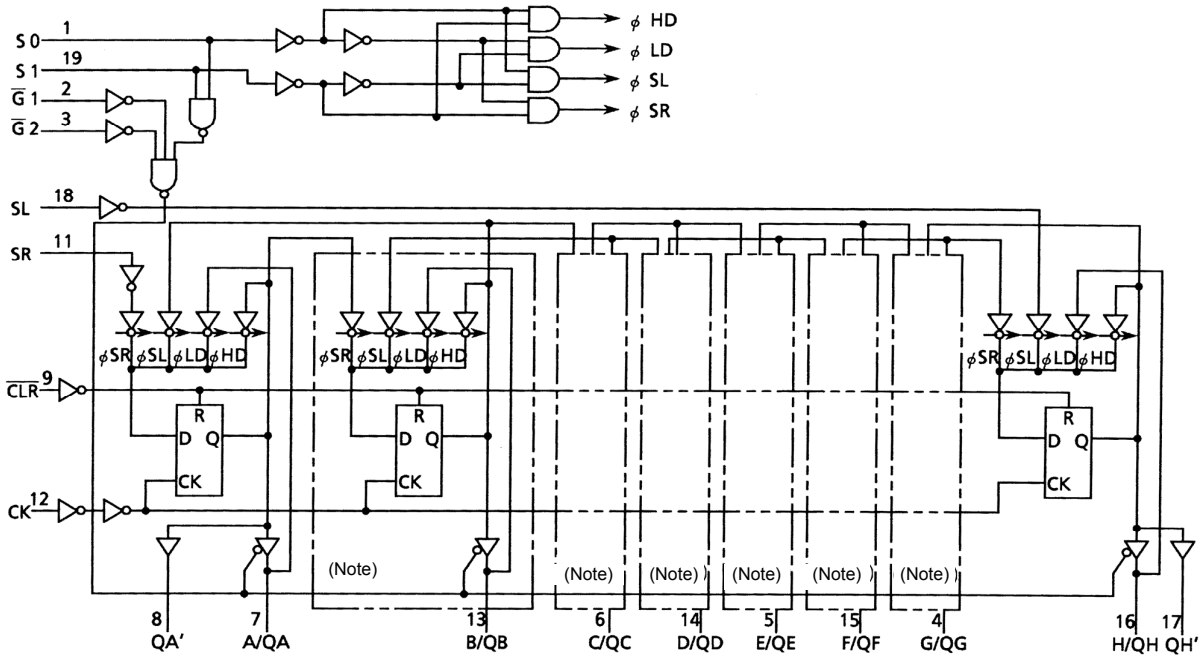
a, h: The level of the steady-state inputs A, H, respectively.

X: Don't care

## Timing Chart




## System Diagram




Note: Equivalent circuits

## Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | ±20 | mA |
| Output diode current | $I_{OK}$ | ±50 | mA |
| DC output current | $I_{OUT}$ | ±50 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±250 | mA |
| Power dissipation | $P_D$ | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 4.5 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Ta = 25°C Min | Ta = 25°C Typ. | Ta = 25°C Max | Ta = −40 to 85°C Min | Ta = −40 to 85°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 4.5 to 5.5 | 2.0 | — | — | 2.0 | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 4.5 to 5.5 | — | — | 0.8 | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 4.5 | 4.4 | 4.5 | — | 4.4 | — | V |
| | | | $I_{OH}$ = −24 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| | | | $I_{OH}$ = −75 mA (Note) | 5.5 | — | — | — | 3.85 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | $I_{OL}$ = 24 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 75 mA (Note) | 5.5 | — | — | — | — | 1.65 | |
| 3-state output off-state current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.5 | — | ±5.0 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 8.0 | — | 80.0 | μA |
| | $I_C$ | Per input: $V_{IN}$ = 3.4 V<br>Other input: $V_{CC}$ or GND | | 5.5 | — | — | 1.35 | — | 1.5 | mA |

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

### Timing Requirements (input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Ta = 25°C Typ. | Ta = 25°C Limit | Ta = −40 to 85°C Limit | Unit |
|---|---|---|---|---|---|---|---|
| Minimum pulse width (CK) | $t_{W(L)}$<br>$t_{W(H)}$ | — | 5.0 ± 0.5 | — | 5.0 | 5.0 | ns |
| Minimum pulse width ($\overline{CLR}$) | $t_{W(L)}$ | — | 5.0 ± 0.5 | — | 5.0 | 5.0 | ns |
| Minimum set-up time (SL, SR, A~H) | $t_s$ | — | 5.0 ± 0.5 | — | 3.5 | 3.5 | ns |
| Minimum set-up time (S0, S1) | $t_s$ | — | 5.0 ± 0.5 | — | 6.0 | 6.5 | ns |
| Minimum hold time (SL, SR, A~H) | $t_h$ | — | 5.0 ± 0.5 | — | 2.0 | 2.0 | ns |
| Minimum hold time (S0, S1) | $t_h$ | — | 5.0 ± 0.5 | — | 0.0 | 0.0 | ns |
| Minimum removal time ($\overline{CLR}$) | $t_{rem}$ | — | 5.0 ± 0.5 | — | 2.0 | 2.0 | ns |

**AC Characteristics ($C_L$ = 50 pF, $R_L$ = 500 Ω, input: $t_r = t_f$ = 3 ns)**

| Characteristics | Symbol | Test Condition | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (CK-QA', QH') | $t_{pLH}$ $t_{pHL}$ | 5.0 ± 0.5 | — | 7.2 | 10.5 | 1.0 | 12.0 | ns |
| Propagation delay time ($\overline{CLR}$ -QA', QH') | $t_{pHL}$ | 5.0 ± 0.5 | — | 6.0 | 10.0 | 1.0 | 11.5 | ns |
| Propagation delay time (CK-QA~QH) | $t_{pLH}$ $t_{pHL}$ | 5.0 ± 0.5 | — | 7.4 | 11.4 | 1.0 | 13.0 | ns |
| Propagation delay time ($\overline{CLR}$ -QA~QH) | $t_{pHL}$ | 5.0 ± 0.5 | — | 6.3 | 10.5 | 1.0 | 12.0 | ns |
| Output enable time | $t_{pZL}$ $t_{pZH}$ | 5.0 ± 0.5 | — | 7.4 | 11.4 | 1.0 | 13.0 | ns |
| Output disable time | $t_{pLZ}$ $t_{pHZ}$ | 5.0 ± 0.5 | — | 7.2 | 9.6 | 1.0 | 11.0 | ns |
| Maximum clock frequency | $f_{max}$ | 5.0 ± 0.5 | 80 | 120 | — | 80 | — | MHz |
| Input capacitance | $C_{IN}$ | — | — | 5 | 10 | — | 10 | pF |
| Bus input capacitance | $C_{I/O}$ | — | — | 13 | — | — | — | pF |
| Power dissipation capacitance | $C_{PD}$ (Note) | — | — | 160 | — | — | — | pF |

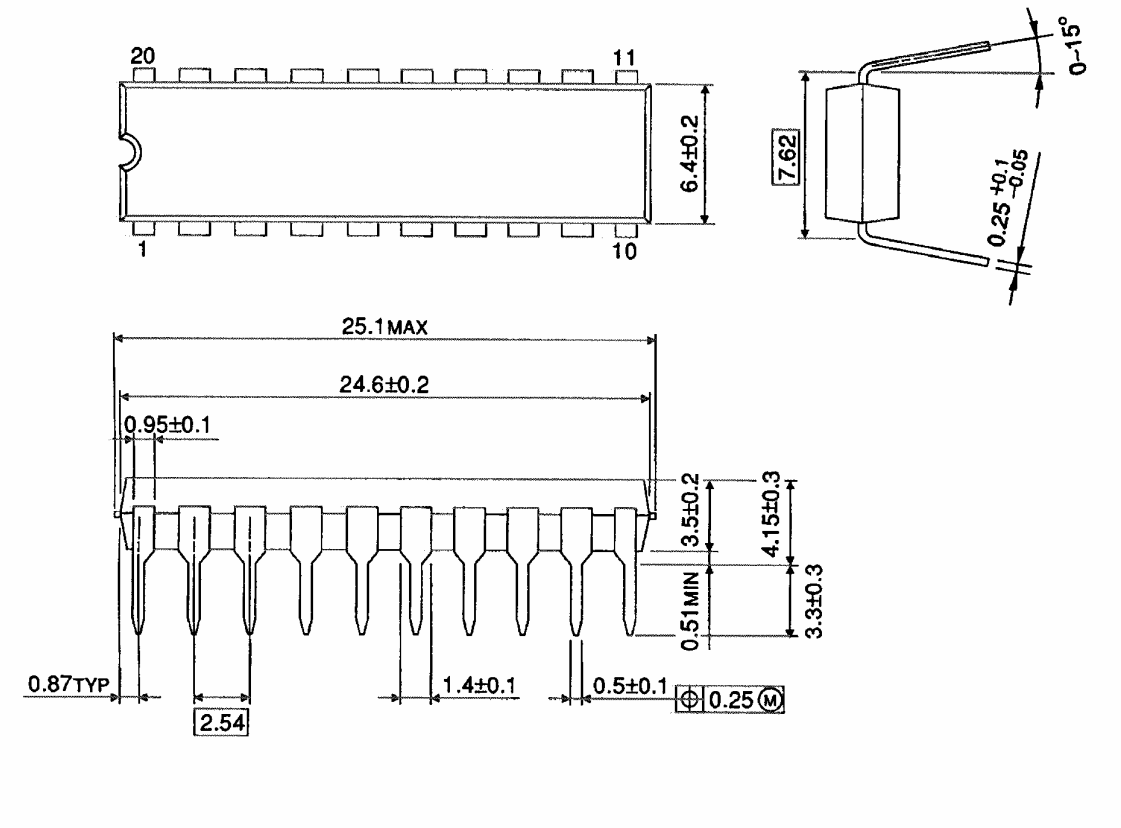
Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\,(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Package Dimensions

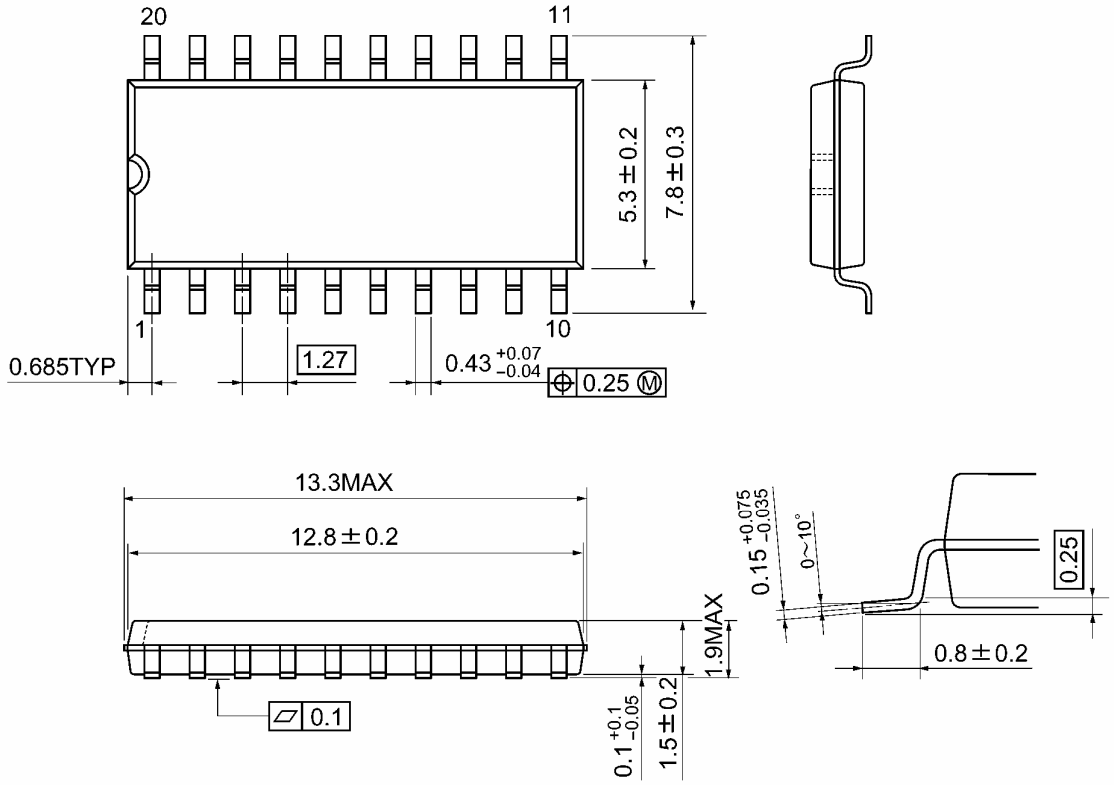
DIP20-P-300-2.54A Unit : mm




Weight: 1.30 g (typ.)

## Package Dimensions

SOP20-P-300-1.27A Unit: mm




Weight: 0.22 g (typ.)

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20070701-EN GENERAL

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