

TC74VHC574F, TC74VHC574FW, TC74VHC574FT

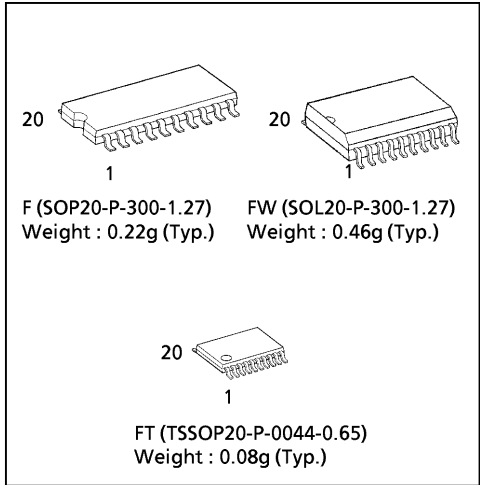
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

(Note) The JEDEC SOP (FW) is not available in Japan.

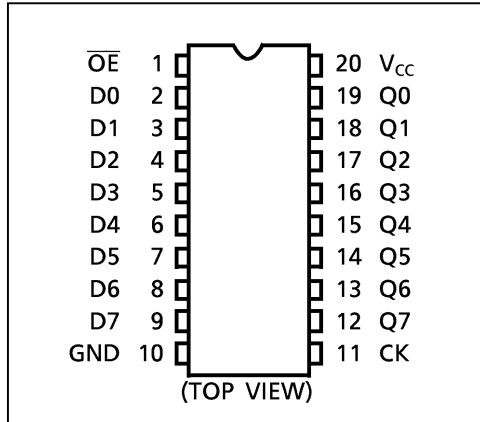
The TC74VHC574 is advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8-bit D-type flip-flop is controlled by a clock input (CK) and a output enable input (\overline{OE}). When the \overline{OE} input is high, the eight outputs are in a high impedance state. An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

- High Speed..... $f_{MAX} = 180\text{MHz}(\text{typ.})$
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise..... $V_{OLP} = 1.2\text{V} (\text{Max.})$
- Pin and Function Compatible with 74ALS574



PIN ASSIGNMENT

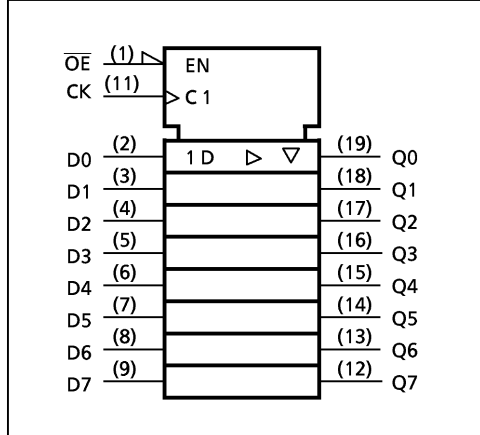


TRUTH TABLE

INPUTS			OUTPUT
\overline{OE}	CK	D	Q
H	X	X	Z
L		X	Q_n
L		L	L
L		H	H

X : Don't Care
Z : High Impedance
 Q_n : No Change

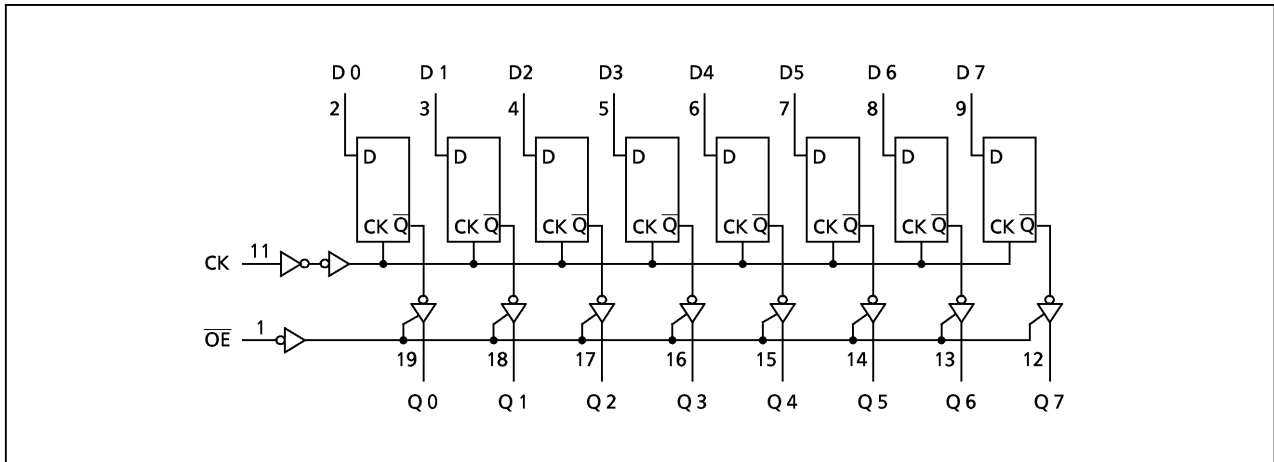
IEC LOGIC SYMBOL



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SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns/V

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DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V _{IH}		2.0 3.0~ 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	—	V	
Low - Level Input Voltage	V _{IL}		2.0 3.0~ 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V	
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			I _{OH} = -4mA I _{OH} = -8mA	3.0	2.58	—	—	2.48	—	
				4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
			I _{OL} = 4mA I _{OL} = 8mA	3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
3 - State Output Off - State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	5.5	—	—	± 0.25	—	± 2.50	μA	
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	0~5.5	—	—	± 0.1	—	± 1.0		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	5.5	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _{W(H)} t _{W(L)}		3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum Set-up Time	t _s		3.3 ± 0.3	—	3.5	3.5	
			5.0 ± 0.5	—	3.5	3.5	
Minimum Hold Time	t _h		3.3 ± 0.3	—	1.5	1.5	
			5.0 ± 0.5	—	1.5	1.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time (CK-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	8.5	13.2	1.0	15.5	ns
				50	—	11.0	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
				50	—	7.1	10.6	1.0	12.0	
3-State Output Enable Time	t_{pZL} t_{pZH}	RL = 1kΩ	3.3 ± 0.3	15	—	8.2	12.8	1.0	15.0	
				50	—	10.7	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.9	9.0	1.0	10.5	
				50	—	7.4	11.0	1.0	12.5	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	RL = 1kΩ	3.3 ± 0.3	50	—	11.0	15.0	1.0	17.0	
			5.0 ± 0.5	50	—	7.1	10.1	1.0	11.5	
Maximum Clock Frequency	f _{MAX}		3.3 ± 0.3	15	80	125	—	65	—	MHz
				50	50	75	—	45	—	
			5.0 ± 0.5	15	130	180	—	110	—	
				50	85	115	—	75	—	
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	1.5	ns
			5.0 ± 0.5	50	—	—	1.0	—	1.0	
Input Capacitance	C _{IN}				—	4	10	—	10	pF
Output Capacitance	C _{OUT}				—	6	—	—	—	
Power Dissipation Capacitance	C _{PD}	(Note 2)			—	28	—	—	—	

Note (1) Parameter guaranteed by design. $t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$

Note (2) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per F/F)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation :

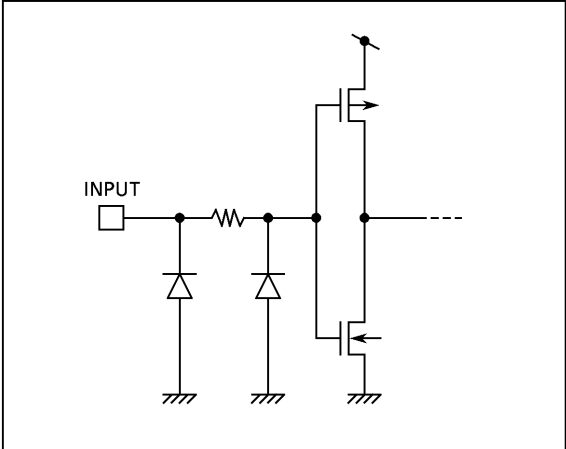
$$C_{PD} \text{ (total)} = 20 + 8 \cdot n$$

NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			UNIT
			V _{CC} (V)	TYP.	MAX.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.8 (0.9)	1.0 (1.2)	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.8 (-0.9)	-1.0 (-1.2)	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	—	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	—	1.5	V

(Note) The value in () only applies to JEDEC SOP (FW) devices.

INPUT EQUIVALENT CIRCUIT



TSSOP 20PIN OUTLINE DRAWING (TSSOP20-P-0044-0.65)

Unit in mm

