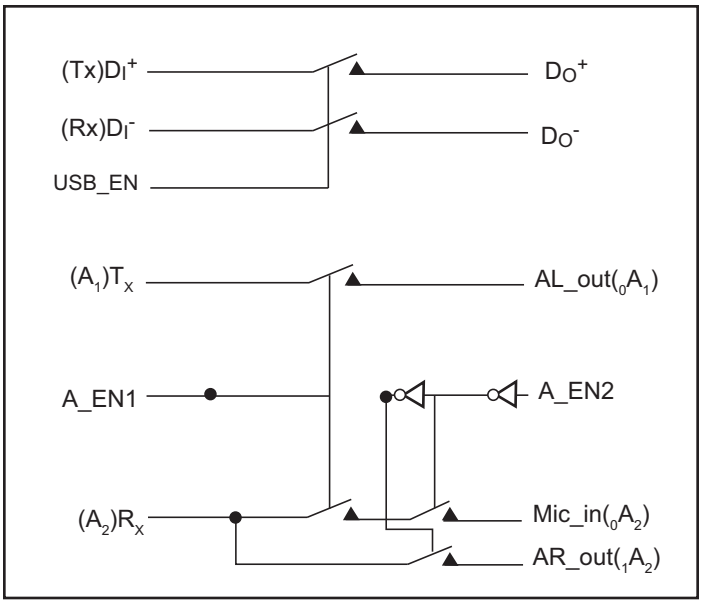
3.3V, Signal Switch Solution for USB 2.0 High Speed (480Mbs) Signals and Audio Signals

Features

- Icc = 1µA
- Ron = 50-ohm @ 3.0V for audio channels
- Off-Isolation = -88dB @ 1 MHz for audio channels
- CrossTalk = -90dB @ 1 MHz
- Ron = 5-ohm @ 2.7V for USB channels
- Con = 5pF for USB channels
- Off-Isolation = -40dB @ 480 mbps for USB channels
- CrossTalk = -38dB @ 480 mbps for USB channels
- Packaging (Pb-free & Green available):
  = 16-pin TQFN (ZN)

Block Diagram



EMU Switch Truth Table

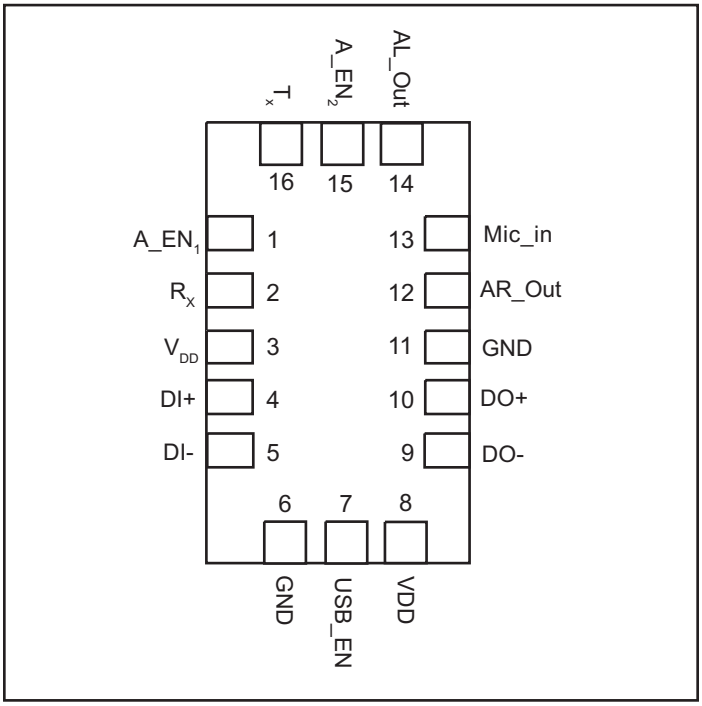
USB_EN	A_EN1	A_EN2	Result
0	0	0	$D_I \pm = T_X = R_X$= Hi-Z
0	0	1	$D_I \pm = T_X$ = Hi-Z, R_X= AR_Out
0	1	0	$D_I \pm$ = Hi-Z, T_X= AL_Out, Rx=Mic_in (Car Kit)
0	1	1	$D_I \pm$ = Hi-Z, T_X= AL_Out, Rx=AR_Out (Stereo Audio)
1	0	0	$D_I \pm = D_O \pm$, $T_X = R_X$= Hi-Z (USB data transfer)
1	0	1	Not Allowed
1	1	0	Not Allowed
1	1	1	Not Allowed

Description

The Enhanced Mini USB port is an inovation that will change the way external plugs are used together with cell phones. This port provides users a single interface to connect audio hands-free kits, audio stereo headsets, battery charger, or USB data cables.

Pericom has develped a unique, single IC, that enables the cell phone designer to provide such features. Pericom's PI3USBA03 offers two channels for high speed USB 2.0 signals (480Mbps), and the other channels are used to pass the stereo and mono audio signals through. Each input/output has high integrated ESD, up to 12kV HBM protection, per JESD22 specification. This single chip solution integrates three ICs into a single easy to use solution. PI3USBA03 also offers PCB board savings with a total package size of 1.3mm x 2.8mm.

Pin Description



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage (V_{DD})	–0.5V to 4.6V
Switch Voltage to Ground Potential	–0.5V to V_{DD} +0.5V
DC Input Voltage	–0.5V to +5.5V
DC Output Current	120mA
Power Dissipation @ 85°C	180mW
Input Diode Current	-50mA
Switch Current	200mA
Peak Switch Current (pulsed at 1ms duration, <10% Duty Cycle)	400mA
Maximum Junction Temperature (T_j)	+150°C
Lead Temperature (T_L) Soldering, 10 seconds	+260°C
Power Dissipation	0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Supply Voltage (V_{DD})	1.65V to 4.2V
Control Input Voltage (V_{IN})(1)	0V to V_{DD}
Switch Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature	–40°C to +85°C

Notes:

1. Unused Inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

USB Signal Path Characteristics ONLY (not related to pins: 1, 2, 12, 13,14, 15, 16)
(T_A = –40°C to +85°C, V_{DD} = 3.3V ±10%)

Paramenter	Description	Test Conditions	Min.	Typ.(4)	Max.	Units
$V_{IH\ (USB\_EN)}$	Input HIGH Voltage for USB_EN	V_{DD} = 2.7V to 3.6V	1.3			V
$V_{IL\ (USB\_EN)}$	Input LOW Voltage for USB_EN	V_{DD} = 2.7V to 3.6V			0.6	
I_{USB_EN}	Control Input Leakage Current	V_{DD} = 2.7V to 3.6V			1.0	µA
V_H	Input Hysteresis	V_{DD} = 2.7V to 3.6V		0.15		
R_{ON}	Switch On-Resistance(1)	VIN = -0.4V, 1.0V ION = -40mA			5	Ω
ΔR_{ON}	On-Resistance match from center ports to any other port(2)			0.12	0.15	
$R_{FLAT(ON)}$	On-Resistance Flatness(3)			1.4		
I_{CC}	Quiescent Supply current	V_{DD} = 3.6V		0.5	1.0	µA

Notes:
1. On-Resistance is determined by the voltage drop between input and output signal pins at the indicated current through the switch.
2. ΔR_{ON} On-Resistance match from center ports to any other port measured at identical V_{DD}, temperature, and voltage.
3. Flatness is defined as the diffeence between the maximum and minimum value of On-Resistance over the specified range of conditions.
4. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.

AC Electrical Characteristics
USB Channels (Not Related To Pins: 1, 2, 12, 13, 14, 15, 16)

(All typical values are at 25°C unless otherwise specified)

Paramenter	Description	Test Conditions	Min.	Typ.	Max.	Units
QIRR	OFF Isolation	V_{DD} = 2.7V to 3.6V @ 480mbps		-40		dB
X_{talk}	Crosstalk	V_{DD} = 2.7V to 3.6V @ 480 mbps		-38		
BW	-3db Bandwidth	V_{DD} = 2.7V to 3.6V		1.1		GHz
	-0.5dB BW	V_{DD} = 2.7V to 3.6V		360		MHz

Notes:
1. R_L = 50-ohm, C_L = 35pF, Input = 1.5V

Capacitance

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	USB_EN Pin Input Capacitance	V_{DD} = 2.7V	2.5	pF
C_{OFF}	D+/D- Port OFF Capacitance		2.0	
C_{ON}	D+/D- Port ON Capacitance		5.0	

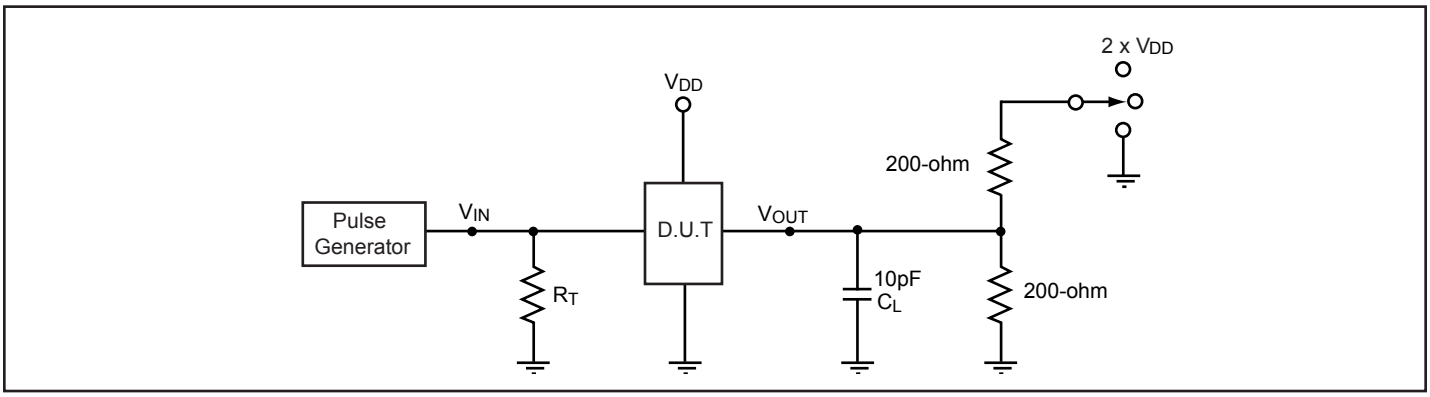
Switching Characteristics USB Channels (Not Related To Pins: 1, 2, 12, 13, 14, 15, 16)

Parameters	Description	Test (2) Conditions	Min.	Typ.(3)	Max.	Units
t_{PD}	Propagation Delay(1)			0.25		ns
t_{PZH}, t_{PZL}	Line Enable Time - USB_EN to D_N		0.5		15.0	
t_{PHZ}, t_{PLZ}	Line Disable Time - USB_EN to D_N		0.5		9.0	

Notes:

1. The switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 10pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.
2. For max. or min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
3. Typical values are at V_{DD} = 3.3V, T_A = 25C ambient and maximum loading.

Test Circuit for Electrical Characteristics



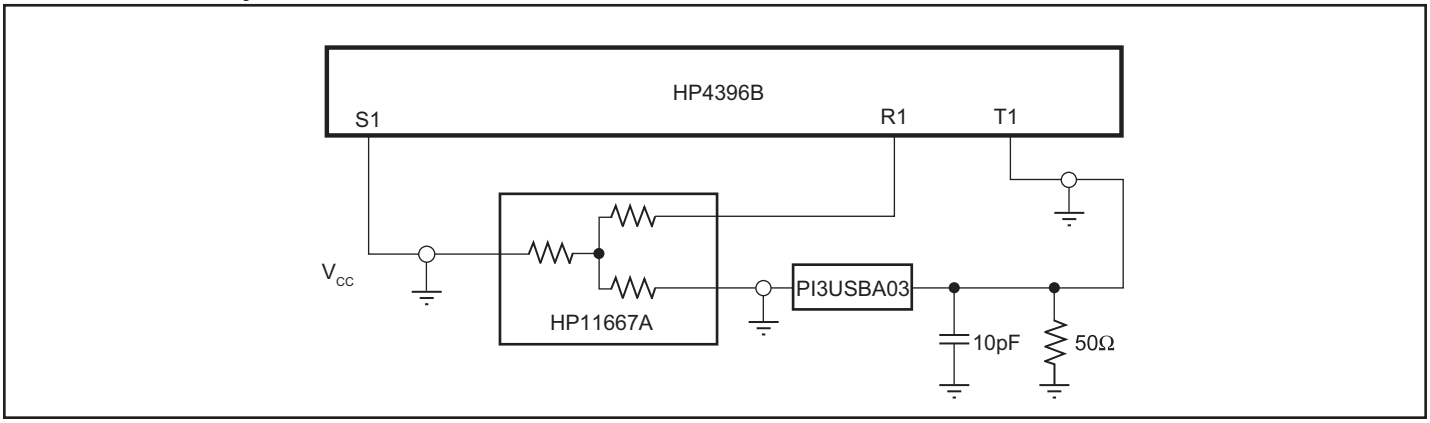
Notes:

- C_L = Load capacitance: includes jig and probe capacitance.
- R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input impulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
- The outputs are measured one at a time with on transition per measurement.

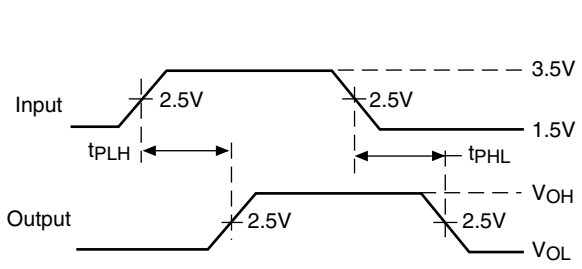
Switch Positions

Test	Switch
t_{PLZ}, t_{PZL} (output on O-side)	2 xV_{DD}
t_{PHZ}, t_{PZH} (output on O-side)	GND
Prop Delay	Open

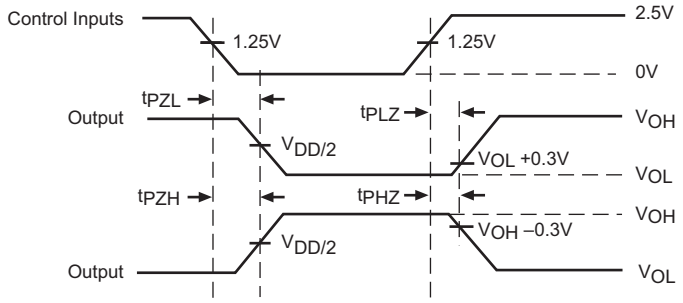
Test Circuit for Dynamic Electrical Characteristics



Switching Waveforms



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times

Audio Signal Path (not related to pins 4, 5, 7, 9, 10)

DC Electrical Characteristics +3V Supply

(V_{DD}= 2.7V to 3.3V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at 3V and +25°C.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Analog Switch						
Analog Signal Range	V_{1AX}, V_{0AX}, V_{AX}		0		V_{DD}	V
On-Resistance	R_{ON}				65	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{DD} = 2.7V, V_{IN} = 1.5V I_{ON} = 10mA		2		
$_0A_X$ On-Resistance Flatness	$R_{ONF(_0A_X)}$	V_{DD} = 2.7V, V_{IN} = 0V - V_{DD}		12		
On Leakage Current	I_{ON}	V_{DD} = MAX, V_{IN} = GND or V_{DD}	-160		160	nA
Digital I/O (A_EN1 and A_EN2)						
Input Logic High	V_{IH}		1.3			V
Input Logic Low	V_{IL}				0.6	
Input Hysteresis	V_H	V_{DD} = 3.3V		200		mV
Input Leakage Current	I_{A_EN}	V_{A_EN} = 0 or V_{DD}	-1		1	µA
Power Supply						
Power-Supply Range	V_{DD}		1.65		4.6	V

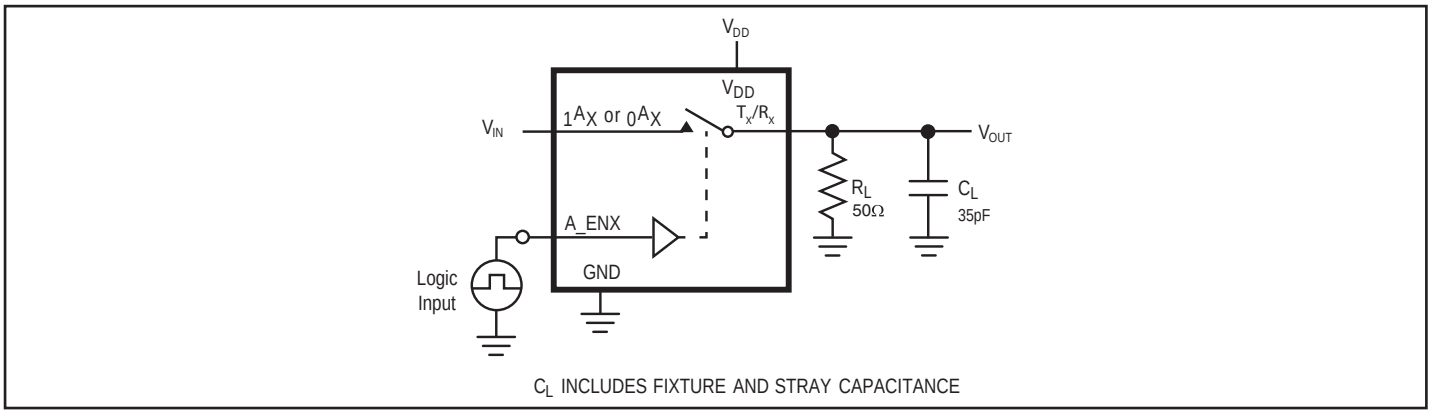
Switch and AC Characteristics (NOT related to pins 4, 5, 7, 9, 10)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Turn-On Time	t_{ON}	*See Test Circuit Figure 1 & 2.*		25	60	ns
Turn-Off Time	t_{OFF}	*See Test Circuit Figure 1 & 2.*		7	20	
Charge Injection	Q	*See Test Circuit Figure 4.*		2.7		pC
Off-Isolation	O_{IRR}	C_L = 5pF, R_L = 50Ω, f = 1 MHz, *See Test Circuit Figure 5.*		-88		dB
Crosstalk	X_{TALK}	C_L = 5pF, R_L = 50Ω, f = 1 MHz, *See Test Circuit Figure 6.*		-90		
3dB Bandwidth	f_{3dB}	*See Test Circuit Figure 9.*		1200		MHz

Capacitance, Audio Switch

Parameter	Symbol	Test Conditions	Min.	Typ.	Units
Off Capacitance	$C_{(OFF)}$	f = 1 MHz, *See Test Circuit Figure 7.*		1.5	pF
On Capacitance	$C_{(ON)}$	f = 1 MHz, *See Test Circuit Figure 8.*		5.0	

Test Circuits and Timing Diagrams (not related to pins 4, 5, 7, 9, 10)



Note:
1. Unused input (NC or NO) must be grounded.

Figure 1. AC Test Circuit

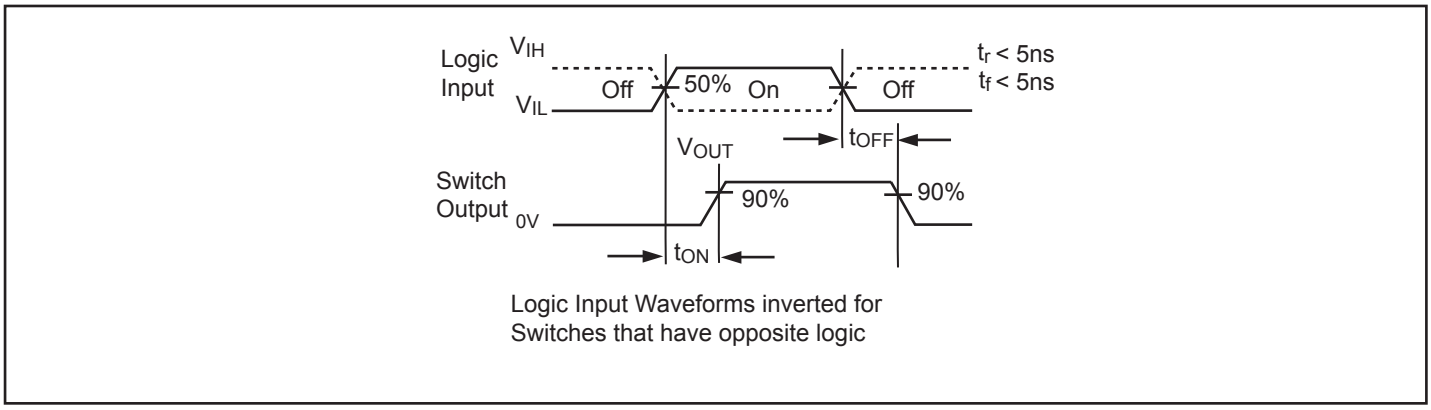


Figure 2. AC Waveforms

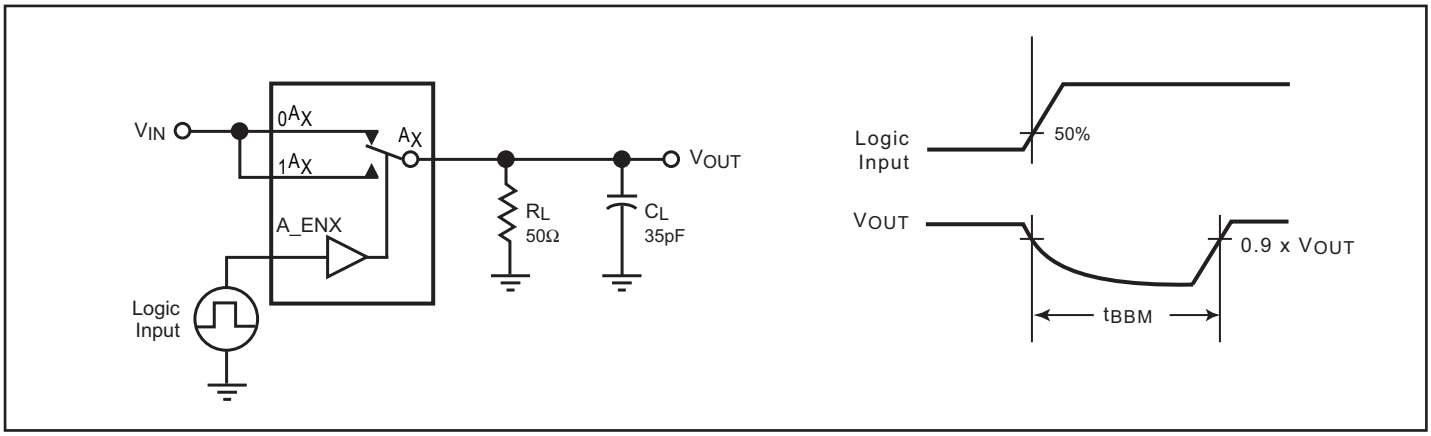


Figure 3. Break Before Make Interval Timing

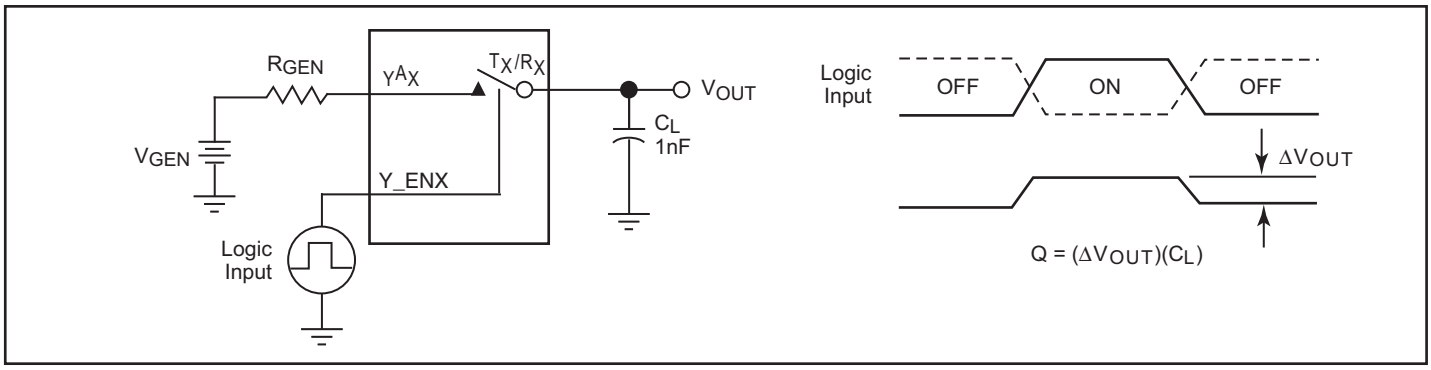


Figure 4. Charge Injection Test

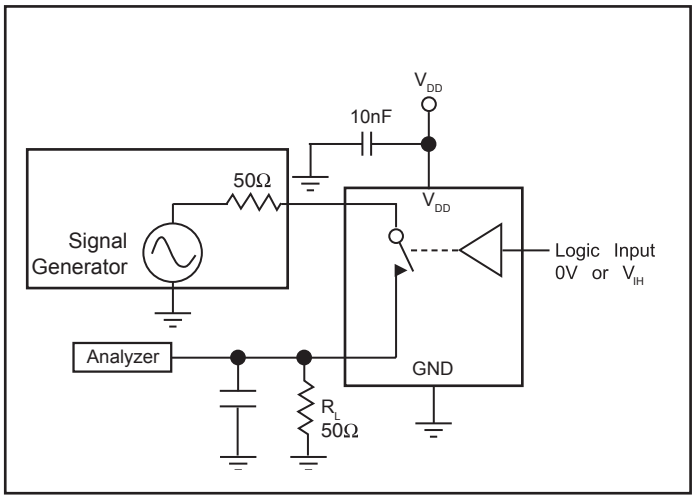


Figure 5. Off Isolation

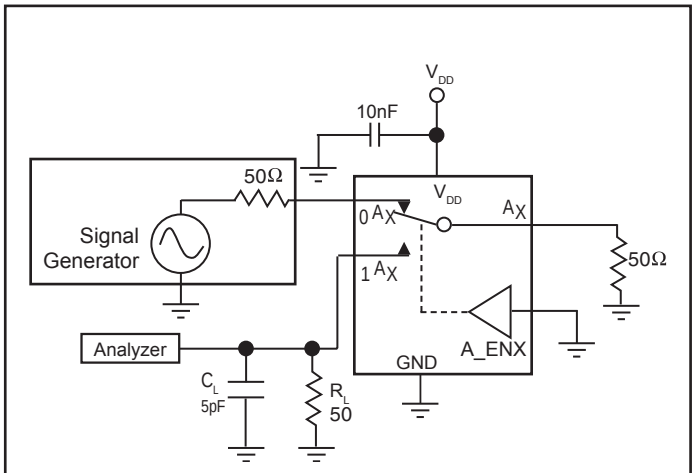


Figure 6. Crosstalk

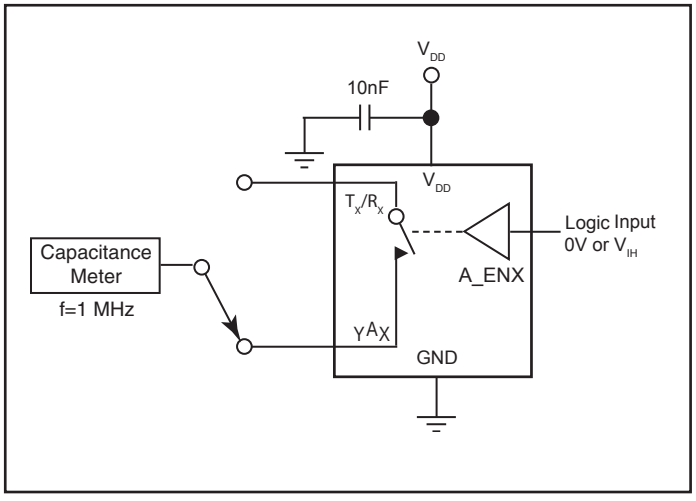


Figure 7. Channel Off Capacitance

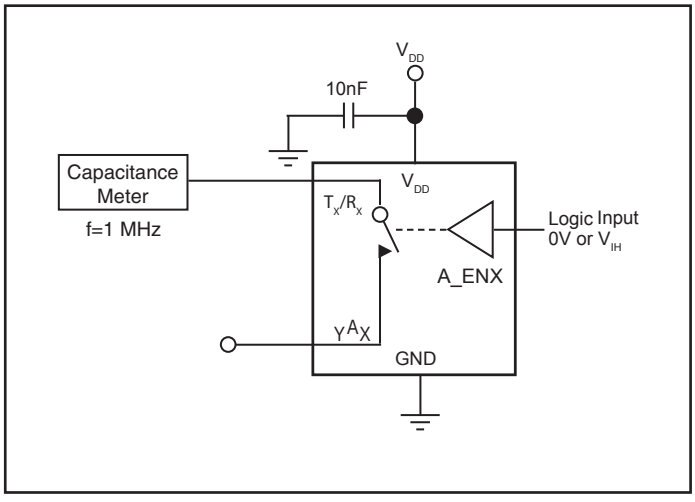


Figure 8. Channel On Capacitance

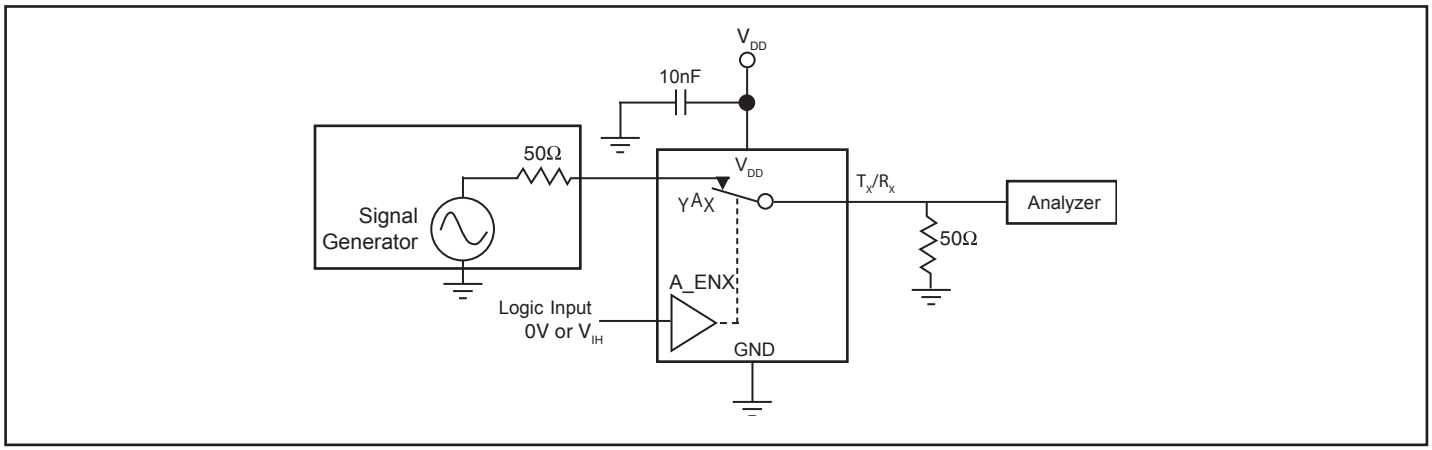


Figure 9. Bandwidth

Application Information

Introduction

USB compliance test was done on the PI3USBA03 USB path. There are two main parts for the compliance test: TDR and Tektronics Signal Quality Test for both USB 2.0 High Speed and USB 2.0 Full Speed Specification. Please refer to section 1 and 2.

Equipment

HP power supply & DMM

TDS8000 Oscilloscope with TEK P6209 Probes

Copper Board and Special SMA connector.

Conclusion

1. TDR passes the USB 2.0 TDR Specification. The impedance is ranging from 72ohm to 106ohm. Please refer to Section 1.
2. PI3USBA03 passes the USB 2.0 High Speed and Full Speed Tektronics Compliance Test. Please refer to Section 2.

Section 1: TDR Measurement for USB Signal Path

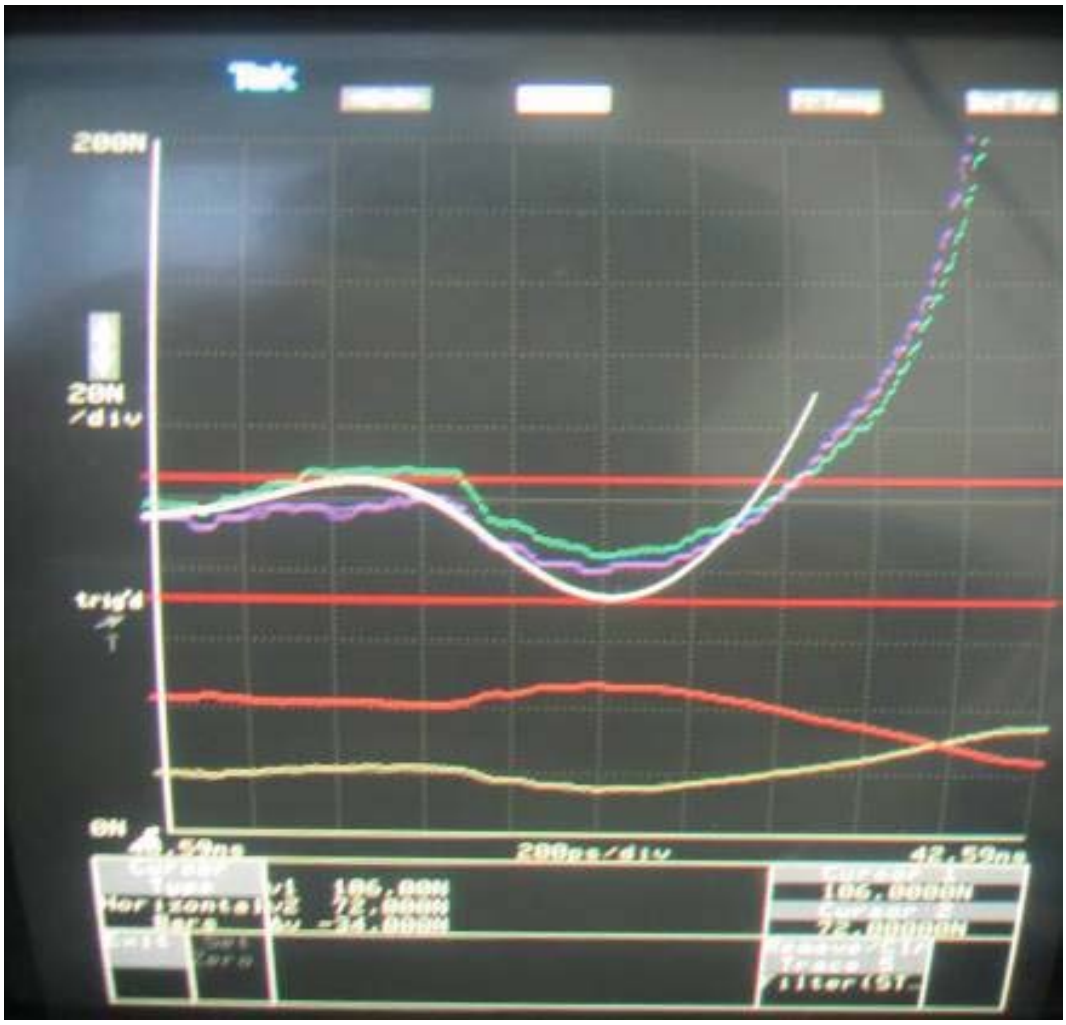


Figure 1: TDRon the USB signal path, V_{DD}=3.3V, 25C

Section 2: Tektronics Compliance Test for USB Port

Part A: USB 2.0 Full Speed Compliance Test Result

Signal Quality Test Results in Tektronics format
Device ID: fsfe_001
Device Description: Full Speed, Far End Device, Down Stream Testing, Tier 6, Dummy Device.
Date: Mon Feb 26 16:41:59 CST 2007
Overall Result: Pass*

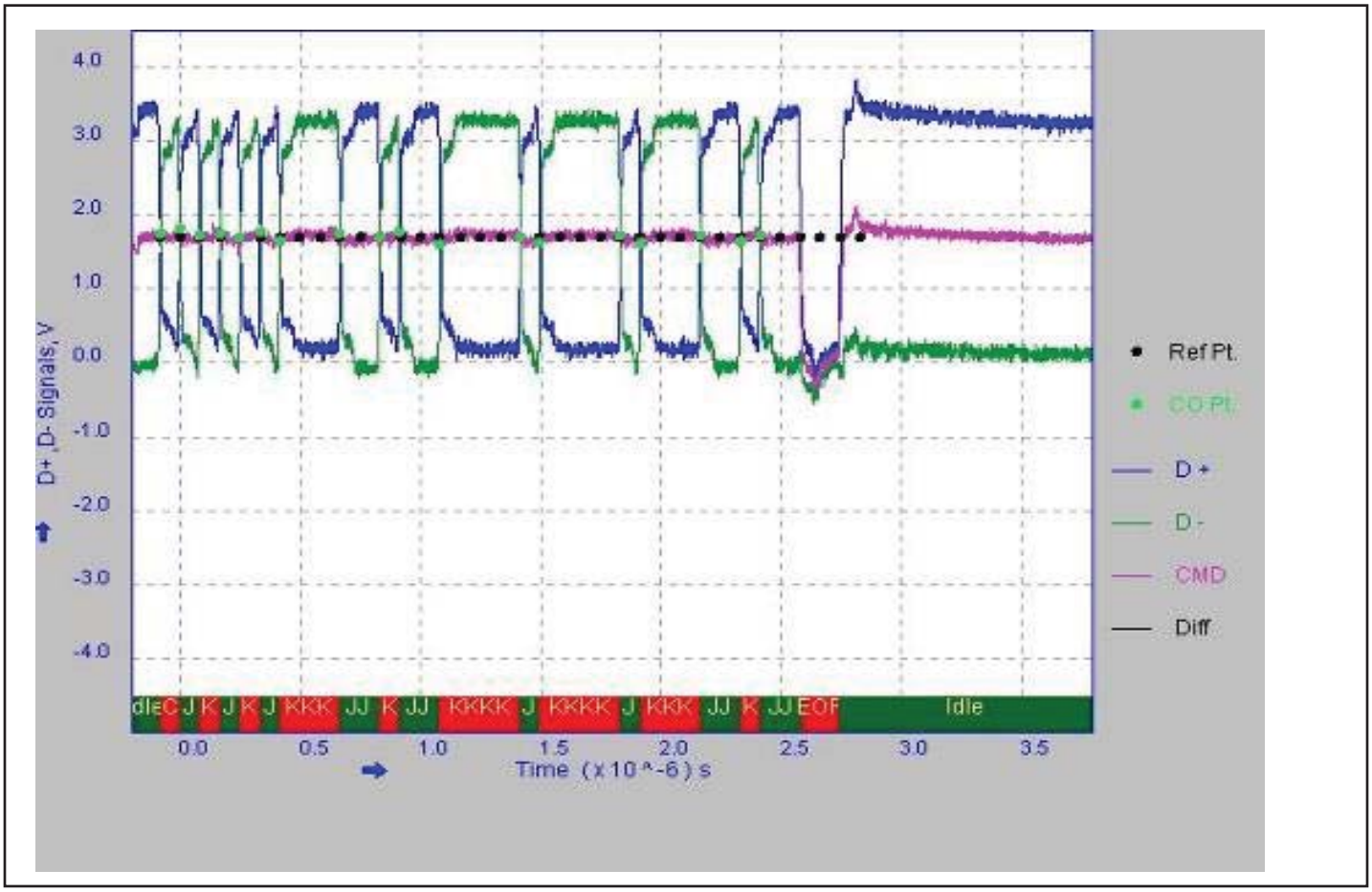


Figure 2. Waveform Plot

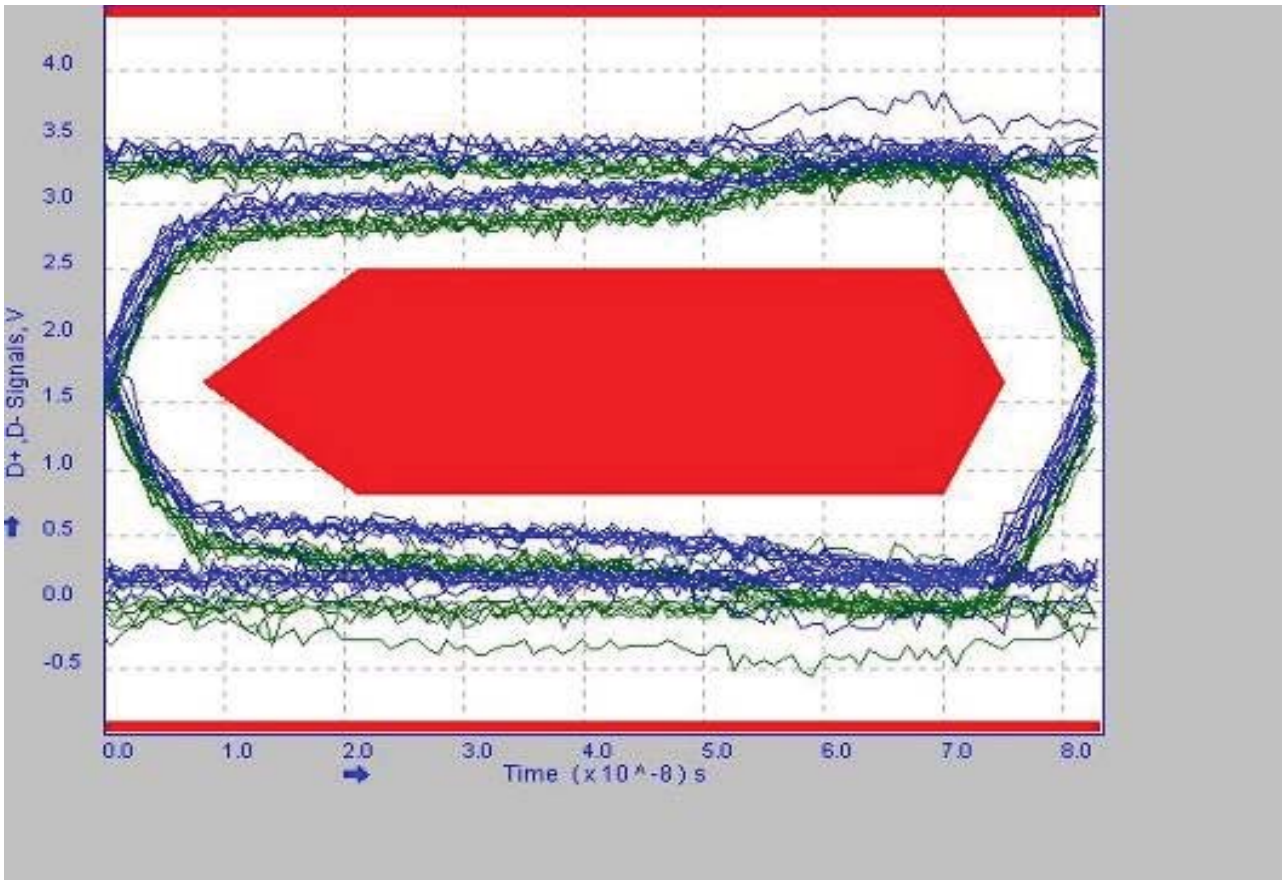


Figure 3. Eye Diagram

Part B: USB 2.0 High Speed Compliance Test Result

Signal Quality Test Results in Tektronics format

Device ID: fsfe_001

Device Description: High Speed, Near End Device, Up Stream Testing, Tier 1, Dummy Device.

Date: Mon Feb 26 16:38:50 CST 2007

Overall Result: Pass*

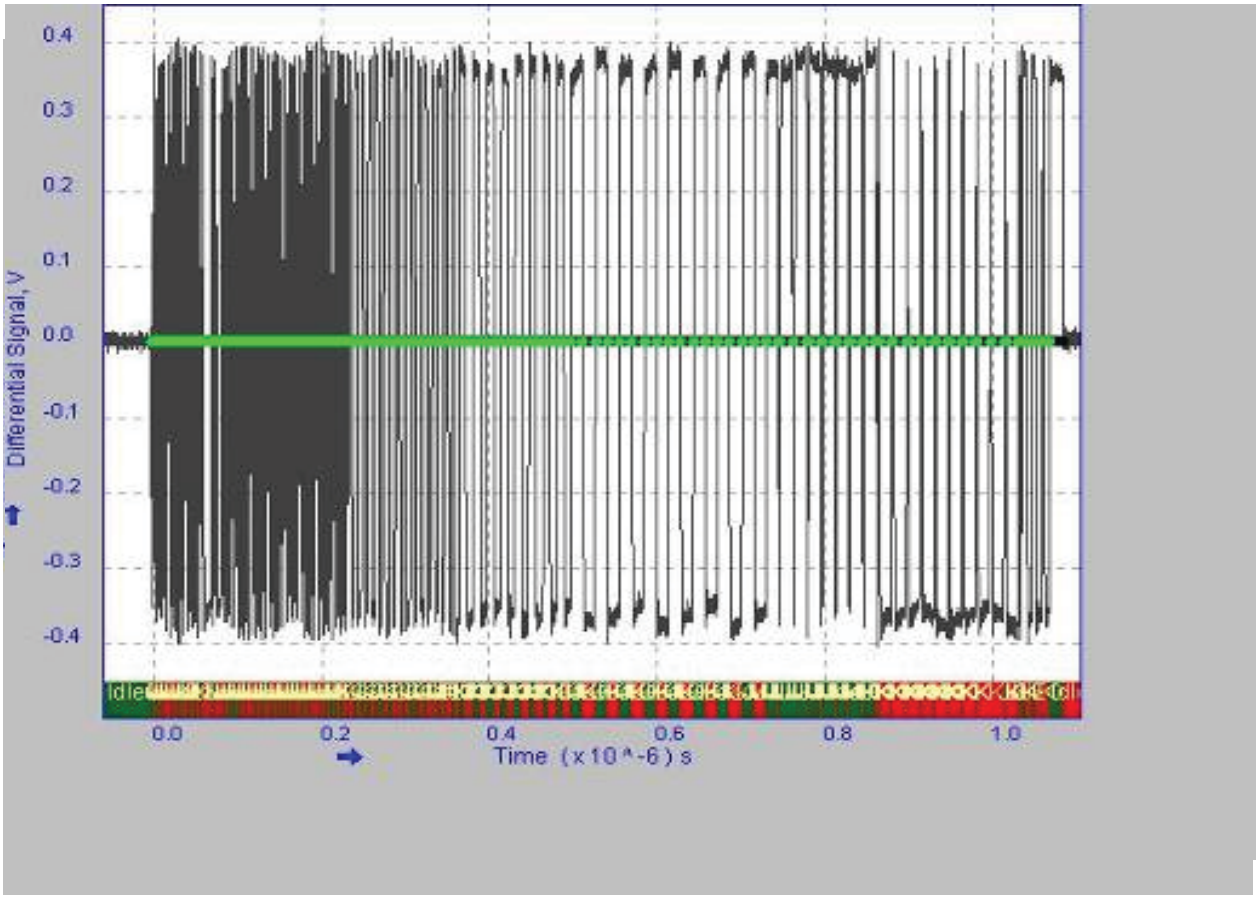


Figure 4. Waveform Plot

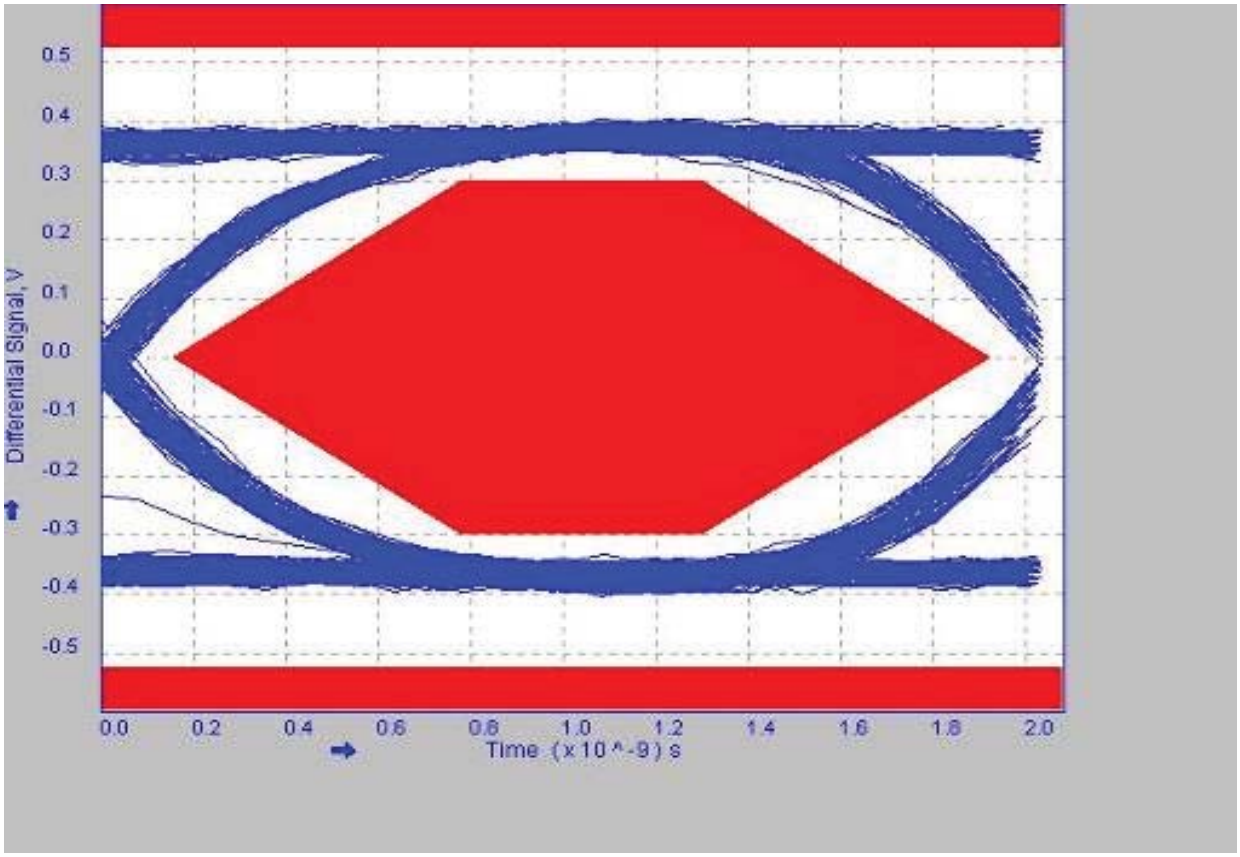


Figure 5. Eye Diagram

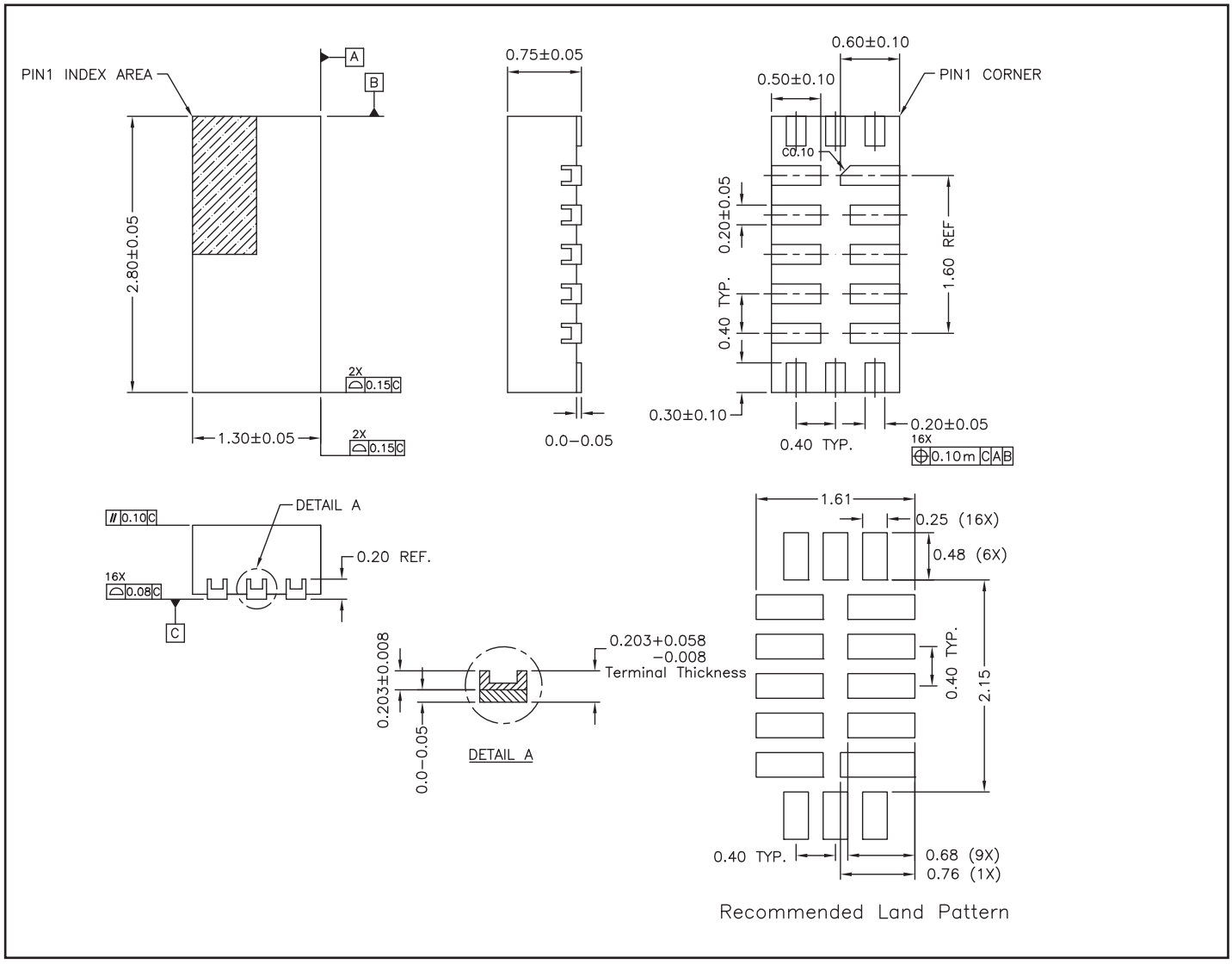
Additional Information :

Consecutive Jitter range : -65.36ps to 71.84ps, RMS Jitter 29.2ps

KJ Paired Jitter range : -81.78ps to 80.23ps, RMS Jitter 32.6ps

JK Paired Jitter range : -88.25ps to 78.97ps, RMS Jitter 30.3ps

Package Mechanical: 16-Contact TQFN (ZN)



Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3USBA03ZNE	ZN	Pb-free & Green, 16-contact TQFN	ME

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel