PI3A223C

Dual SPDT Analog Switch with Negative Signal Support for AC Coupled Signals

Features

- CMOS Technology for Bus and Analog Applications
- Low On-Resistance: 0.6Ω.
- V_{DD} Range: 2.7V to 4.2V
- V_{INPUT} tolerance down to -1.5V
- High Off Isolation: -80dB @ 100kHz
- Integrated ESD protection up to 2kV HBM
- Crosstalk Rejection Reduces Signal Distortion:
  -80dB @ 100kHz
- Input signals can be from -1.5V up to +3.6V without distortion.
- Break-Before-Make Switching
- Extended Industrial Temperature Range: –40°C to 85°C
- Packaging (Pb-free & Green):
  − 10-contact TQFN (ZM10) 1.4×1.8

Applications

- Cell Phones
- PDAs
- MP3 players
- Portable Instrumentation
- Computer Peripherals
- Speaker Headset Switching
- Power Routing
- Relay Replacement
- Audio and Video Signal Routing
- PCMCIA Cards
- Modems

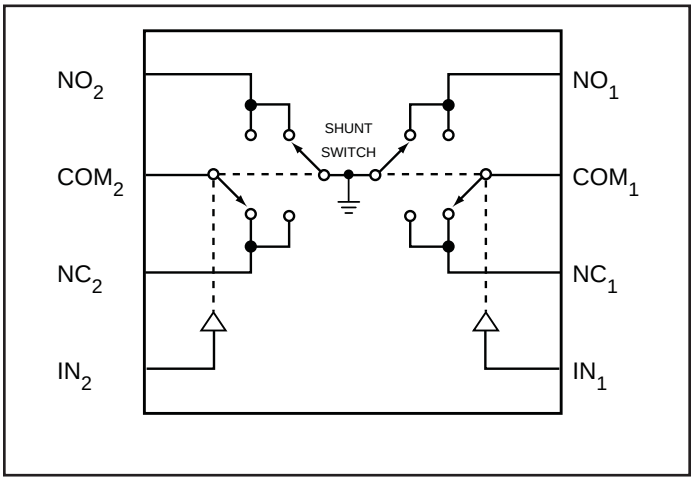
Description

Pericom Semiconductor's PI3A223C is a dual, fast single-pole double throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. The PI3A223C has an On-Resistance of 0.6Ω at +2.8V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

With the use of 3rd party headsets, AC coupling is required to protect against EOS damage caused by DC offsets. Pericom's PI3A223C can support these AC coupled audio signals, since the switch can tolerate signals down to -1.5V without a negative power supply.

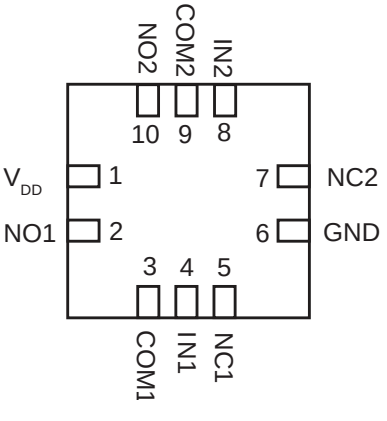
Functional Block Diagram



Pin Description

Pin #	Name	Description
2, 10	NO_X	Data Port (Normally open)
6	GND	Ground
5, 7	NC_X	Data Port (Normally closed)
3, 9	COM_X	Common Output / Data Port
1	V_{DD}	Positive Power Supply
4, 8	IN_X	Logic Control

Pin Configuration (top view)



Logic Function Table

Logic Input (IN_X)	Function
0	NC_X Connected to COM_X
1	NO_X Connected to COM_X

Note: x = 1 or 2

Absolute Maximum Ratings(1)

Supply Voltage V_{DD}	2.7V to 4.2V ±10%
DC Control Switch Voltage (V_{INx})	0V to 5V
DC Input Voltage (V_{INPUT})(2)	–1.5V to VDD
Continuous Current NO_NC_COM_	±300mA
Peak Current NO_NC_COM_ (pulsed at 1ms 50% duty cycle)	±400mA
Peak Current NO_NC_COM_ (pulsed at 1ms 10% duty cycle)	±500mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	250mW

Recommended Operating Conditions(3)

Supply Voltage Operating (V_{DD})	2.7V to 4.2V ± 5%
Control Input Voltage (V_{IN})	0V to 3.3V
Switch Input Voltage (V_{INPUT})	–1.5V to 3.3V
Operating Temperature (T_A)	–40°C to +85°C
Input Rise and Fall Time (t_r,t_f) Control Input V_{DD} = 2.3V - 3.6V	0ns/V to 10ns/V
Thermal Resistance (θ_{JA})	350°C/W
Lead Temperature (soldering 10s)	+300°C
Bump Temperature (soldering notes)	
Infared (15s)	+220°C
Vapor Phase (60ns)	+215°C

Notes:

1. "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.
2. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
3. Control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics Supply

(V_{DD} =2.7V to 3.3V, T_A = –40°C to 85°C, unless otherwise noted. Typical values at +25°C.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Analog Switch						
Analog Signal Range	V_{NO} , V_{NC} , V_{COM}		-1.5		V_{DD}	V
NC On-Resistance	$R_{ON(NC)}$	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NC} = –1.5V to +3.3V		0.5		Ω
NO On-Resistance	$R_{ON(NO)}$	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NO} = –1.5V to +3.3V		0.5		
On-Resistance Match Between Channels	ΔR_{ON}	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NO} or VNC = 1.5V to 3.3V		0.02		
NC On-Resistance Flatness	$R_{ONF(NC)}$	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NC} = –1.5V to +3.3V		0.1		
NO On-Resistance Flatness	$R_{ONF(NO)}$	V_{DD} = 2.7V, I_{COM} = 100mA, V_{NO} = –1.5V to +3.3V		0.1		
NO or NC Off Leakage Current	$I_{OFF (NO)}$ or $I_{OFF (NC)}$	V_{DD} = 3.3V, V_{NO} or V_{NC} = 0.3V	-400		400	nA
COM On Leakage Current	$I_{COM (ON)}$	V_{DD} = 3.3V, V_{NO} or V_{NC} = 0.3V, V_{COM} = 0.3V	-160		160	
Total Harmonic Distortion	THD	Load = 8Ω pulled to GND, V_{DD} = 2.7V, Vinput = 2Vpp, frequency = 20Hz to 20KHz		0.035		%
		Load = 16Ω pulled to GND, V_{DD} = 2.7V, Vinput = 2Vpp, frequency = 20Hz to 20KHz.		0.03		
Digital I/O						
Input Logic High	V_{IH}		1.3			V
Input Logic Low	V_{IL}				0.6	
Input Hysteresis	V_H	V_{DD} = 2.7V		120		mV
IN Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}	-0.5		0.5	µA

Supply Current

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Current	I_{CC}	V_{DD} = 2.8V, V_{IN} = 0V, 1.3V, 2.8V		17	35	µA
		V_{DD} = 3.6V, V_{IN} = 0V, 1.3V, 2.8V, 3.6V		36	50	
		V_{DD} = 4.4V, V_{IN} = 0V, 1.8V, 3.6V, 4.4V		73	90	
		V_{DD} = 4.4V, V_{IN} = 1.3V		2.3	3.0	mA

Switch and AC Characteristics

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Turn-On Time	t_{ON}	V_{DD} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 1 & 2.*			65	ns
Turn-Off Time	t_{OFF}	V_{DD} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 1 & 2.*			65	
Break-Before-Make Delay	t_{BBM}	V_{DD} = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF, *See Test Circuit Figure 3.*			20	
Charge Injection	Q	*See Test Circuit Figure 4.*		35		pC
Off-Isolation	O_{IRR}	C_L = 5pF, R_L = 50Ω, f = 100kHz, V_{COM} = 1 V_{RMS}, *See Test Circuit Figure 5.*		-80		dB
Crosstalk	X_{TALK}	C_L = 5pF, R_L = 50Ω, f = 100kHz, V_{COM} = 1 V_{RMS}, *See Test Circuit Figure 6.*		-80		
3dB Bandwidth	f_{3dB}	*See Test Circuit Figure 9.*		100		MHz

DC Electrical Characteristics Supply

(V_{DD} =3.3V to 4.4V, T_A = –40°C to 85°C, unless otherwise noted. Typical values are at +25°C.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Analog Switch						
Analog Signal Range	V_{NO} , V_{NC} , V_{COM}		-1.5		3.3	V
NC On-Resistance	$R_{ON(NC)}$	V_{DD} = 4.2V, I_{COM} = 100mA, V_{NC} = –1.5V to +3.3V		0.4		Ω
NO On-Resistance	$R_{ON(NO)}$	V_{DD} = 4.2V, I_{COM} = 100mA, V_{NO} = –1.5V to +3.3V		0.4		
On-Resistance Match Between Channels	ΔR_{ON}	V_{DD} = 4.2V, I_{COM} = 100mA, V_{NO} or VNC = 3.3V		0.02		
NC On-Resistance Flatness	$R_{ONF(NC)}$	V_{DD} = 4.2V, I_{COM} = 100mA, V_{NC} = –1.5V to +3.3V		0.1		
NO On-Resistance Flatness	$R_{ONF(NO)}$	V_{DD} = 4.2V, I_{COM} = 100mA, V_{NO} = –1.5V to +3.3V		0.1		
NO or NC Off Leakage Current	$I_{OFF (NO)}$ or $I_{OFF (NC)}$	V_{DD} = 4.2V, V_{NO} or V_{NC} = 0.3V	-400		400	nA
COM On Leakage Current	$I_{COM (ON)}$	V_{DD} = 4.2V, V_{NO} or V_{NC} = 0.3V, V_{COM} = 0.3V	-160		160	
Total Harmonic Distortion	THD	Load = 8Ω pulled to GND, V_{DD} = 3.3V, Vinput = 2Vpp, Freq = 20Hz to 20KHz		0.03		%
		Load = 16Ω pulled to GND, V_{DD} = 3.3V, Vinput = 2Vpp, frequency = 20Hz to 20KHz.		0.025		
Digital I/O						
Input Logic High	V_{IH}		1.3			V
Input Logic Low	V_{IL}				0.6	
Input Hysteresis	V_H	V_{DD} = 4.2V		170		mV
IN Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}	-0.5		0.5	µA

Capacitance

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NC Off Capacitance	$C_{NC (OFF)}$	f = 1MHz, *See Test Circuit Figure 7.*		20		pF
NO Off Capacitance	$C_{NO (OFF)}$	f = 1MHz, *See Test Circuit Figure 7.*		20		
NC On Capacitance	$C_{NC (ON)}$	f = 1MHz, *See Test Circuit Figure 8.*		60		
NO On Capacitance	$C_{NO (ON)}$	f = 1MHz, *See Test Circuit Figure 8.*		60		

Test Circuits and Timing Diagrams

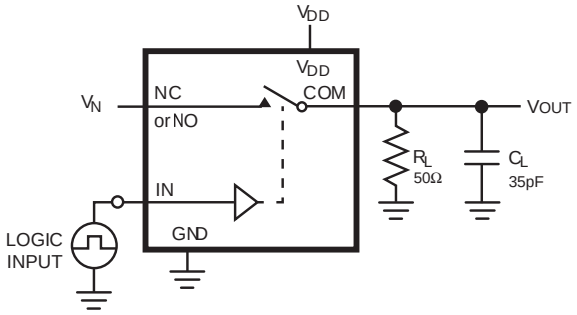


Figure 1. AC Test Circuit

Notes:
1. Unused input (NC or NO) must be grounded.

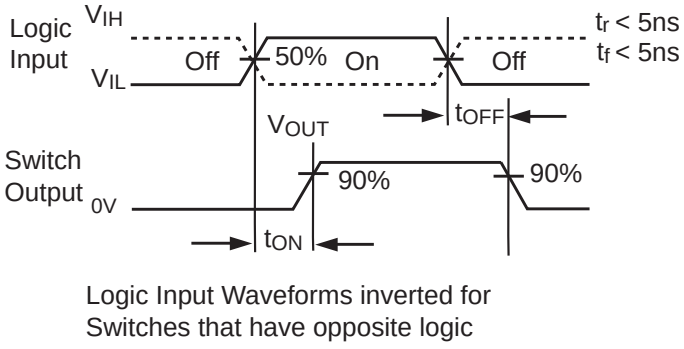


Figure 2. AC Waveforms

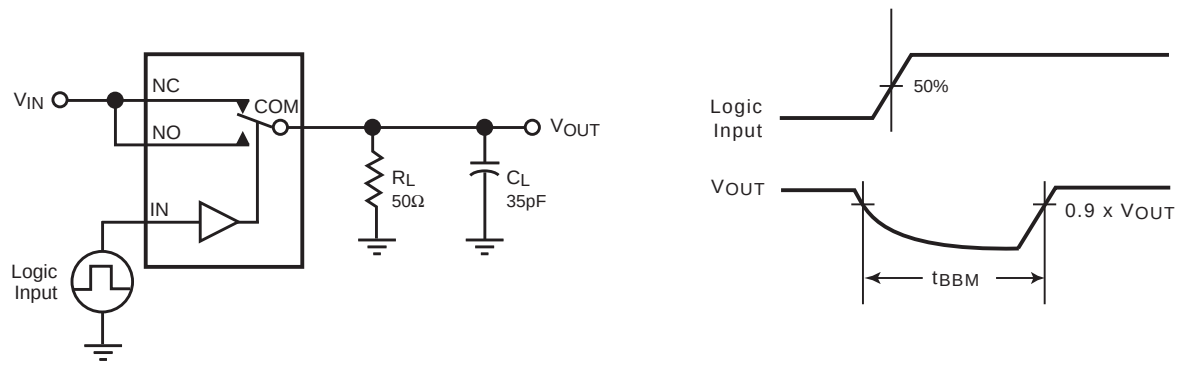


Figure 3. Break Before Make Interval Timing

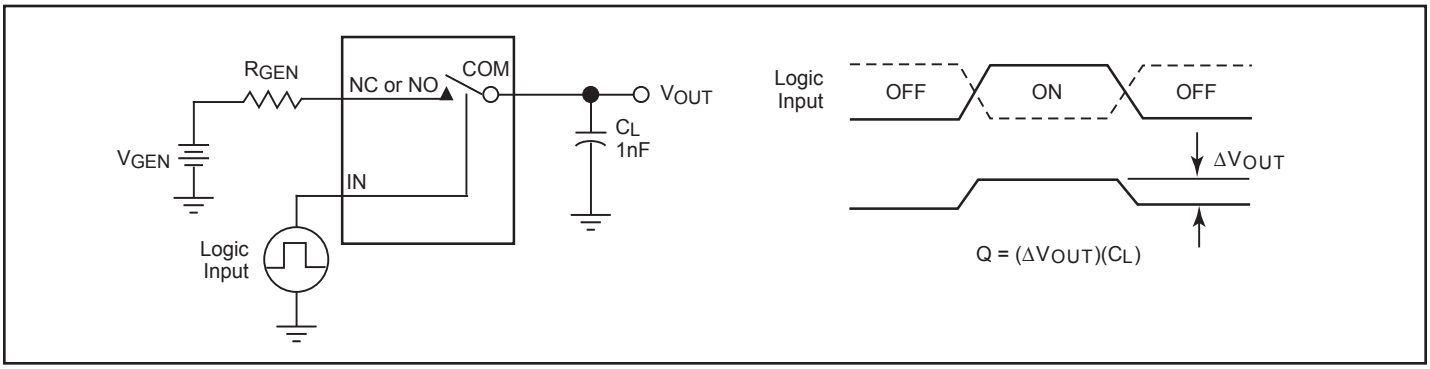


Figure 4. Charge Injection Test

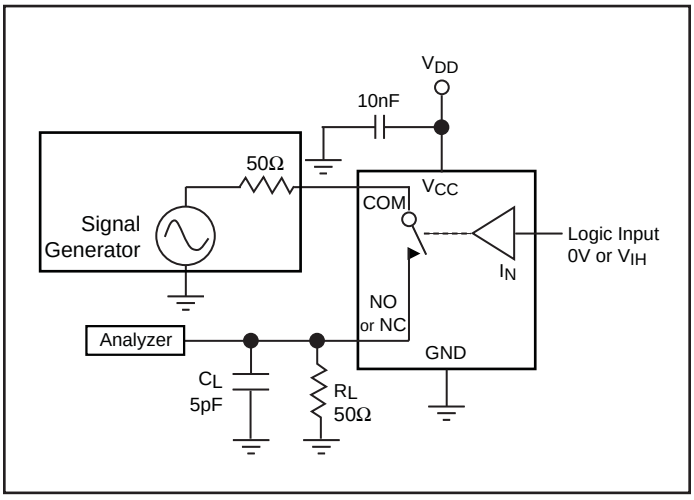


Figure 5. Off Isolation

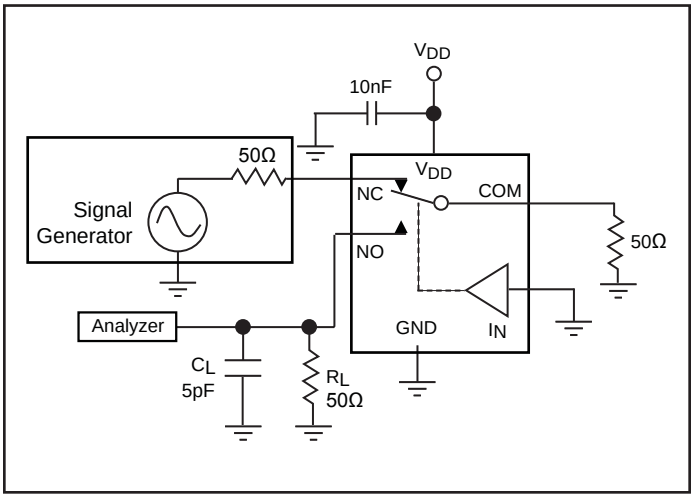


Figure 6. Crosstalk

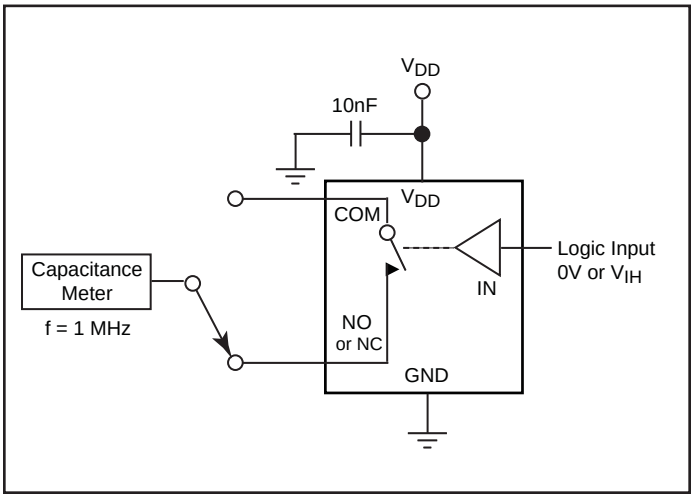


Figure 7. Channel Off Capacitance

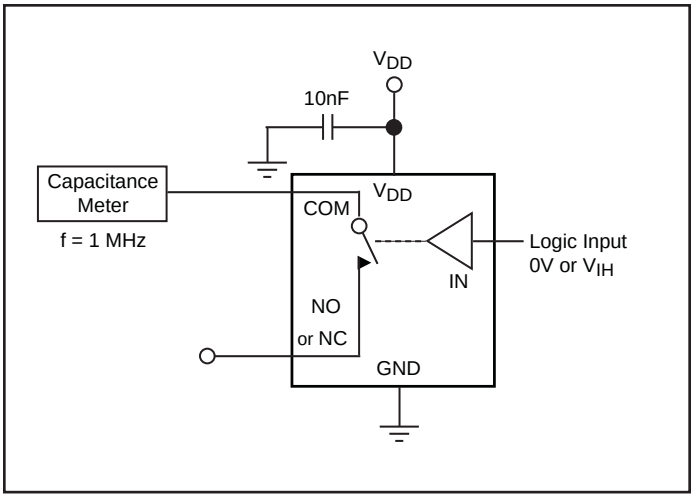


Figure 8. Channel On Capacitance

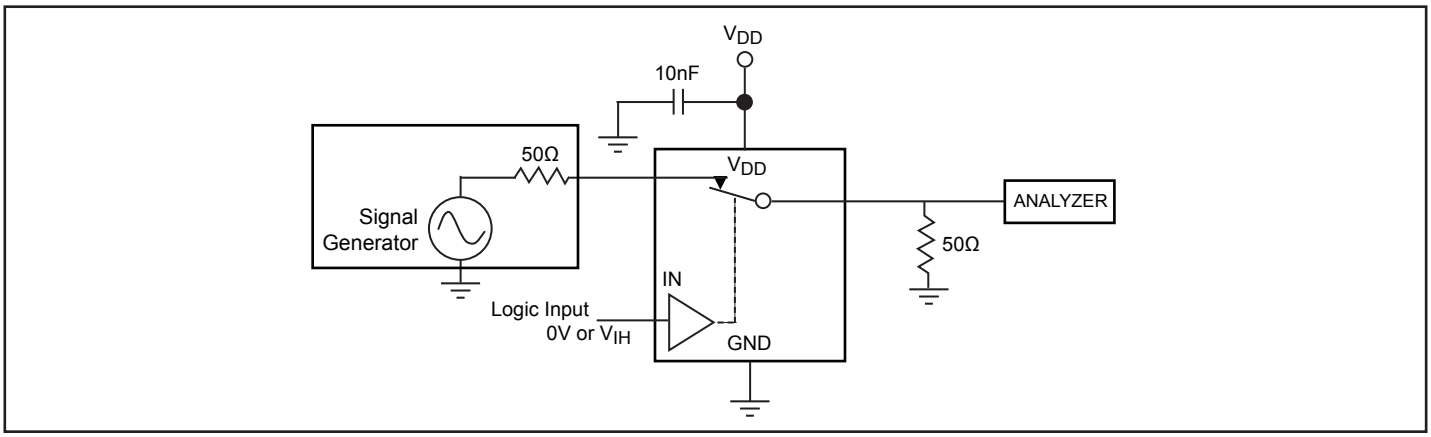
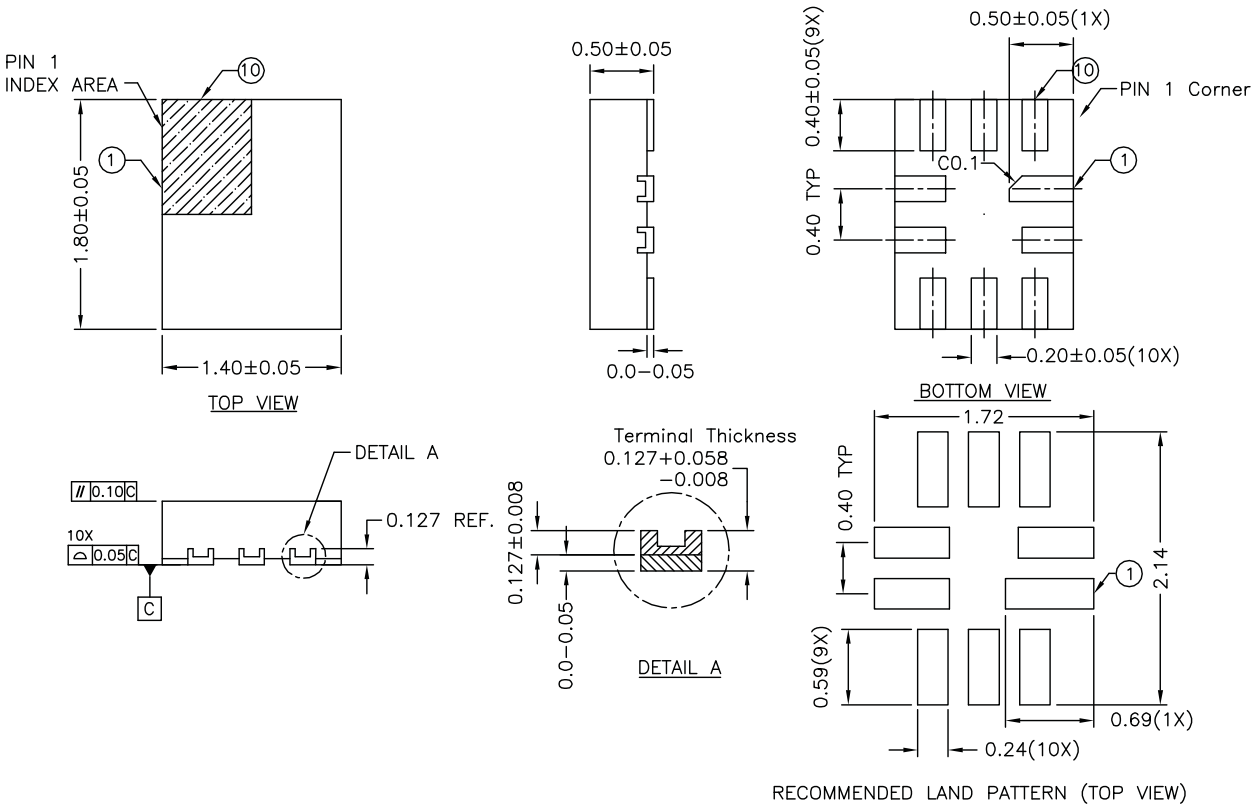


Figure 9. Bandwidth

Packaging Mechanical: 10-pin UQFN (ZM10)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−236/MO−248
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

PERICOM Semiconductor Corporation — DATE: 01/29/09

DESCRIPTION: 10-contact, Ultra-thin Quad Flat No-Lead (UQFN)

PACKAGE CODE: ZM10

DOCUMENT CONTROL #: PD-2066 — REVISION: A

09-0072

Ordering Information

Ordering Code	Packaging Code	Package Type	Top Mark
PI3A223CZME	ZM	1.4 X 1.8, Pb-Free & Green, 10-contact TQFN	FB

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free & Green
- X suffix = Tape/Reel