3.0V, SOTiny™ Single-Supply 0.4Ω SPST (NO) CMOS Analog Switch

Features

- Low On-Resistance: 0.4Ω Max (+2.7V Supply)
- 0.1Ω Max. On-Resistance Flatness at +25°C
- Fast Switching: 10ns Max.
- +1.5 V to +3.6V Single-Supply Operation
- TTL/CMOS-Logic Compatible
- –25dB Off-Isolation at 100KHz
- 1nA Max. Off-Leakage at +25°C
- Packaging (Pb-free & Green available):
  – 6-pin Small Compact SOT-23 (T)
  – 6-contact No Lead TDFN (ZC)

Applications

- Cellular Phones
- Communications Circuits
- Battery-Operated Equipment
- DSL Modems
- Audio and Video Signal Routing
- PCMCIA Cards

Pin Description

Pin Number	Name	Description
1	COM	Analog Switch, Common
2	NO	Analog Switch, Normally Open
3	GND	Ground
4	$\overline{IN}$	Digital Control Input
5	IN	Digital Control Input
6	V_{CC}	Positive Supply Voltage

Note:
1. NO and COM pins are identical and interchangeable. Any pin may be considered as an input or an output; signals pass.

Description

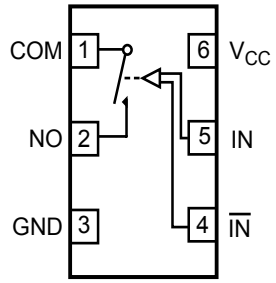
PI3A4628 is a single-pole/single-throw (SPST) normally open (NO) analog switch that operates from a single +1.5V to +3.6V supply. The device has two control inputs.

The switch has 0.4Ω Max On-Resistance (R_{ON}), with 0.1Ω Max R_{ON} flatness over the analog signal range when powered from a +3.0V supply. Leakage currents are less than 2nA and fast switching times are less than 10ns.

To minimize PC board area use, the device is available in the ultra compact TDFN and the small compact SOT-23 packages.

Block Diagram/Pin Configuration

Top View



Switches shown for Logic “0” input

Truth Table

$\overline{IN}$	IN	Switch State
1	0	OFF
1	1	OFF
0	0	ON
0	1	ON

Absolute Maximum Ratings

Voltages Referenced to GND
V_{CC} ..... –0.5V to +3.6V

V_{IN}, V_{COM}, V_{NC}, V_{NO} (1) ..... –0.5V to V_{CC} +0.3V
or 30mA, whichever occurs first

Current (any terminal) ..... ±200mA

Peak Current, COM, NO, NC
(Pulsed at 1ms, 10% duty cycle) ..... ±400mA

Thermal Information

Continuous Power Dissipation

SOT-23 (derate 7.1mW/ºC above +70ºC) 0.5W

Storage Temperature ..... –65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Note:

1. Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

***Caution**: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.*

Electrical Specifications - Single +3.3V Supply

(V_{CC} = +3.3V ± 10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Test Conditions	Package	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch								
Analog Signal Range (3)	V_{ANALOG}			Full	0		V_{CC}	V
On Resistance	R_{ON}	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = +1.5V		25			0.4	Ω
			SOT23	Full			0.5	
			TDFN				0.6	
On-Resistance Match Between Channels(4)	ΔR_{ON}			25			0.05	
				Full			0.06	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$	V_{CC} = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0.8V, 2.0V		25			0.1	
				Full			0.1	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_{CC} = 3.3V, V_{COM} = 0V V_{NO} or V_{NC} = +2.0V		25	–1		1	nA
				Full	-20		10	
COM On Leakage Current(6)	$I_{COM(ON)}$	V_{CC} = 3.3V, V_{COM} = +2.0V V_{NO} or V_{NC} = +2.0V		25	–2		2	
				Full	-20		20	

Electrical Specifications - Single +3.3V Supply (continued)

(V_{CC} = +3.3V ±10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Test Conditions	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel				0.5	
Input Current with Voltage High	I_{INH}	V_{IN} = 1.4V, all others = 0.5V		–1		1	µA
Input Current with Voltage Low	I_{INL}	V_{IN} = 0.5V, all others = 1.4V		–1		1	
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 3.3V, V_{NO} or V_{NC} = 2.0V, Figure 1	25			10	ns
			Full			10	
Turn-Off-Time	t_{OFF}		25			10	
			Full			10	
Charge Injection(3)	Q	C_L =1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	25		50		pC
Off Isolation(7)	O_{IRR}	R_L = 50Ω, f = 100 KHz, Figure 4			-25		dB
NC or NO Capacitance	$C_{NC/NO\ (OFF)}$	f = 1MHz, Figure 5			130		pF
COM Off Capacitance	$C_{COM(OFF)}$				130		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 6			270		
Supply							
Power-Supply Range	V_{CC}		Full	1.5		3.6	V
Positive Supply Current	I_{CC}	V_{CC} = 3.6V, V_{IN} = 0V or V_{CC}				100	nA

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ Max. - R_{ON} Min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NO} or V_{NC})]. See Figure 3.

Electrical Specifications - Single +2.5V Supply

(V_{CC} = +2.5V ±10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

Parameter	Symbol	Test Conditions	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} = 2.5V, I_{COM} = –8mA, V_{NO} or V_{NC} = 1.8V	25			0.4	Ω
			Full			0.4	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{CC} = 2.5V, I_{COM} = –8mA, V_{NO} or V_{NC} = 0.8V, 1.8V	25			0.05	
			Full			0.06	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$		25			0.1	
			Full			0.1	
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} = 2.5V, V_{NO} or V_{NC} = 1.8V, Figure 1	25			10	ns
			Full			15	
Turn-Off-Time	t_{OFF}		25			10	
			Full			10	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 2	25		42		pC
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic Low Level	Full			0.5	
Input High Current	I_{INH}	V_{IN} = 1.4V, all others = 0.5V	Full	–1		1	µA
Input Low Current	I_{INL}	V_{IN} = 0.5V, all others = 1.4V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Electrical Specifications - Single +1.8V Supply

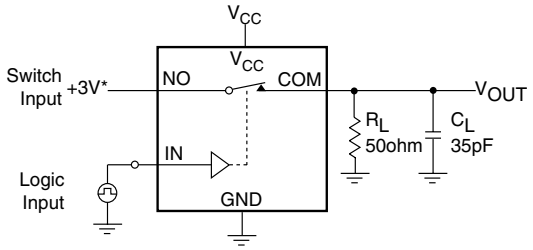
(V_{CC} = +1.8V ±10%, GND = 0V, V_{IH} = 1.4V, V_{IL} = 0.5V)

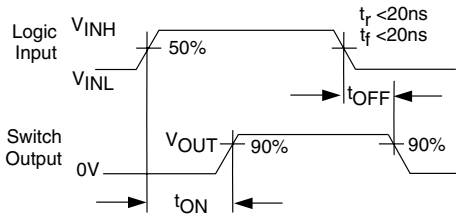
Parameter	Symbol	Test Conditions	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range(3)	V_{ANALOG}			0		V_{CC}	V
On-Resistance	R_{ON}	V_{CC} =1.8V, I_{COM} = –4mA, V_{NO} or V_{NC} = 1.5V	25			0.4	Ω
			Full			0.8	
On-Resistance Match Between Channels(4)	ΔR_{ON}	V_{CC} =1.8V, I_{COM} = –4mA, V_{NO} or V_{NC} = 0.8V, 1.5V	25			0.05	
			Full			0.06	
On-Resistance Flatness(5)	$R_{FLAT(ON)}$		25			0.4	
			Full			0.6	
Dynamic							
Turn-On-Time	t_{ON}	V_{CC} =1.8V, V_{NO} or V_{NC} = 1.5V, Figure 1	25			15	ns
			Full			15	
Turn-Off-Time	t_{OFF}		25			10	
			Full			15	
Charge Injection(3)	Q	C_L -1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	25		29		pC
Logic Input							
Input High Voltage	V_{IH}	Guaranteed Logic High Level	Full	1.4			V
Input Low Voltage	V_{IL}	Guaranteed Logic LowLevel	Full			0.5	
Input High Current	I_{INH}	V_{IN} = 1.4V, all others = 0.5V	Full	–1		1	µA
Input Low Current	I_{INL}	V_{IN} = 0.5V, all others = 1.4V	Full	–1		1	

Notes:

1. The algebraic convention, where most negative value is a minimum and most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. $\Delta R_{ON} = R_{ON}$ max. - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of On-Resistance measured.

Test Circuits/Timing Diagrams



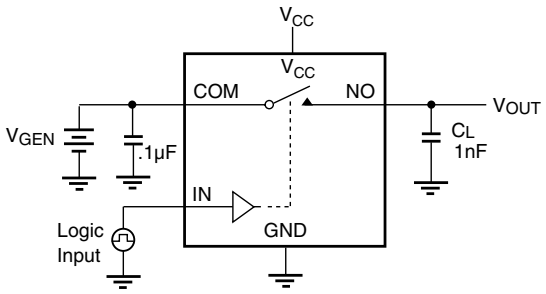


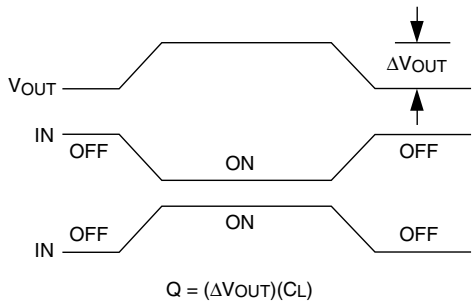
C_L INCLUDES FIXTURE AND STRAY CAPACITANCE

$$V_{OUT} = V_{NO}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

LOGIC INPUT WAVEFORMS INVERTED FOR SWITCHES THAT HAVE OPPOSITE LOGIC
* 1.5V FOR 3.3V SUPPLY

Figure 1. Switching Time





Q = (ΔVOUT)(CL)

Figure 2. Charge Injection

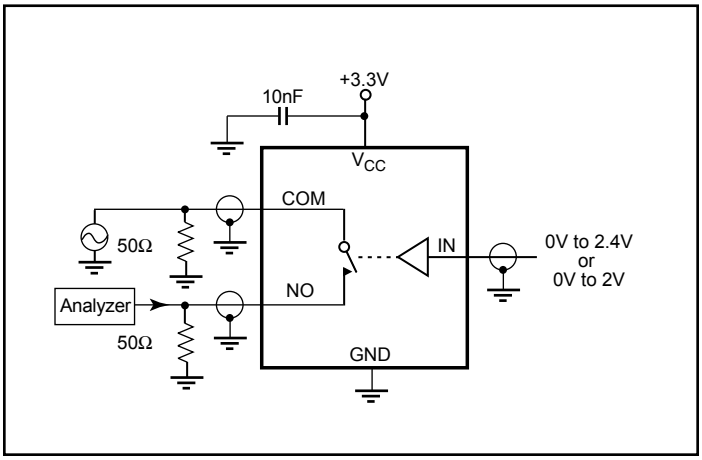


Figure 3. Off Isolation

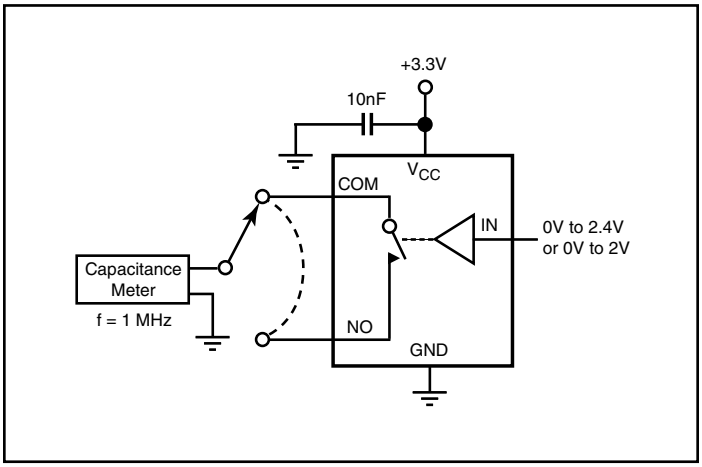
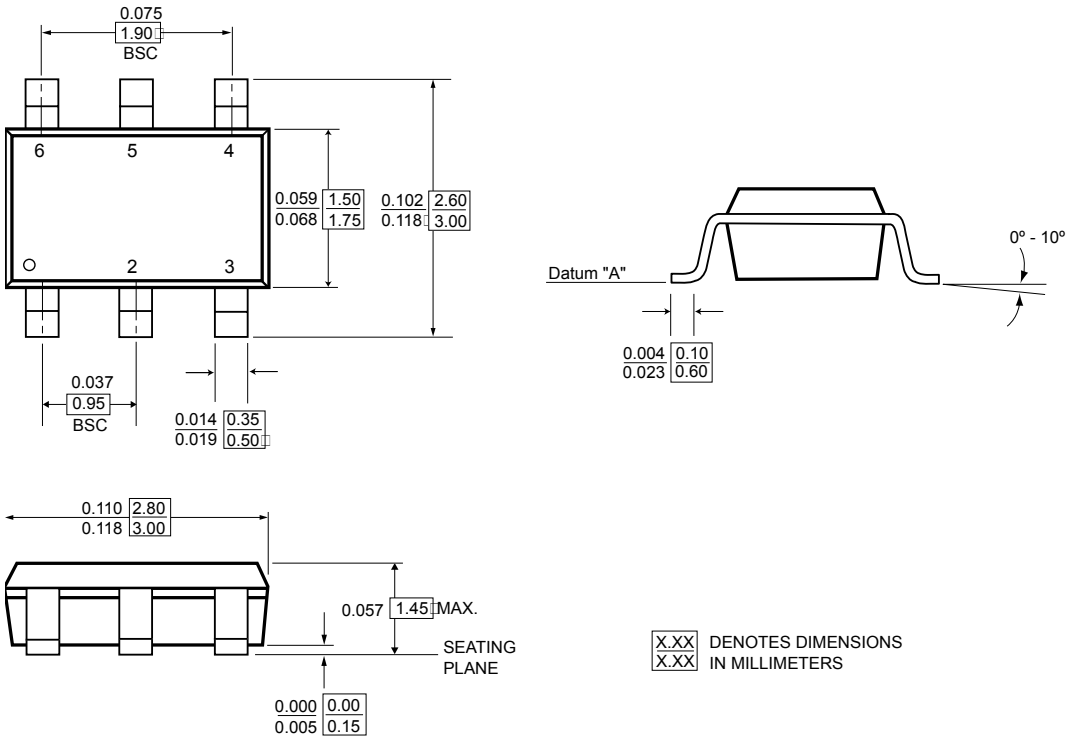
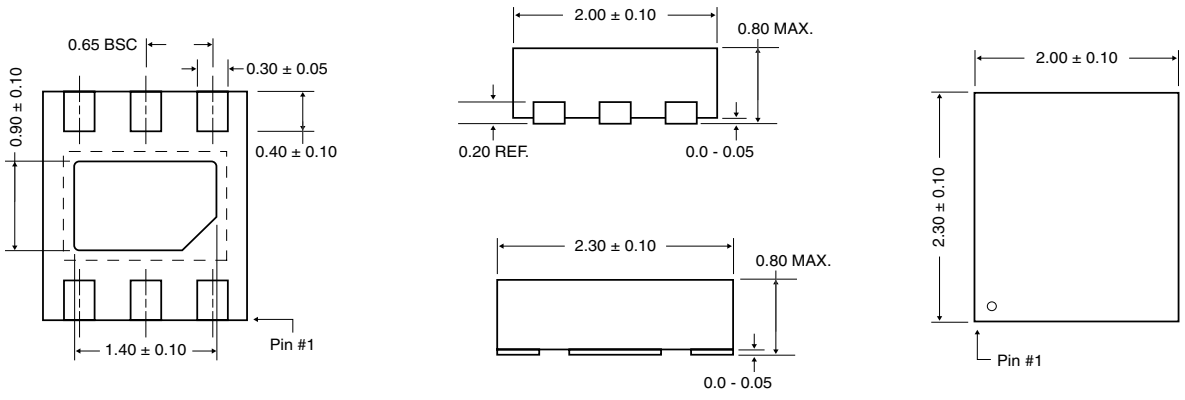


Figure 4. Channel On/Off Capacitance

Packaging Mechanical: 6-Pin SOT-23 (T)



Packaging Mechanical: 6-Pin TDFN (ZC)



Ordering Information

Ordering Code	Package Code	Package Description	Top Mark
PI3A4628TX	T	6-pin Small Compact, SOT-23	ZB
PI3A4628TEX	T	Pb-free & Green, 6-pin Small Compact, SOT-23	ZB
PI3A4628ZCEX	ZC	Pb-free & Green, 6-contact Small Compact, TDFN	ZB

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. X = Tape/Reel
3. Number of transistors = TBD