TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WT74FU

D-Type Flip Flop with Preset and Clear

The TC7WT74FU is high speed CMOS D-FLIP FLOP fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar schottky TTL while maintaining the CMOS low power dissipation.

The input threshold levels are compatible with TTL output voltage.

The signal level applied to the D-INPUT is tranceferred to Q-OUTPUT during the positive going trasition of the CK pulse.

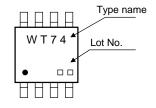
CLEAR and PRESET are independent of the CK and are accompished by setting the appropriate input low.

All inputs are equipped with protection circuits against static dichage or transient excess voltage.

Features

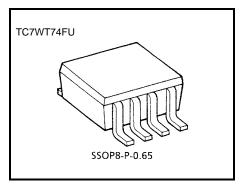
- High speed: f_{MAX} = 53MHz(typ.) at VCC = 5 V
- Low power dissipation: $I_{CC} = 2 \ \mu A \ (max.)$ at $Ta = 25^{\circ}C$
- Compatible with TTL outputs: $V_{IL} = 3 V(max.)$ at Ta=25°C
- Output drive capability: 10 LSTTL Loads
- Symmetrical output impedance: |IOH| = IOL = 4mA(min.)

Marking



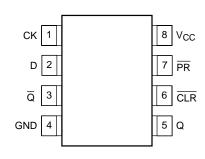
Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5~7	V
DC input voltage	V _{IN}	–0.5~ V _{CC} + 0.5	V
DC output voltage	Vout	–0.5~ V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	ICC	±25	mA
Power dissipation	PD	300	mW
Storage temperature	T _{stg}	-65~150	°C
Lead temperature (10s)	ΤL	260	°C



Weight SSOP8-P-0.65 : 0.02 g (typ.)

Pin Assignment (top view)

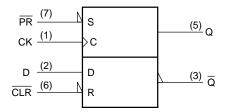


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Truth Table

	Inp	uts		Out	puts	Function
CLR	PR	D	СК	Q	IQ	
L	Н	Х	Х	L	Н	Clear
Н	L	Х	Х	Н	L	Preset
L	L	Х	Х	Н	Н	_
Н	Н	L	Ļ	L	Н	_
Н	Н	Н		Н	L	_
Н	Н	Х		Qn	Qn	No Change





X: Don't care

Recommended Operating Conditions

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	4.5~5.5	V
Input voltage	V _{IN}	0~ V _{CC}	V
Output voltage	Vout	0~5.5	V
Operating temperature	T _{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~500	ns

DC Electrical Characteristics

Characteristics Svm		C) maked	Test Condition		-	Ta = 25°0)	Ta = -40~85°C		Unit		
Chara	ciensiics	Symbol			V _{CC} (V)	Min	Тур.	Max	Min	Max	Unit	
Input	High level	VIH			4.5~5.5	2.0	_	_	2.0	_	V	
voltage	Low level	VIL			4.5~5.5	_		0.8	_	0.8	v	
		igh level VOH	High level VOH	Vou VIN = VIL	$I_{OH} = -20 \ \mu A$	4.5	4.4	4.5	_	4.4	_	V
Output	nigri ievei			or V _{IH}	$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31		4.13		
voltage	age			$V_{IN} = V_{IL}$	$I_{OL}=20~\mu A$	4.5		0.0	0.10	_	0.10	V
	Low level	ow level V _{OL} or	or V _{IH}	I _{OL} = 4 mA	4.5		0.17	0.26		0.33	V	
Input leakag	e current	I _{IN}	$V_{IN} = V_{CC}$	$V_{IN} = V_{CC}$ or GND				±0.1		±1	μA	
	Icc		$V_{IN} = V_{CC}$ or GND		5.5	_	_	2.0	_	20.0	μΑ	
Quiescent supply current		Ісст	PER INPUT: V _{IN} = 0.5 V or 2.4V OTHER INPUT: V _{CC} or GND		5.5	_	_	2.0	_	2.9	μμΑ	

Timing Requirements (Input: $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Symbol Test Condition		Ta =	25°C	Ta = -40~85°C	Unit	
Characteristics	Symbol Test Condition		V _{CC} (V)	Тур	LIMIT	LIMIT	Unit	
Maximum pulse frequency	t _W (L)		4.5	_	25	29	ns	
width (CLOCK)	t _W (H)		5.5	_	20	23	115	
Maximum pulse frequency	t(1.)		4.5	_	30	34	ns	
width (CLR, PR)	t _W (L)		5.5	_	25	28	115	
Minimum set-up time	+-		4.5	_	25	29	ns	
Minimum set-up time	ts	5.5	_	20	23	115		
Minimum hold time	t _h		4.5	_	10	10	ns	
			5.5	_	8	8	115	
Maximum removal	t _{rem}		4.5	_	10	10	ns	
time(CLR , PR)			5.5	_	10	10		
Clock frequency	f		4.5	_	22	16	MHz	
Clock frequency			5.5		25	19	IVI⊓∠	

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

Characteristics	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Output transition time	t _{TLH} t _{THL}	_	_	6	12	ns
Propagation d <u>el</u> ay time (CLOCK – Q, Q)	t _{PLH}	_		17	28	ns
P <u>ropagation</u> delay time (CLR,PR -Q, Q)	t _{PLH} t _{PHL}	_	_	20	30	ns
Maximum clock time	f _{MAX}	_	24	53	_	MHz

AC Electrical Characteristics ($C_L = 15pF$, Input $t_r = t_f = 6ns$)

Characteristics	Symbol	Test Condition			Ta = 25°C		Ta = -40~85°C		Unit
	Symbol	Test Condition	V _{CC} (V)	Min.	Тур.	Max.	Min.	Max.	Unit
Output transition time	t⊤∟H		4.5	_	8	15	_	19	ns
	t _{THL}		5.5		7	13		16	113
Propagation d <u>e</u> lay time (CLOCK – Q, Q)	tPLH		4.5	_	21	33	_	41	
	tPHL		5.5	_	19	35	_	37	ns
Propagation delay time	tPLH	_	4.5	_	23	35	_	43	ns
(CLR, PR - Q, Q)	tPHL		5.5	_	20	32	_	40	
Maximum clock frequency	f	_	4.5	22	48	_	16		MHz
Maximum clock frequency	fMAX		5.5	25	53	_	19		
Input capacitance	CIN	_		_	5	10	_	10	pF
Power dissipation capacitance	C _{PD}			_	34	_	_	10	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

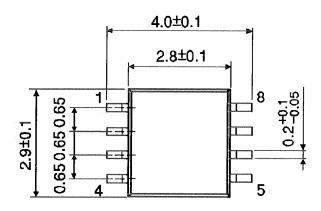
 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

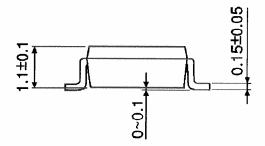
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Package Dimensions

SSOP8-P-0.65

Unit : mm





Weight: 0.02 g (typ.)

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