

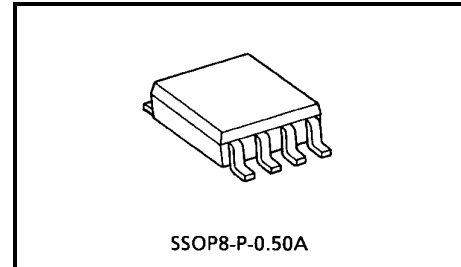
TC7WBL126AFK

Low-Voltage Dual Bus Switch

The TC7WBL126AFK provides two bits of low-voltage high-speed bus switching. The low ON-resistance of the switch allows connections to be made with minimal propagation delay and while maintaining CMOS low power dissipation.

The device comprises dual 2-bit switches with separate bus enable (OE) signals. When OE is high, the switch is on and port A is connected to port B. When OE is low, the switch is off and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits to guard against static discharge.

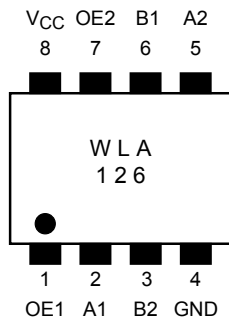


Weight: 0.01 g (typ.)

Features

- Operating voltage range: $V_{CC} = 2$ to 3.6 V
- High speed: $t_{pd} = 0.31$ ns (max) @ 3 V
- Ultra-low ON-resistance: $R_{ON} = 5 \Omega$ (typ.) @ 3 V
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Power-down protection provided on inputs (OE input only)
- Package: US8

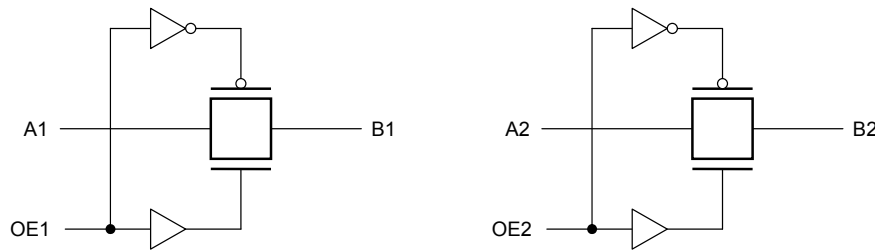
Pin Assignment (top view)



Truth Table

Inputs	Function
OE	
H	A port = B port
L	Disconnect

Logic Diagram



Absolute Maximum Ratings (Note) (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5~4.6	V
Control pin input voltage	V_{IN}	-0.5~4.6	V
Switch terminal I/O voltage	V_S	-0.5~ $V_{CC}+0.5$	V
Clump diode current	Control input pin	-50	mA
	Switch terminal	±50	
Switch I/O current	I_S	128	mA
Power dissipation	P_D	200	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	-65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristic	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~3.6	V
Control pin input voltage	V_{IN}	0~3.6	V
Switch I/O voltage	V_S	0~ V_{CC}	V
Operating temperature	T_{opr}	-40~85	°C
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristic	Symbol	Test Condition	V _{CC} (V)	Min	Typ.	Max	Unit
High-level control input voltage	V _{IH}	—	2.0 to 3.6	0.7 × V _{CC}	—	—	V
Low-level control input voltage	V _{IL}	—	2.0 to 3.6	—	—	0.3 × V _{CC}	
Control input current	I _{IN}	V _{IN} = 0 to 3.6 V	2.0 to 3.6	—	—	±1.0	μA
Power off leakage current	I _{OFF}	OE = 0 to 3.6 V	0	—	—	±1.0	μA
Off-stage leakage current (switch off)	I _{SZ}	A, B = 0 to V _{CC} , OE = GND	2.0 to 3.6	—	—	±1.0	μA
Switch ON-resistance (Note 2)	R _{ON}	V _{IS} = 0 V, I _{IS} = 30 mA (Note 1)	3.0	—	2	7	Ω
		V _{IS} = 3.0 V, I _{IS} = 30 mA (Note 1)	3.0	—	4	9	
		V _{IS} = 2.4 V, I _{IS} = 15 mA (Note 1)	3.0	—	5	15	
		V _{IS} = 0 V, I _{IS} = 24 mA (Note 1)	2.3	—	3	10	
		V _{IS} = 2.3 V, I _{IS} = 24 mA (Note 1)	2.3	—	5	15	
		V _{IS} = 2.0 V, I _{IS} = 15 mA (Note 1)	2.3	—	8	25	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0	3.6	—	—	10	μA

Note 1: All typical values are at Ta = 25°C.

Note 2: Measured by voltage drop between A and B pins at indicated current through the switch. ON-resistance is determined by the lower of the voltages on the two pins (A or B).

AC Characteristics (Ta = -40 to 85°C)

Characteristic	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Propagation delay (bus to bus)	t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note)	3.3 ± 0.3	—	0.31	ns
			2.5 ± 0.2	—	0.52	
Output enable time	t _{pZL} t _{pZH}	Figure 1, Figure 3	3.3 ± 0.3	—	7	ns
			2.5 ± 0.2	—	10	
Output disable time	t _{pLZ} t _{pHZ}	Figure 1, Figure 3	3.3 ± 0.3	—	8	ns
			2.5 ± 0.2	—	9	

Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical ON-resistance of the switch and the 50 pF load capacitance when driven by an ideal voltage from the source (zero output impedance).

Capacitance (Ta = 25°C)

Characteristic	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Control input capacitance	C _{IN}		3.0	3	pF
Switch terminal capacitance	C _{I/O}	OE = GND	3.0	23	pF

AC Test Circuit

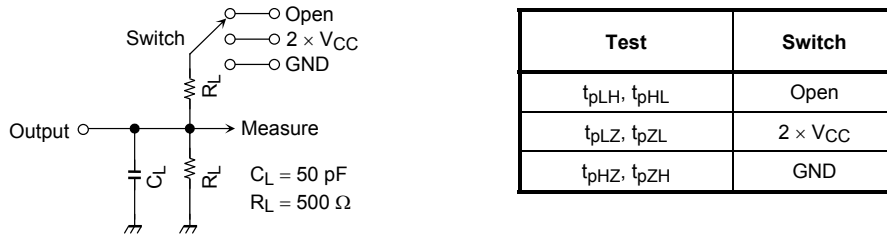


Figure 1

AC Waveforms

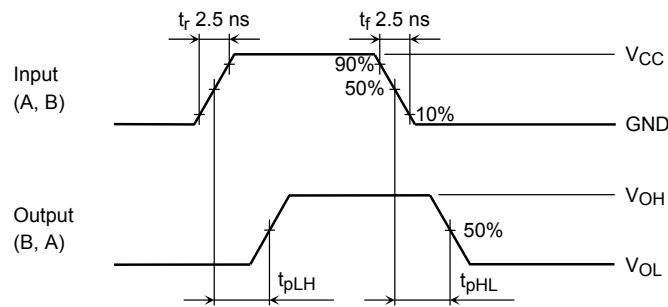


Figure 2 t_{pLH}, t_{pHL}

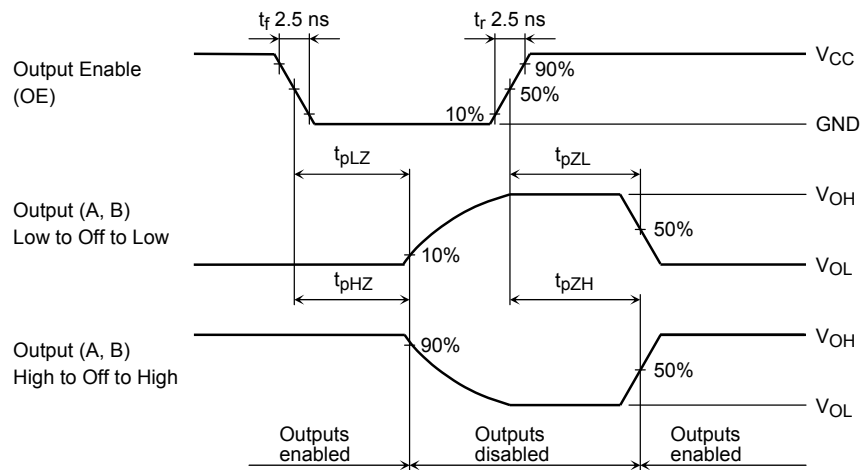
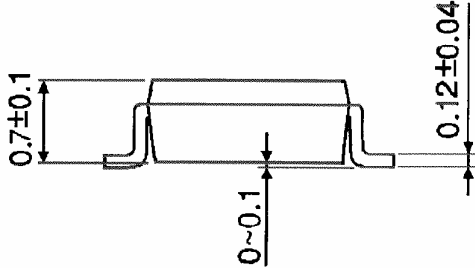
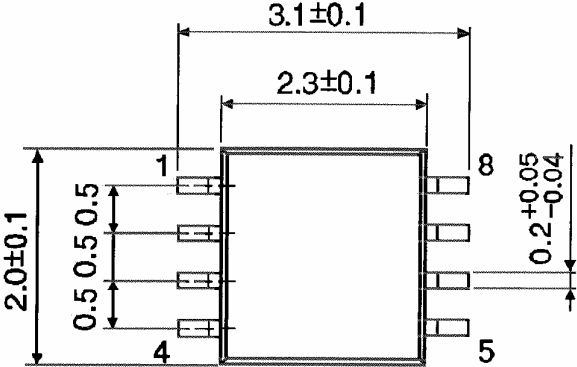


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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20070701-EN GENERAL

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