TOSHIBA TC7W00F/FU/FK

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7W00F, TC7W00FU, TC7W00FK

DUAL 2-INPUT NAND GATE

The TC7W00 is a high speed C2MOS 2-INPUT NAND GATE fabricated with silicon gate C2MOS technology.

It achives the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

•	High Speed	
		V _{CC} = 5V

• Low Power Dissipation
$$I_{CC} = 1\mu A$$
 (Max.) at

• High Noise Immunity
$$V_{NIH} = V_{NIL}$$

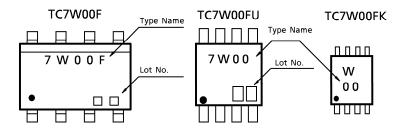
= 28% V_{CC} (Min.)

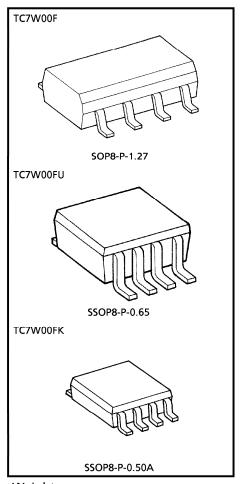
• Symmetrical Output Impedance ...
$$|I_{OH}| = I_{OL} = 4mA$$

Balanced Propagation Delays $t_{pLH} = t_{pHL}$

Wide Operating Voltage Range ... $V_{CC(opr)} = 2 \sim 6V$

MARKING





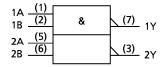
Weight SOP8-P-1.27 : 0.05g (Typ.) SSOP8-P-0.65 : 0.02g (Typ.) SSOP8-P-0.50A : 0.01g (Typ.)

2001-05-31

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V _C C	-0.5~7	V
DC Input Voltage	VIN	-0.5~V _{CC} +0.5	V
DC Output Voltage	Vout	-0.5~V _{CC} +0.5	V
Input Diode Current	ΙΙΚ	± 20	mA
Output Diode Current	^I ОК	± 20	mA
DC Output Current	IOUT	± 25	mA
DC V _{CC} / Ground Current	lcc	± 25	mA
Payer Dissipation	D-	300 (FM8, SM8)	mW
Power Dissipation	PD	200 (US8)	mvv
Storage Temperature	T _{stg}	-65∼150	°C
Lead Temperature (10s)	TL	260	°C

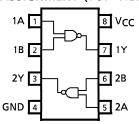
LOGIC DIAGRAM



TRUTH TABLE

А	В	Υ
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

PIN ASSIGNMENT (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	2~6	V
Input Voltage	VIN	0~V _{CC}	V
Output Voltage	Vout	0~V _{CC}	V
Operating Temperature	T _{opr}	- 40~85	°C
		$0 \sim 1000 \text{ (V}_{CC} = 2.0\text{V)}$	
Input Rise and Fall Time	t _r , t _f	0~ 500 (V _{CC} = 4.5V)	ns
		$0 \sim 400 \ (V_{CC} = 6.0V)$	

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	. TEST CONDITION			Т	a = 25°	'n	Ta = −40~85°C		UNIT										
CHARACTERISTIC	3 TIVIBOL			Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	OIVII										
High Lovel				2.0	1.5	_	_	1.5	_											
High-Level Input Voltage	V _{IH}		_	4.5	3.15	—	—	3.15	<u> </u>	V										
input voitage				6.0	4.2	_	_	4.2	_											
Low-Level				2.0	_	_	0.5	_	0.5											
Input Voltage	V _{IL}		_	4.5	_	_	1.35	—	1.35	V										
input voitage				6.0	_	_	1.8	_	1.8											
		V _{IN} = V _{IH} or V _{IL}		2.0	1.9	2.0	—	1.9	_											
High Lovel	V _{ОН}		$I_{OH} = -20\mu A$	4.5	4.4	4.5	—	4.4	_											
High-Level				6.0	5.9	6.0	—	5.9		V										
Output Voltage			$I_{OH} = -4mA$	4.5	4.18	4.31	—	4.13	_											
			$I_{OH} = -5.2 \text{mA}$	6.0	5.68	5.80	_	5.63												
				2.0	_	0.0	0.1	_	0.1											
l and land			$I_{OL} = 20 \mu A$	4.5	—	0.0	0.1	—	0.1											
Low-Level	VOL	V_{OL} $V_{IN} = V_{IH}$		6.0	_	0.0	0.1	_	0.1	V										
Output Voltage			I _{OL} = 4mA	4.5	_	0.17	0.26	_	0.33											
													$I_{OL} = 5.2 \text{mA}$	6.0	_	0.18	0.26	_	0.33	
Input Leakage	IN	V _{IN} = V _{CC} o	or GND	6.0	_	_	± 0.1		± 1.0											
Current	.114	114 CC								μ A										
Quiescent Supply Current	lcc	V _{IN} = V _{CC} o	or GND	6.0	_	_	1.0	_	10.0	μ., τ										

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Т	UNIT		
CHARACTERISTIC	3 TIVIBOL	TEST CONDITION	MIN.	TYP.	MAX.	ONIT
Output Transition Time	t _{TLH} t _{THL}	_	_	4	8	ns
Propagation Delay Time	t _{pLH}	_	_	6	12	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

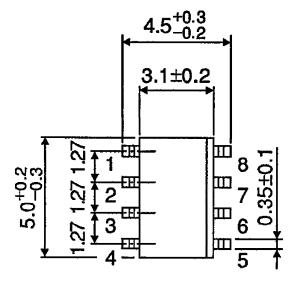
CHARACTERISTIC	SYMBOL	TEST CONDITION)NI		Ta = 25°C			$Ta = -40 \sim 85^{\circ}C$		
CHARACTERISTIC	STIVIBOL	TEST CONDITION	Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT	
Output Transition	+		2.0	_	25	75	_	95		
Time	t _{TLH}	_	4.5	_	7	15	_	19	ns	
Time	t _{THL}		6.0	_	6	13	_	16		
Propagation Delay	4		2.0	_	27	75	_	95		
	t _{pLH}	_	4.5	—	9	15	l —	19	ns	
Time	t _{pHL}		6.0	_	8	13	—	16		
Input Capacitance	CIN	_		_	5	10	_	10		
Power Dissipation Capacitance	C _{PD}	(Note 1)		_	20	_	_		pF	

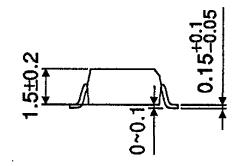
(Note 1) CpD is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder. $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2$ (per gate)

PACKAGE DIMENSIONS SOP8-P-1.27

Unit: mm

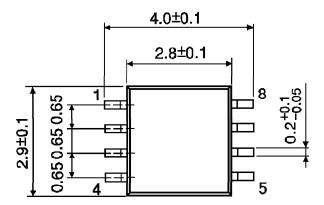


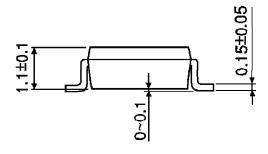


Weight: 0.05g (Typ.)

PACKAGE DIMENSIONS SSOP8-P-0.65

Unit: mm

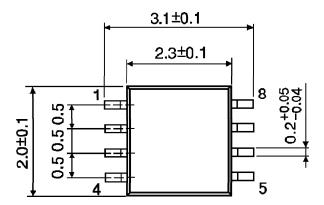


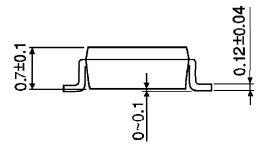


Weight: 0.02g (Typ.)

PACKAGE DIMENSIONS SSOP8-P-0.50A

Unit: mm





Weight: 0.01g (Typ.)

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000707EBA

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