

FEATURES
Ultralow on resistance

- 0.28 Ω typical
- 0.48 Ω max at 125°C

Excellent audio performance, ultralow distortion

- 0.025 Ω typical
- 0.052 Ω max R_{ON} flatness

1.65 V to 3.6 V single supply
High current carrying capability

- 300 mA continuous current
- 500 mA peak current

Automotive temperature range: -40°C to +125°C
Rail-to-rail operation
Typical power consumption (<0.01 μ W)
Known good die (KGD): these die are fully guaranteed to data sheet specifications
APPLICATIONS

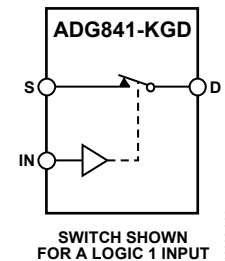
- Handsets
- PDA's
- MP3 players
- Power routing
- Battery-powered systems
- Communication systems
- Modems
- PCMCIA cards

GENERAL DESCRIPTION

The [ADG841-KGD](#) is a low voltage CMOS device containing a single-pole, single-throw (SPST) switch. The [ADG841-KGD](#) is closed for a Logic 1 input. The device offers ultralow on resistance of less than 0.48 Ω over the full temperature range. The [ADG841-KGD](#) is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies.

Additional application and technical information can be found in the [ADG841](#) data sheet.

FUNCTIONAL BLOCK DIAGRAM


SWITCH SHOWN FOR A LOGIC 1 INPUT

Figure 1.

PRODUCT HIGHLIGHTS

1. <0.48 Ω over full temperature range of -40°C to +125°C.
2. Compatible with 1.8 V CMOS logic.
3. High current handling capability (300 mA continuous current at 3.3 V).
4. Low THD + N (0.02% typ).

Table 1. [ADG841-KGD](#) Truth Table

Logic (IN)	ADG841-KGD
0	Off
1	On

Rev. 0

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TABLE OF CONTENTS

Specifications—2.7 V to 3.6 V	3	Pad Configuration and Function Descriptions	7
Specifications—2.5 V \pm 0.2 V	4	Test Circuits	8
Specifications—1.65 V to 1.95	5	Outline Dimensions	9
Absolute Maximum Ratings	6	Die Specifications and Assembly Recommendations	9
ESD Caution	6	Ordering Guide	9

REVISION HISTORY

11/11—Revision 0: Initial Version

SPECIFICATIONS—2.7 V TO 3.6 V¹

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	$V_{DD} = 2.7\text{ V}$
On Resistance (R_{ON})	0.28			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = -100\text{ mA}$
	0.37	0.43	0.48	Ω max	Figure 3
On Resistance Flatness ($R_{FLAT(ON)}$)	0.025			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_{DS} = -100\text{ mA}$
	0.034	0.044	0.052	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage I_S (OFF)	± 0.2			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; Figure 4
Channel On Leakage I_D , I_S (ON)	± 0.2			nA typ	$V_S = V_D = 0.6\text{ V or }3.3\text{ V}$; Figure 5
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	3.2			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	10.5			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	14	15.5	16.5	ns max	$V_S = 1.5\text{ V}$; Figure 6
t_{OFF}	6.5			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	7.8	8	8.2	ns max	$V_S = 1.5\text{ V}$; Figure 6
Charge Injection	200			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; Figure 7
Off Isolation	−54			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; Figure 8
Total Harmonic Distortion (THD + N)	0.012			%	$R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 3\text{ V p-p}$
Insertion Loss	−0.02			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Figure 9
−3 dB Bandwidth	21			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; Figure 9
C_S (OFF)	160			pF typ	
C_D (OFF)	160			pF typ	
C_D , C_S (ON)	238			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1	4	μA max	

¹ Temperature range is -40°C to $+125^\circ\text{C}$

² Guaranteed by design; not subject to production test.

SPECIFICATIONS—2.5 V ± 0.2 V¹V_{DD} = 2.5 V ± 0.2 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	
On Resistance (R _{ON})	0.3			Ω typ	V _{DD} = 2.3 V, V _S = 0 V to V _{DD} , I _{DS} = −100 mA
	0.35	0.4	0.45	Ω max	Figure 3
On Resistance Flatness (R _{FLAT(ON)})	0.025			Ω typ	V _{DD} = 2.3 V, V _S = 0 V to V _{DD} , I _{DS} = −100 mA
	0.04	0.05	0.05	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage I _S (OFF)	±0.2			nA typ	V _{DD} = 2.7 V
Channel On Leakage I _D , I _S (ON)	±0.2			nA typ	V _S = 0.6 V/2.4 V, V _D = 2.4 V/0.6 V; Figure 4
					V _S = V _D = 0.6 V or 2.4 V; Figure 5
DIGITAL INPUTS					
Input High Voltage, V _{INH}			1.7	V min	
Input Low Voltage, V _{INL}			0.7	V max	
Input Current, I _{INL} or I _{INH}	0.005			μA typ	V _{IN} = V _{INL} or V _{INH}
			±0.1	μA max	
Digital Input Capacitance, C _{IN}	3.2			pF typ	
DYNAMIC CHARACTERISTICS²					
t _{ON}	13			ns typ	R _L = 50 Ω, C _L = 35 pF
	16.5	18	19	ns max	V _S = 1.5 V; Figure 6
t _{OFF}	7			ns typ	R _L = 50 Ω, C _L = 35 pF
	8.2	8.4	8.6	ns max	V _S = 1.5 V; Figure 6
Charge Injection	150			pC typ	V _S = 1.25 V, R _S = 0 Ω, C _L = 1 nF; Figure 7
Off Isolation	−54			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; Figure 8
Total Harmonic Distortion (THD + N)	0.022			%	R _L = 32 Ω, f = 20 Hz to 20 kHz, V _S = 1.5 V p-p
Insertion Loss	−0.02			dB typ	R _L = 50 Ω, C _L = 5 pF; Figure 9
−3 dB Bandwidth	21			MHz typ	R _L = 50 Ω, C _L = 5 pF; Figure 9
C _S (OFF)	170			pF typ	
C _D (OFF)	170			pF typ	
C _D , C _S (ON)	238			pF typ	
POWER REQUIREMENTS					
I _{DD}	0.003			μA typ	V _{DD} = 2.7 V
		1	4	μA max	Digital inputs = 0 V or 2.7 V

¹ Temperature range is −40°C to +125°C.² Guaranteed by design; not subject to production test.

SPECIFICATIONS—1.65 V TO 1.95¹

$V_{DD} = 1.65 \text{ V to } 1.95 \text{ V}$, $GND = 0 \text{ V}$, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.37			Ω typ	$V_{DD} = 1.8 \text{ V}$, $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = -100 \text{ mA}$ Figure 3
	0.4	0.84	0.84	Ω max	
	0.6	1.8	1.8	Ω max	$V_{DD} = 1.65 \text{ V}$, $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = -100 \text{ mA}$
On Resistance Flatness ($R_{FLAT(ON)}$)	0.17			Ω typ	$V_{DD} = 1.65 \text{ V}$, $V_S = 0 \text{ V to } V_{DD}$, $I_{DS} = -100 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (OFF)	± 0.2			nA typ	$V_{DD} = 1.95 \text{ V}$ $V_S = 0.6 \text{ V}/1.65 \text{ V}$, $V_D = 1.65 \text{ V}/0.6 \text{ V}$; Figure 4
Channel On Leakage I_D , I_S (ON)	± 0.2			nA typ	$V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}$; Figure 5
DIGITAL INPUTS					
Input High Voltage, V_{INH}			$0.65 V_{DD}$	V min	
Input Low Voltage, V_{INL}			$0.35 V_{DD}$	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS²					
t_{ON}	19			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$; Figure 6
	26	28	30	ns max	
t_{OFF}	8			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$ $V_S = 1.5 \text{ V}$; Figure 6
	9.5	9.8	10	ns max	
Charge Injection	100			pC typ	$V_S = 1 \text{ V}$, $R_S = 0 \text{ V}$, $C_L = 1 \text{ nF}$; Figure 7
Off Isolation	−54			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$; Figure 8
Total Harmonic Distortion (THD + N)	0.14			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz to } 20 \text{ kHz}$, $V_S = 1.2 \text{ V p-p}$
Insertion Loss	−0.02			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; Figure 9
−3 dB Bandwidth	21			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$; Figure 9
C_S (OFF)	178			pF typ	
C_D (OFF)	178			pF typ	
C_D , C_S (ON)	238			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 1.95 \text{ V}$ Digital inputs = 0 V or 1.95 V
		1	4	μA max	

¹ Temperature range -40°C to $+125^\circ\text{C}$.

² Guaranteed by design; not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	-0.3 V to +4.6 V
Analog Inputs ¹	-0.3 V to $V_{DD} + 0.3$ V
Digital Inputs ¹	-0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C

¹ Overvoltages at S or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PAD CONFIGURATION AND FUNCTION DESCRIPTIONS

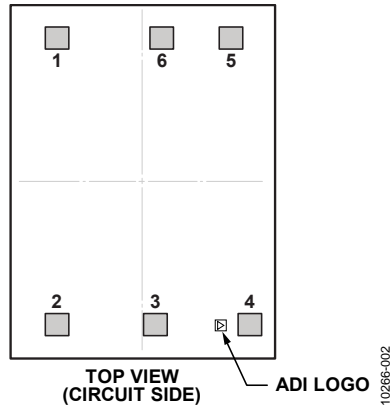


Figure 2. Pad Configuration

Table 6. Pad Function Descriptions

Pad No.	X-Axis (μm)	Y-Axis (μm)	Mnemonic	Pad Type	Description
1	-254	401	V _{DD}	Single	Positive Power Supply Pad.
2	-254	-401	IN	Single	Logic Control Input Pad.
3	6	-401	S	Single	Source Pad.
4	306	-401	GND	Single	Ground Pad.
5	249	401	NC	Single	No Connect.
6	39	401	D	Single	Drain Pad.

TEST CIRCUITS

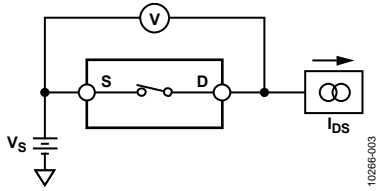


Figure 3. On Resistance

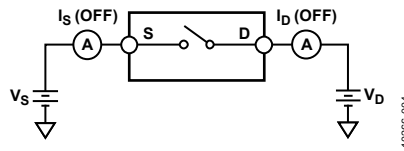


Figure 4. Off Leakage

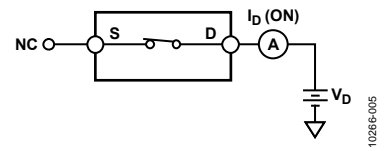


Figure 5. On Leakage

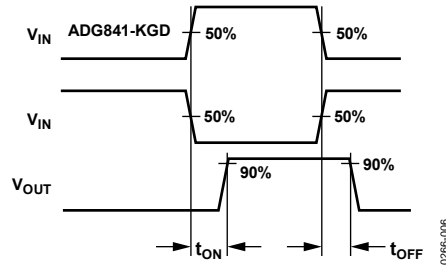
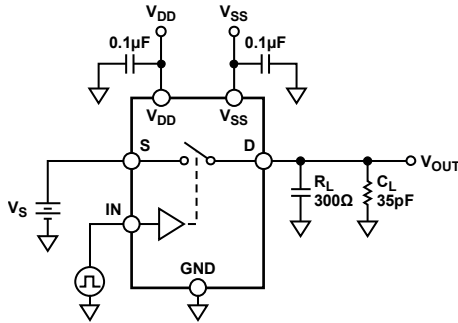


Figure 6. Switching Times, t_{ON} , t_{OFF}

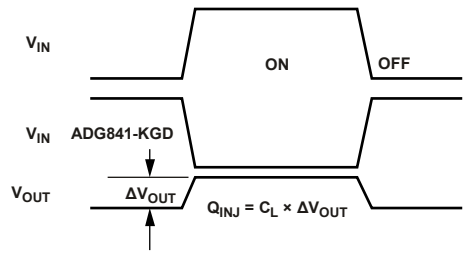
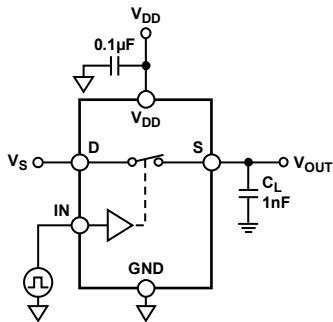
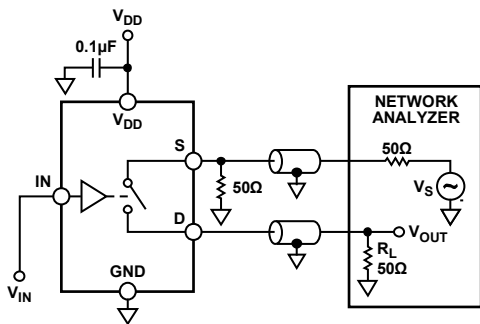
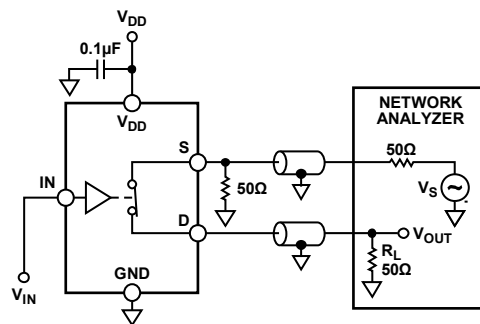


Figure 7. Charge Injection



ADG841-KGD - $V_{IN} = 0$
 OFF ISOLATION = $20 \log \frac{V_{OUT}}{V_S}$

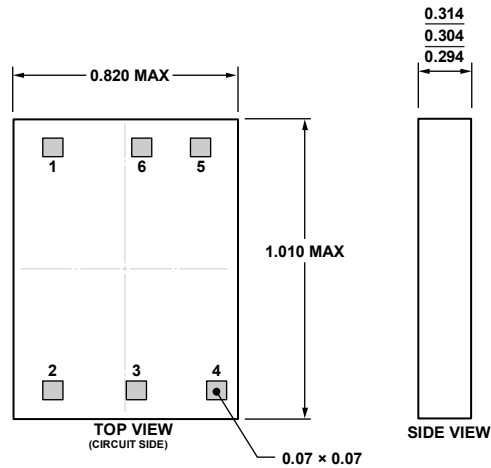
Figure 8. Off Isolation



INSERTION LOSS = $20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_{OUT \text{ WITHOUT SWITCH}}}$

Figure 9. Bandwidth

OUTLINE DIMENSIONS



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Figure 10. 6-Pad Bare Die [CHIP]
(C-6-3)
Dimensions shown in millimeters

DIE SPECIFICATIONS AND ASSEMBLY RECOMMENDATIONS

Table 7. Die Specifications

Parameter	Value	Unit ¹
Chip Size	735 × 925	µm
Scribe Line Width	85 × 85	µm
Die Size	820 × 1010	µm (maximum)
Thickness	304 ± 10	µm
Bond Pad	70 × 70	µm (minimum)
Bond Pad Composition	98.5 Al, 1 Si, 0.5 Cu	%
Backside	Bare	N/A
Passivation	Nitride	N/A

¹ N/A means not applicable.

Table 8. Assembly Recommendations

Assembly Component	Recommendation
Die Attach	Epoxy adhesive
Bonding Method	Gold ball or aluminum wedge
Bonding Sequence	Four first

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG841-KGD-CHIPS	-40°C to +125°C	6-Pad Bare Die [CHIP]	C-6-3

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