

**FEATURES**

- 0.5  $\Omega$  typical on resistance**
- 0.8  $\Omega$  maximum on resistance at 125°C**
- 1.65 V to 3.6 V operation**
- Automotive temperature range: -40°C to +125°C**
- High current carrying capability: 300 mA continuous**
- Rail-to-rail switching operation**
- Fast-switching times <20 ns**
- Typical power consumption (<0.1  $\mu$ W)**

**APPLICATIONS**

- Cellular phones**
- PDA's**
- MP3 players**
- Power routing**
- Battery-powered systems**
- PCMCIA cards**
- Modems**
- Audio and video signal routing**
- Communication systems**

**GENERAL DESCRIPTION**

The ADG836 is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.8  $\Omega$  over the full temperature range. The ADG836 is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on, and has an input signal range that extends to the supplies. The ADG836 exhibits break-before-make switching action.

The ADG836 is available in a 10-lead MSOP and a 3 mm  $\times$  3 mm 12-lead LFCSP.

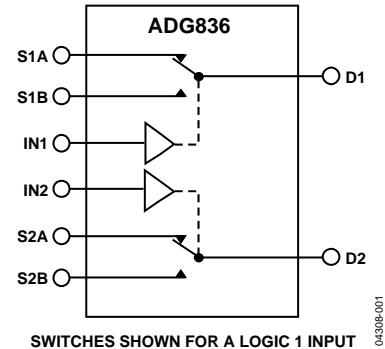


Figure 1.

**PRODUCT HIGHLIGHTS**

1. <0.8  $\Omega$  over full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.02% typ).
6. 3 mm  $\times$  3 mm LFCSP package and 10-lead MSOP package.

**Rev. A**

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.  
Tel: 781.329.4700 [www.analog.com](http://www.analog.com)  
Fax: 781.461.3113 © 2005 Analog Devices, Inc. All rights reserved.

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## REVISION HISTORY

### 4/05—Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Table 1.....	3
Changes to Table 2.....	4
Changes to Table 3.....	5
Changes to Ordering Guide .....	13

### Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 1.**

Parameter	Temperature <sup>1</sup>			Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C	−40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.5			$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$ , $I_S = 100\text{ mA}$ ; Figure 19
	0.65	0.75	0.8	$\Omega$ max	
On Resistance Match	0.04			$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0.65\text{ V}$ , $I_S = 100\text{ mA}$
Between Channels ( $\Delta R_{ON}$ )		0.075	0.08	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.1			$\Omega$ typ	$V_{DD} = 2.7\text{ V}$ , $V_S = 0\text{ V to }V_{DD}$
		0.15	0.16	$\Omega$ max	$I_S = 100\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$ , $V_D = 3.3\text{ V}/0.6\text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6\text{ V or }3.3\text{ V}$ ; Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	21			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	26	28	29	ns max	$V_S = 1.5\text{ V}/0\text{ V}$ ; Figure 22
$t_{OFF}$	4			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
	7	8	9	ns max	$V_S = 1.5\text{ V}$ ; Figure 22
Break-Before-Make Time Delay ( $t_{BBM}$ )	17		5	ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$
				ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$ ; Figure 23
Charge Injection	40			pC typ	$V_S = 1.5\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Figure 24
Off Isolation	−67			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	−90			dB typ	S1A–S2A/S1B–S2B, $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; Figure 28
	−67			dB typ	S1A–S1B/S2A–S2B, $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 100\text{ kHz}$ ; Figure 27
Total Harmonic Distortion (THD + N)	0.02			%	$R_L = 32\ \Omega$ , $f = 20\text{ Hz to }20\text{ kHz}$ , $V_S = 2\text{ V p-p}$
Insertion Loss	−0.05			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 26
−3 dB Bandwidth	57			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	
$C_D$ , $C_S$ (ON)	75			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003			$\mu\text{A}$ typ	$V_{DD} = 3.6\text{ V}$
		1	4	$\mu\text{A}$ max	Digital inputs = 0 V or 3.6 V

<sup>1</sup> Temperature range for Y version is  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup> Guaranteed by design, not subject to production test.

# ADG836

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$ ,  $GND = 0 \text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	Temperature <sup>1</sup>			Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.65			$\Omega$ typ	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V to } V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
	0.72	0.8	0.88	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.04			$\Omega$ typ	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0.7 \text{ V}$ , $I_S = 100 \text{ mA}$
		0.08	0.085	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.16			$\Omega$ typ	$V_{DD} = 2.3 \text{ V}$ , $V_S = 0 \text{ V to } V_{DD}$ , $I_S = 100 \text{ mA}$
		0.23	0.24	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_{DD} = 2.7 \text{ V}$ $V_S = 0.6 \text{ V}/2.4 \text{ V}$ , $V_D = 2.4 \text{ V}/0.6 \text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6 \text{ V or } 2.4 \text{ V}$ ; Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			1.7	V min	$V_{IN} = V_{INL} \text{ or } V_{INH}$
Input Low Voltage, $V_{INL}$			0.7	V max	
Input Current				$\mu\text{A}$ typ	
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ max	
			$\pm 0.1$	pF typ	
$C_{IN}$ , Digital Input Capacitance	4				
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	23			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	29	30	31	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$ ; Figure 22
$t_{OFF}$	5			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	7	8	9	ns max	$V_S = 1.5 \text{ V}$ ; Figure 22
Break-before-Make Time Delay ( $t_{BBM}$ )	17			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$ ; Figure 23
Charge Injection	30			pC typ	$V_S = 1.25 \text{ V}$ , $R_S = 0 \Omega$ , $C_L = 1 \text{ nF}$ ; Figure 24
Off Isolation	-67			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	-90			dB typ	S1A-S2A/S1B-S2B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 28
	-67			dB typ	S1A-S1B/S2A-S2B, $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 27
Total Harmonic Distortion (THD + N)	0.022			%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , $V_S = 1.5 \text{ V p-p}$
Insertion Loss	-0.06			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
-3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	
$C_D$ , $C_S$ (ON)	75			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003			$\mu\text{A}$ typ	$V_{DD} = 2.7 \text{ V}$ Digital inputs = 0 V or 2.7 V
		1	4	$\mu\text{A}$ max	

<sup>1</sup> Temperature range for Y version is -40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

$V_{DD} = 1.65 \text{ V} \pm 1.95 \text{ V}$ , GND = 0 V, unless otherwise noted.

**Table 3.**

Parameter	Temperature <sup>1</sup>			Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	1			$\Omega$ typ	$V_{DD} = 1.8 \text{ V}$ , $V_S = 0 \text{ V to } V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
	1.4	2.2	2.2	$\Omega$ max	
	2	4	4	$\Omega$ max	$V_{DD} = 1.65 \text{ V}$ , $V_S = 0 \text{ V to } V_{DD}$ , $I_S = 100 \text{ mA}$ ; Figure 19
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.1			$\Omega$ typ	$V_{DD} = 1.65 \text{ V}$ , $V_S = 0.7 \text{ V}$ , $I_S = 100 \text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (OFF)	$\pm 0.2$			nA typ	$V_{DD} = 1.95 \text{ V}$ $V_S = 0.6 \text{ V}/1.65 \text{ V}$ , $V_D = 1.65 \text{ V}/0.6 \text{ V}$ ; Figure 20
Channel On Leakage $I_D$ , $I_S$ (ON)	$\pm 0.2$			nA typ	$V_S = V_D = 0.6 \text{ V or } 1.65 \text{ V}$ ; Figure 21
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			$0.65 V_{DD}$	V min	
Input Low Voltage, $V_{INL}$			$0.35 V_{DD}$	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	4			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	28			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	37	38	39	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$ ; Figure 22
$t_{OFF}$	7			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
	9	10	11	ns max	$V_S = 1.5 \text{ V}$ ; Figure 22
Break-Before-Make Time Delay ( $t_{BBM}$ )	21			ns typ	$R_L = 50 \Omega$ , $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1 \text{ V}$ ; Figure 23
Charge Injection	20			pC typ	$V_S = 1 \text{ V}$ , $R_S = 0 \text{ V}$ , $C_L = 1 \text{ nF}$ ; Figure 24
Off Isolation	-67			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 25
Channel-to-Channel Crosstalk	-90			dB typ	S1A-S2A/S1B-S2B; $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 28
	-67			dB typ	S1A-S1B/S2A-S2B; $R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ , $f = 100 \text{ kHz}$ ; Figure 27
Total Harmonic Distortion, THD	0.14			%	$R_L = 32 \Omega$ , $f = 20 \text{ Hz to } 20 \text{ kHz}$ , $V_S = 1.2 \text{ V p-p}$
Insertion Loss	-0.08			dB typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
-3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$ , $C_L = 5 \text{ pF}$ ; Figure 26
$C_S$ (OFF)	25			pF typ	
$C_D$ , $C_S$ (ON)	75			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.003			$\mu\text{A typ}$ $\mu\text{A max}$	$V_{DD} = 1.95 \text{ V}$ Digital inputs = 0 V or 1.95 V
		1.0	4		

<sup>1</sup> Temperature range for Y version is -40°C to +125°C.

<sup>2</sup> Guaranteed by design, not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

**Table 4.**

Parameter	Rating
V <sub>DD</sub> to GND	−0.3 V to +4.6 V
Analog Inputs <sup>1</sup>	−0.3 V to V <sub>DD</sub> + 0.3 V
Digital Inputs <sup>1</sup>	−0.3 V to 4.6 V or 10 mA, whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1ms, 10% duty cycle max)
Continuous Current, S or D	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP Package	
θ <sub>JA</sub> Thermal Impedance	206°C/W
θ <sub>JC</sub> Thermal Impedance	44°C/W
LFCSP Package	
θ <sub>JA</sub> Thermal Impedance (3-Layer Board)	61.1°C/W
IR Reflow, Peak Temperature <20 sec	235°C

<sup>1</sup> Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

**Table 5. Truth Table**

Logic	Switch A	Switch B
0	Off	On
1	On	Off

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# PIN CONFIGURATIONS

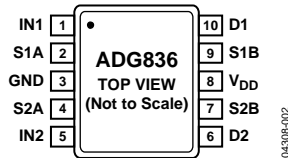


Figure 2. 10-Lead MSOP (RM-10)

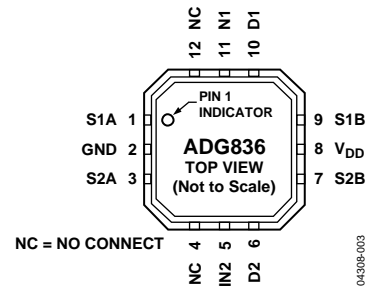


Figure 3. 12-Lead LFCSP (CP-12)

**Table 6. Terminology**

V <sub>DD</sub>	Most positive power supply potential.
I <sub>DD</sub>	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
V <sub>D</sub> (V <sub>S</sub> )	Analog voltage on terminals D, S.
R <sub>ON</sub>	Ohmic resistance between D and S.
R <sub>FLAT (ON)</sub>	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
ΔR <sub>ON</sub>	On resistance match between any two channels.
I <sub>S</sub> (OFF)	Source leakage current with the switch off.
I <sub>D</sub> (OFF)	Drain leakage current with the switch off.
I <sub>D</sub> , I <sub>S</sub> (ON)	Channel leakage current with the switch on.
V <sub>INL</sub>	Maximum input voltage for Logic 0.
V <sub>INH</sub>	Minimum input voltage for Logic 1.
I <sub>INL</sub> (I <sub>INH</sub> )	Input current of the digital input.
C <sub>S</sub> (OFF)	Off switch source capacitance. Measured with reference to ground.
C <sub>D</sub> (OFF)	Off switch drain capacitance. Measured with reference to ground.
C <sub>D</sub> , C <sub>S</sub> (ON)	On switch capacitance. Measured with reference to ground.
C <sub>IN</sub>	Digital input capacitance.
t <sub>ON</sub>	Delay time between the 50% and the 90% points of the digital input and switch on condition.
t <sub>OFF</sub>	Delay time between the 50% and the 90% points of the digital input and switch off condition.
t <sub>BBM</sub>	On or off time measured between the 80% points of both switches when switching from one to another.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.
Off Isolation	A measure of unwanted signal coupling through an off switch.
Crosstalk	A measure of unwanted signal, which is coupled through from one channel to another, as a result of parasitic capacitance.
-3 dB Bandwidth	The frequency at which the output is attenuated by 3 dB.
On Response	The frequency response of the on switch.
Insertion Loss	The loss due to the on resistance of the switch.
THD + N	The ratio of the harmonics amplitude plus noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

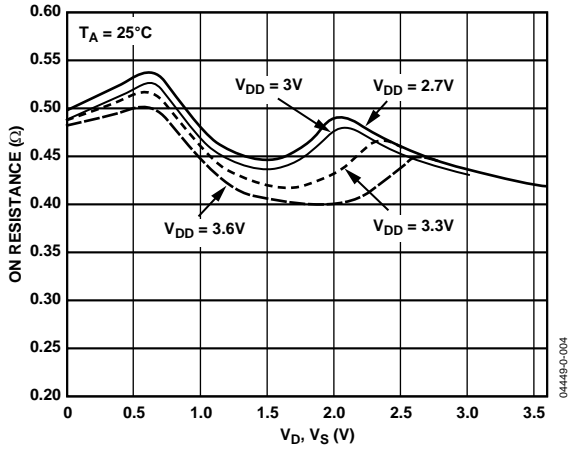


Figure 4. On Resistance vs.  $V_D$  ( $V_S$ )  $V_{DD} = 2.7$  to  $3.6$  V

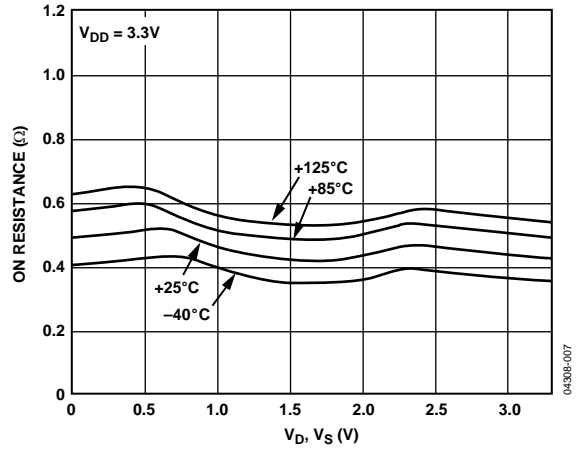


Figure 7. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperature,  $3.3$  V

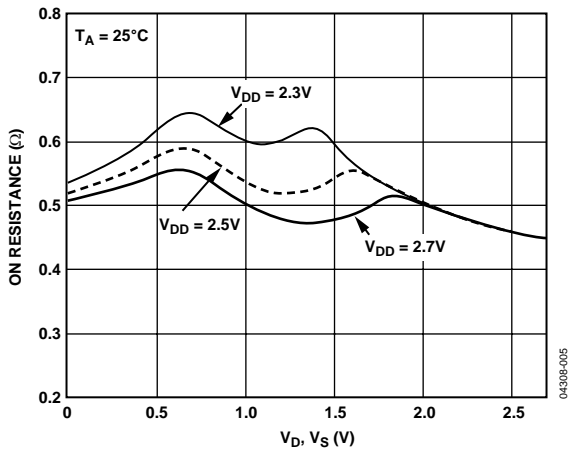


Figure 5. On Resistance vs.  $V_D$  ( $V_S$ )  $V_{DD} = 2.5$  V to  $0.2$  V

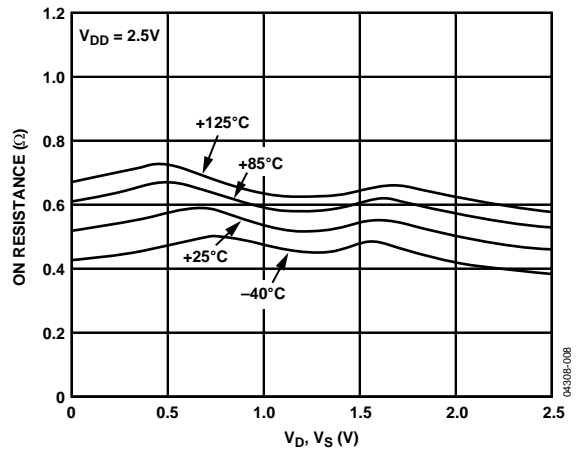


Figure 8. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperature,  $2.5$  V

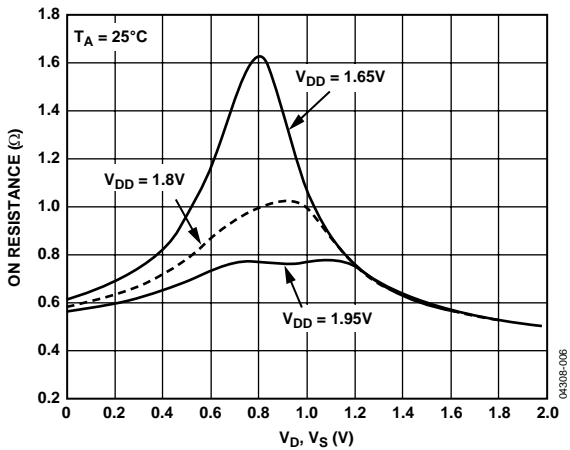


Figure 6. On Resistance vs.  $V_D$  ( $V_S$ )  $V_{DD} = 1.8 \pm 3.6$

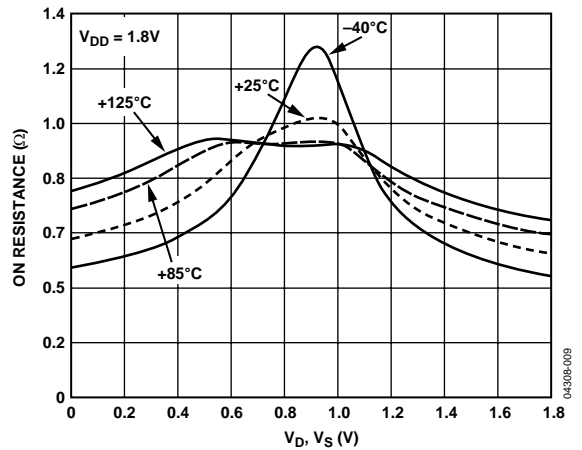


Figure 9. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperature,  $1.8$  V



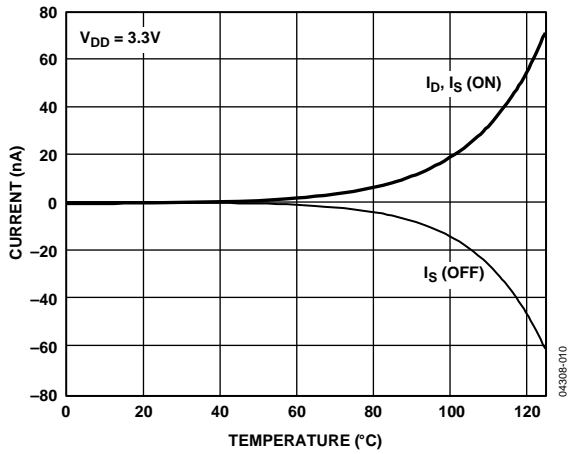


Figure 10. Leakage Current vs. Temperature, 3.3 V

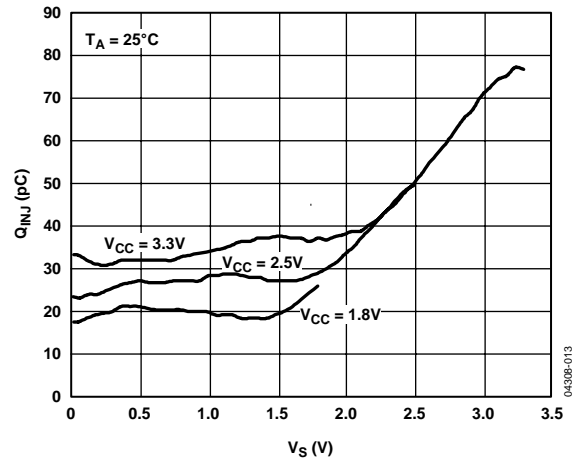


Figure 13. Charge Injection vs. Source Voltage

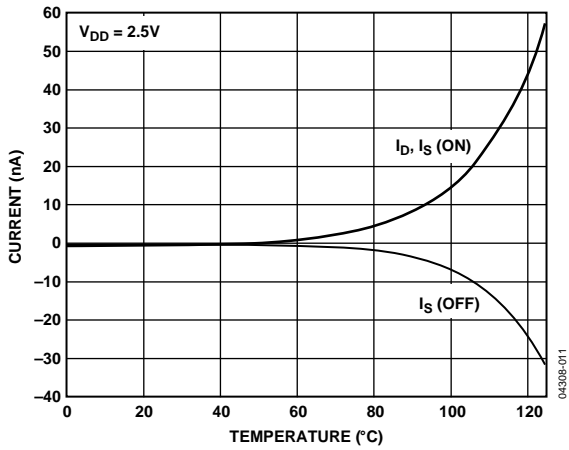


Figure 11. Leakage Current vs. Temperature, 2.5 V

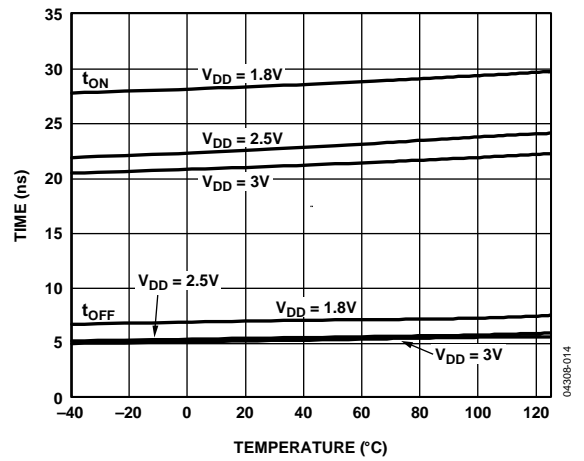


Figure 14.  $t_{ON}/t_{OFF}$  Times vs. Temperature

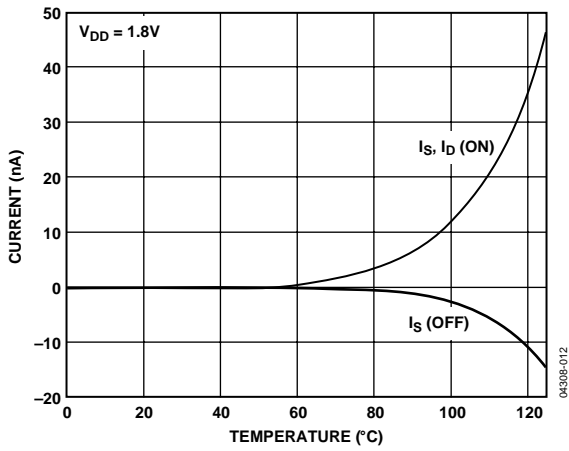


Figure 12. Leakage Current vs. Temperature, 1.8 V

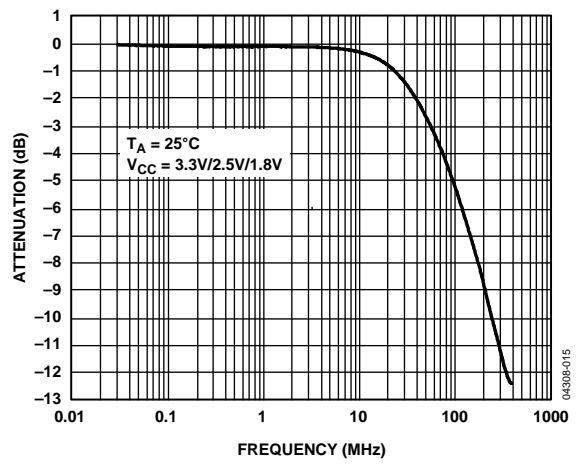


Figure 15. Bandwidth

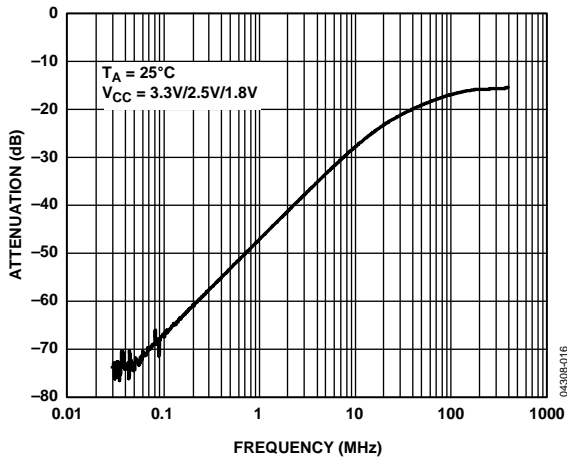


Figure 16. Off Isolation vs. Frequency

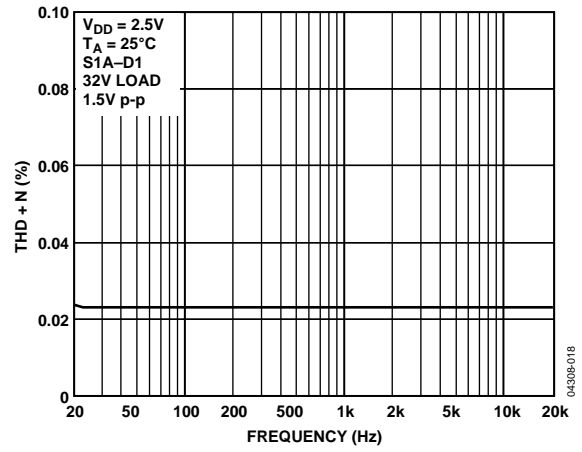


Figure 18. Total Harmonic Distortion + Noise

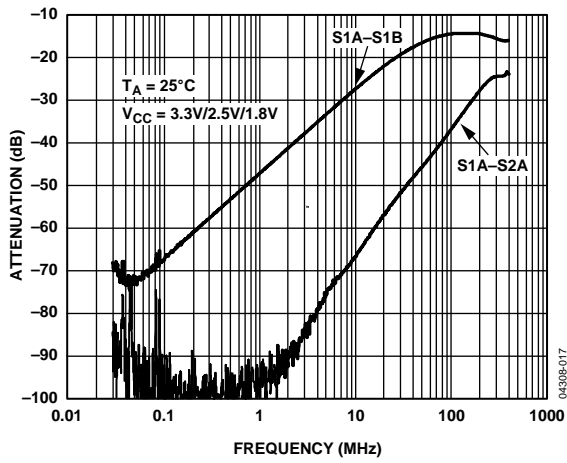
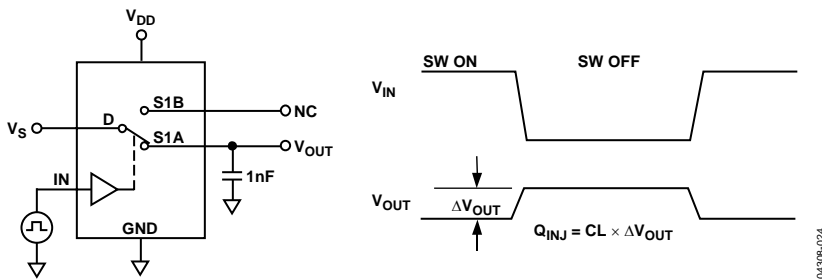
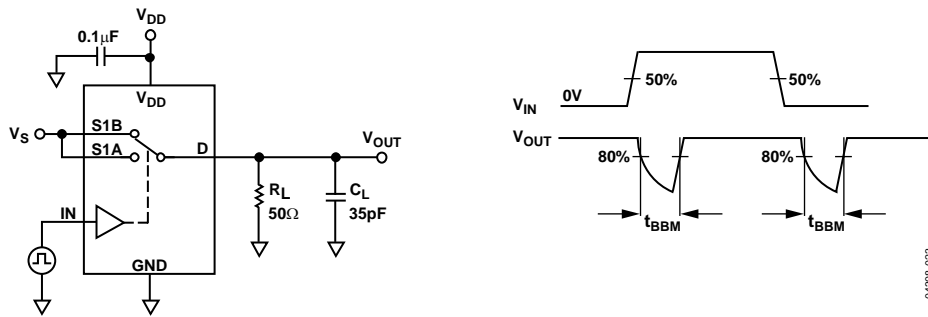
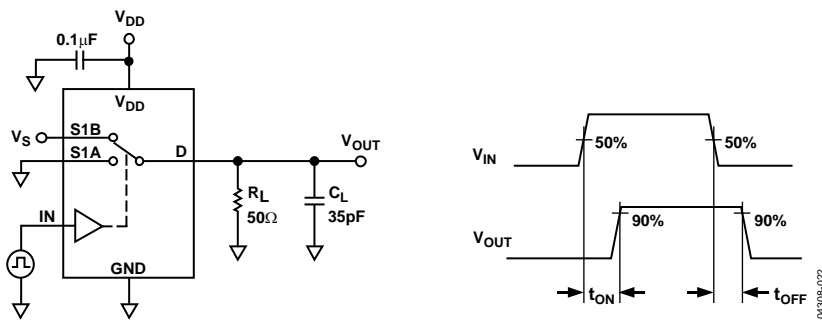
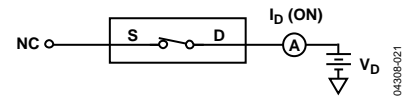
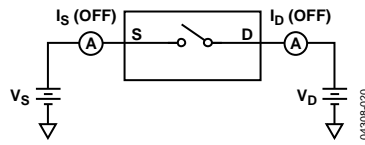
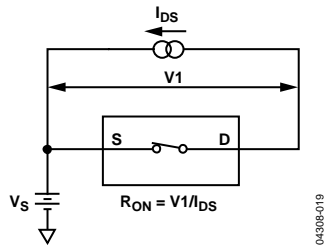


Figure 17. Crosstalk vs. Frequency

# TEST CIRCUITS



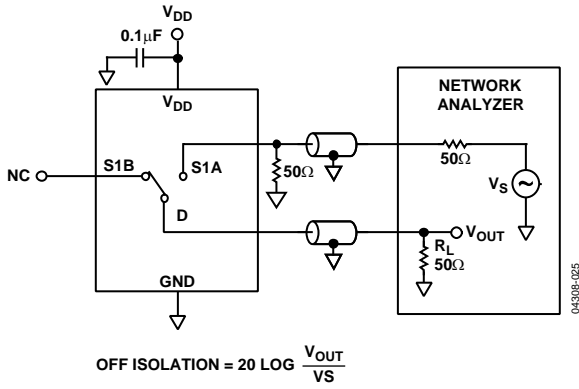


Figure 25. Off Isolation

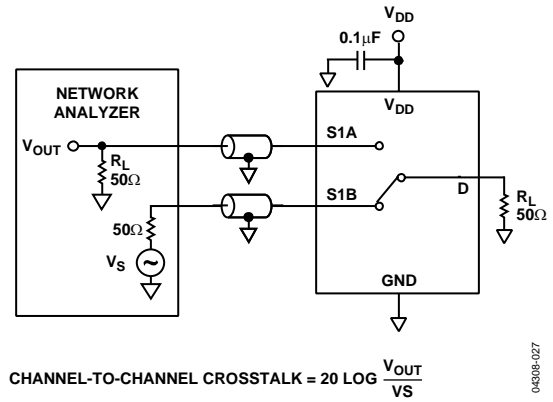


Figure 27. Channel-to-Channel Crosstalk (S1A-S1B)

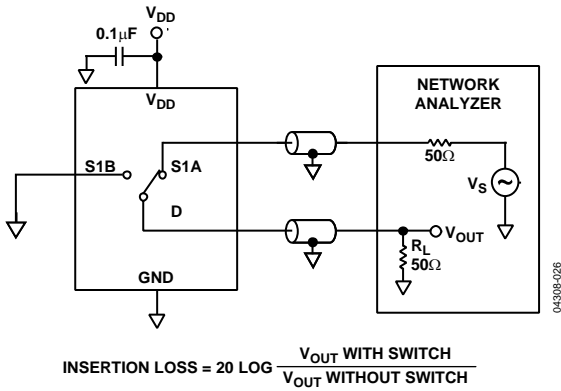


Figure 26. Bandwidth

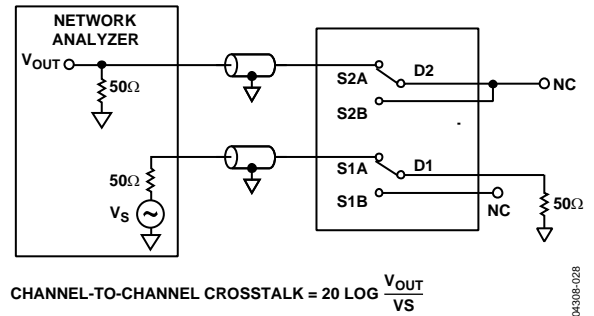
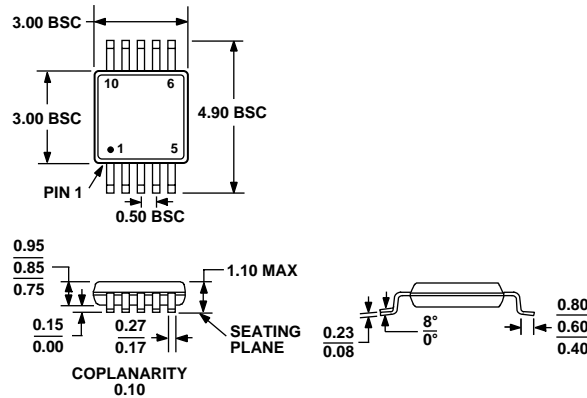


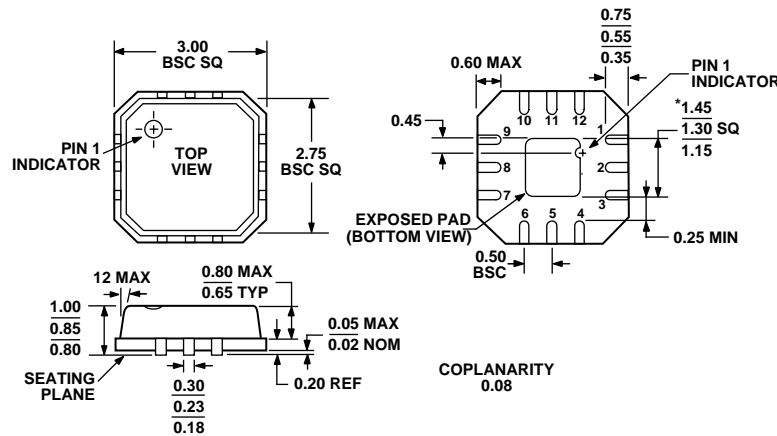
Figure 28. Channel-to-Channel Crosstalk (S1A-S2A)

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 29. 10-Lead Mini Small Outline Package [MSOP] (RM-10)  
Dimensions shown in millimeters



\*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1 EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 30. 12-Lead Lead Frame Chip Scale Package [LFCSP\_VQ] 3 x 3 mm Body, Very Thin Quad (CP-12-1)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding <sup>1</sup>
ADG836YRM	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRM-REEL	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRM-REEL7	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S9A
ADG836YRMZ <sup>2</sup>	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YRMZ-REEL <sup>2</sup>	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YRMZ-REEL7 <sup>2</sup>	-40°C to +125°C	Mini Small Outline Package (MSOP)	RM-10	S05
ADG836YCP-REEL	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	S9A
ADG836YCP-REEL7	-40°C to +125°C	Lead Frame Chip Scale Package (LFCSP_VQ)	CP-12-1	S9A

<sup>1</sup> Branding on this package is limited to three characters due to space constraints.

<sup>2</sup> Z = Pb-free part.

**ADG836**

**NOTES**

**NOTES**

**ADG836**

**NOTES**