CBTL04082A; CBTL04082B

3.3 V, 4 differential channel, 2 : 1 multiplexer/demultiplexer switch for PCI Express Gen2

Rev. 1 — 28 February 2011 **Product data sheet**

1. General description

CBTL04082A/B is an 8-to-4 bidirectional differential channel multiplexer/demultiplexer switch for PCI Express Generation 2 (Gen2) applications. The CBTL04082A/B can switch four differential signals to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimized the channel-to-channel skew as well as channel-to-channel crosstalk, as required by the high-speed serial interface. CBTL04082A/B allows expansion of existing high speed ports for extremely low power.

The devices’ pinouts are optimized to match different application layouts. CBTL04082A has input and output pins on the opposite of the package, and is suitable for edge connector(s) with different signal sources on the motherboard. CBTL04082B has outputs on both sides of the package, and the device can be placed between two connectors to multiplex differential signals from a controller. Please refer to Section 8 for layout examples.

2. Features and benefits

- 4 bidirectional differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching for PCIe Gen2 5 Gbit/s
- High bandwidth: 6 GHz at –3 dB
- Insertion loss:
  - –0.5 dB at 100 MHz
  - –1.2 dB at 2.5 GHz
- Low intra-pair skew: 5 ps typical
- Low inter-pair skew: 35 ps maximum
- Low crosstalk: –30 dB at 2.5 GHz
- Low off-state isolation: –25 dB at 2.5 GHz
- Low return loss: –20 dB at 2.5 GHz
- V_{DD} operating range: 3.3 V ± 10 %
- Dual shutdown pins for channel 0/1 and 2/3 independently to minimize power consumption
  - Standby current less than 1 μA
- ESD tolerance:
  - 8 kV HBM
  - 1 kV CDM
- HVQFN42 package

3. Applications

- Routing of high-speed differential signals with low signal attenuation
  - PCIe Gen2
  - DisplayPort 1.2
  - USB 3.0
  - SATA 6 Gbit/s

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBTL04082ABS	HVQFN42	plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 × 9 × 0.85 mm[1]	SOT1144-1
CBTL04082BBS	HVQFN42	plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 × 9 × 0.85 mm[1]	SOT1144-1

[1] Total height after printed-circuit board mounting = 1.0 mm (maximum).

5. Functional diagram

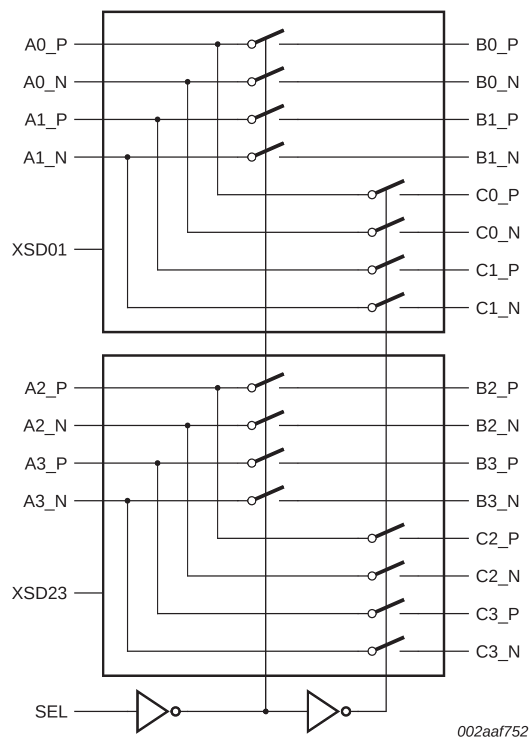
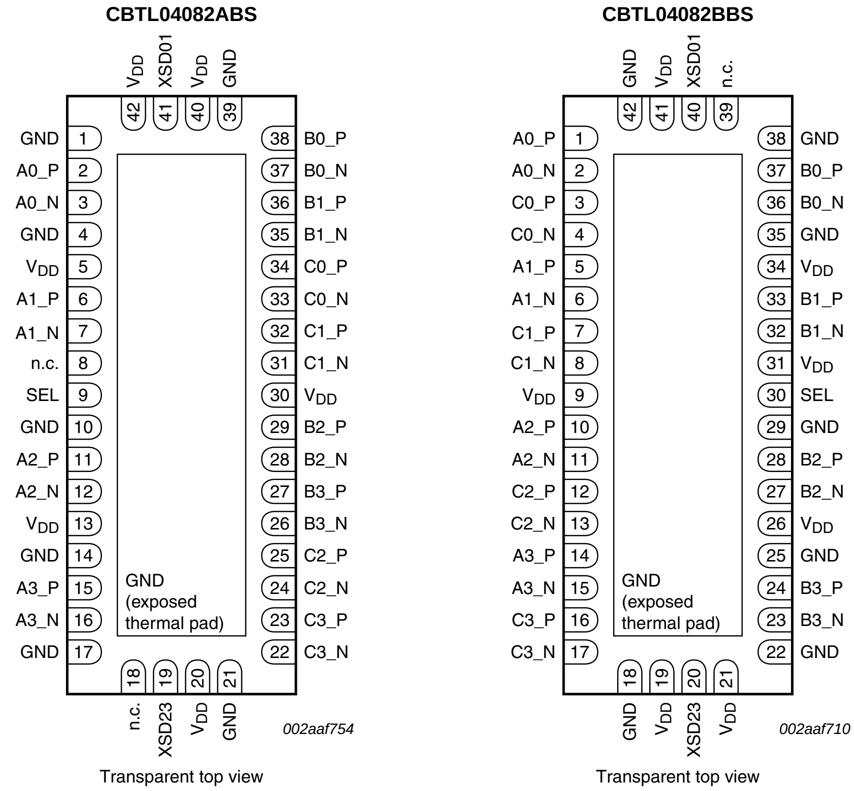


Fig 1. Functional diagram of CBTL04082A; CBTL04082B

6. Pinning information

6.1 Pinning



a. CBTL04082A

b. CBTL04082B

Fig 2. Pin configuration for HVQFN42

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	CBTL04082A	CBTL04082B		
A0_P	2	1	I/O	channel 0, port A differential signal input/output
A0_N	3	2	I/O	
A1_P	6	5	I/O	channel 1, port A differential signal input/output
A1_N	7	6	I/O	
A2_P	11	10	I/O	channel 2, port A differential signal input/output
A2_N	12	11	I/O	
A3_P	15	14	I/O	channel 3, port A differential signal input/output
A3_N	16	15	I/O	

Table 2. Pin description *…continued*

Symbol	Pin		Type	Description
	CBTL04082A	CBTL04082B		
B0_P	38	37	I/O	channel 0, port B differential signal input/output
B0_N	37	36	I/O	
B1_P	36	33	I/O	channel 1, port B differential signal input/output
B1_N	35	32	I/O	
B2_P	29	28	I/O	channel 2, port B differential signal input/output
B2_N	28	27	I/O	
B3_P	27	24	I/O	channel 3, port B differential signal input/output
B3_N	26	23	I/O	
C0_P	34	3	I/O	channel 0, port C differential signal input/output
C0_N	33	4	I/O	
C1_P	32	7	I/O	channel 1, port C differential signal input/output
C1_N	31	8	I/O	
C2_P	25	12	I/O	channel 2, port C differential signal input/output
C2_N	24	13	I/O	
C3_P	23	16	I/O	channel 3, port C differential signal input/output
C3_N	22	17	I/O	
SEL	9	30	CMOS single-ended input	operation mode select SEL = LOW: A ↔ B SEL = HIGH: A ↔ C
XSD01	41	40	CMOS single-ended input	Shutdown pin; should be driven LOW or connected to GND for normal operation. When HIGH, channel 0 and channel 1 are switched off (non-conducting high-impedance state), and supply current consumption is minimized.
XSD23	19	20	CMOS single-ended input	Shutdown pin; should be driven LOW or connected to GND for normal operation. When HIGH, channel 2 and channel 3 are switched off (non-conducting high-impedance state), and supply current consumption is minimized.
V_{DD}	5, 13, 20, 30, 40, 42	9, 19, 21, 26, 31, 34, 41	power	positive supply voltage, 3.3 V (±10 %)
GND[1]	1, 4, 10, 14, 17, 21, 39, center pad	18, 22, 25, 29, 35, 38, 42, center pad	power	supply ground
n.c.	8, 18	39	-	not connected; these pins can be connected to any signal externally

[1] HVQFN42 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 "Functional diagram of CBTL04082A; CBTL04082B".

7.1 Function selection

Table 3. Function selection

X = Don't care.

XSD01	XSD23	SEL	Function
HIGH	-	X	An, Bn and Cn pins are high-Z, n = 0, 1
LOW	-	LOW	An to Bn or vice versa, n = 0, 1
LOW	-	HIGH	An to Cn or vice versa, n = 0, 1
-	HIGH	X	An, Bn and Cn pins are high-Z, n = 2, 3
-	LOW	LOW	An to Bn or vice versa, n = 2, 3
-	LOW	HIGH	An to Cn or vice versa, n = 2, 3

7.2 Shutdown function

The CBTL04082A/B provides a shutdown function to minimize power consumption when the application is not active, but power to the CBTL04082A/B is provided. Pin XSD01 and XSD23 (active HIGH) places channel 0/1 and 2/3 (respectively) in high-impedance state (non-conducting) while reducing current consumption to near-zero.

Table 4. Shutdown function

XSD01	XSD23	Channel 0	Channel 1	Channel 2	Channel 3
HIGH	-	high-Z	high-Z	-	-
LOW	-	active	active	-	-
-	HIGH	-	-	high-Z	high-Z
-	LOW	-	-	active	active

8. Application design-in information

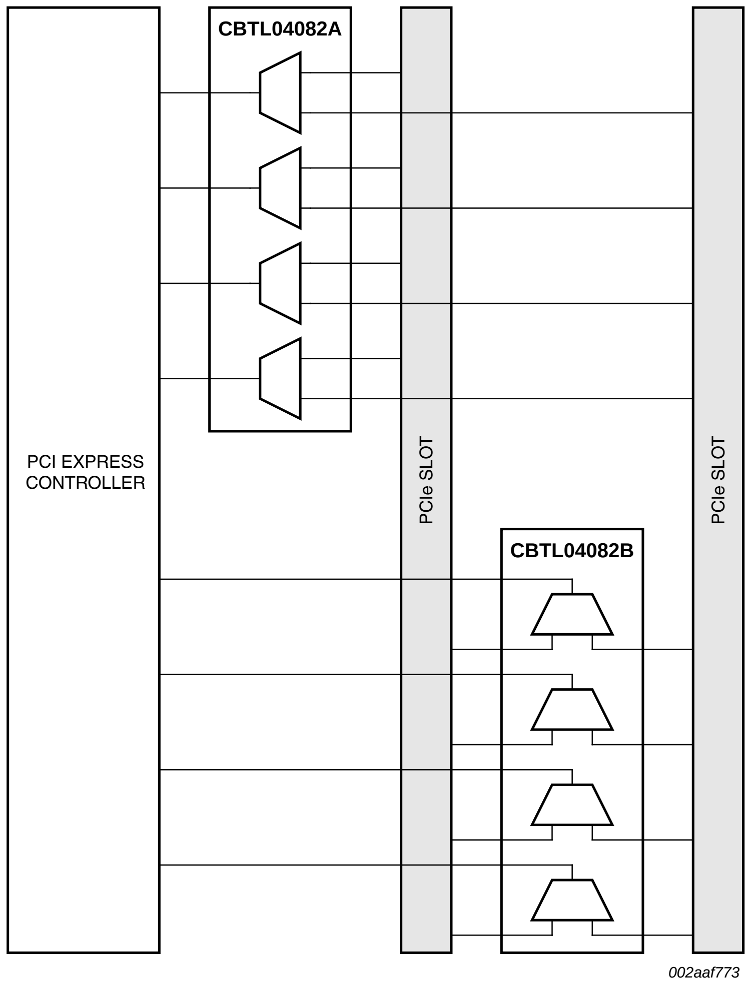


Fig 3. A/B pinout difference (layout)

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.6	V
T_{case}	case temperature		–40	+85	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	8000	V
		CDM [2]	-	1000	V

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	3.3	3.6	V
V_I	input voltage		-	-	V_{DD}	V
T_{amb}	ambient temperature	operating in free air	–40	-	+85	°C

11. Static characteristics

Table 7. Static characteristics

V_{DD} = 3.3 V ± 10 %; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_{DD}	supply current	V_{DD} = max.; V_I = GND or V_{DD}; XSD01 = XSD23 = LOW	-	2.7	5	mA
I_{stb}	standby current	V_{DD} = max.; V_I = GND or V_{DD}; XSD01 = XSD23 = HIGH	-	-	1	µA
I_{IH}	HIGH-level input current	V_{DD} = max.; V_I = V_{DD}	-	-	±5 [2]	µA
I_{IL}	LOW-level input current	V_{DD} = max.; V_I = GND	-	-	±5 [2]	µA
V_{IH}	HIGH-level input voltage	SEL, XSD01, XSD23 pins	$0.65V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	SEL, XSD01, XSD23 pins	-	-	$0.35V_{DD}$	V
V_I	input voltage	differential pins	-	-	2.4	V
		SEL, XSD01, XSD23 pins	-	-	V_{DD}	V
V_{IC}	common-mode input voltage		0	-	2.0	V
V_{ID}	differential input voltage	peak-to-peak	-	-	1.6	V
R_{on}	ON-state resistance	V_{DD} = 3.3 V; V_I = 2 V; I_I = 19 mA	-	6	-	Ω

[1] Typical values are at V_{DD} = 3.3 V, T_{amb} = 25 °C, and maximum loading.

[2] Input leakage current is ±50 µA if differential pairs are pulled to HIGH and LOW.

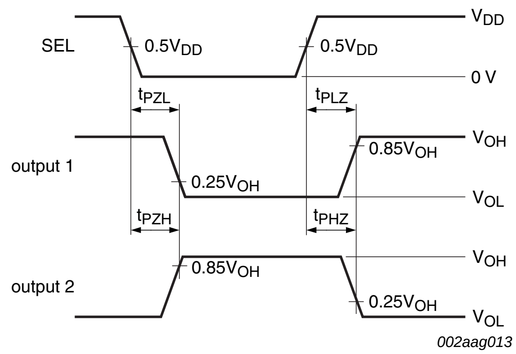
12. Dynamic characteristics

Table 8. Dynamic characteristics

V_{DD} = 3.3 V ± 10 %; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
DDIL	differential insertion loss	channel is OFF				
		f = 100 MHz	-	–50	-	dB
		f = 2.5 GHz	-	–25	-	dB
		channel is ON				
		f = 100 MHz	-	–0.5	-	dB
		f = 2.5 GHz	-	–1.2	-	dB
DDNEXT	differential near-end crosstalk	adjacent channels are ON				
		f = 100 MHz	-	–50	-	dB
		f = 2.5 GHz	-	–30	-	dB
B_{-3dB}	–3 dB bandwidth		-	6.0	-	GHz
DDRL	differential return loss	f = 100 MHz	-	–25	-	dB
		f = 2.5 GHz	-	–20	-	dB
t_{PD}	propagation delay	from Port A to Port B, or Port A to Port C, or vice versa	-	80	-	ps
Switching characteristics						
$t_{startup}$	start-up time	supply voltage valid or XSD01/XSD23 going LOW to channel specified operating characteristics	-	-	10	ms
t_{PZH}	OFF-state to HIGH propagation delay		-	-	300	ns
t_{PZL}	OFF-state to LOW propagation delay		-	-	70	ns
t_{PHZ}	HIGH to OFF-state propagation delay		-	-	50	ns
t_{PLZ}	LOW to OFF-state propagation delay		-	-	50	ns
$t_{sk(dif)}$	differential skew time	intra-pair	-	5	-	ps
t_{sk}	skew time	inter-pair	-	-	35	ps

[1] Typical values are at V_{DD} = 3.3 V; T_{amb} = 25 °C, and maximum loading.



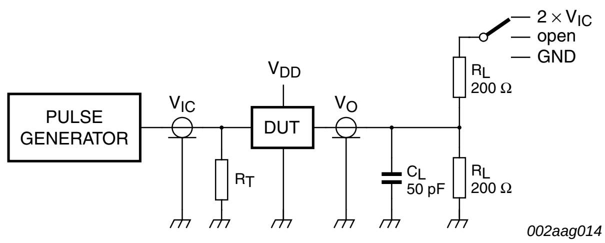
Output 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

Output 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

The outputs are measured one at a time with one transition per measurement.

Fig 4. Voltage waveforms for enable and disable times

13. Test information



C_L = load capacitance; includes jig and probe capacitance.

R_T = termination resistance; should be equal to Z_o of the pulse generator.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 5 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

Fig 5. Test circuitry for switching times

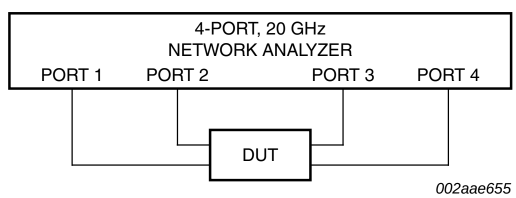


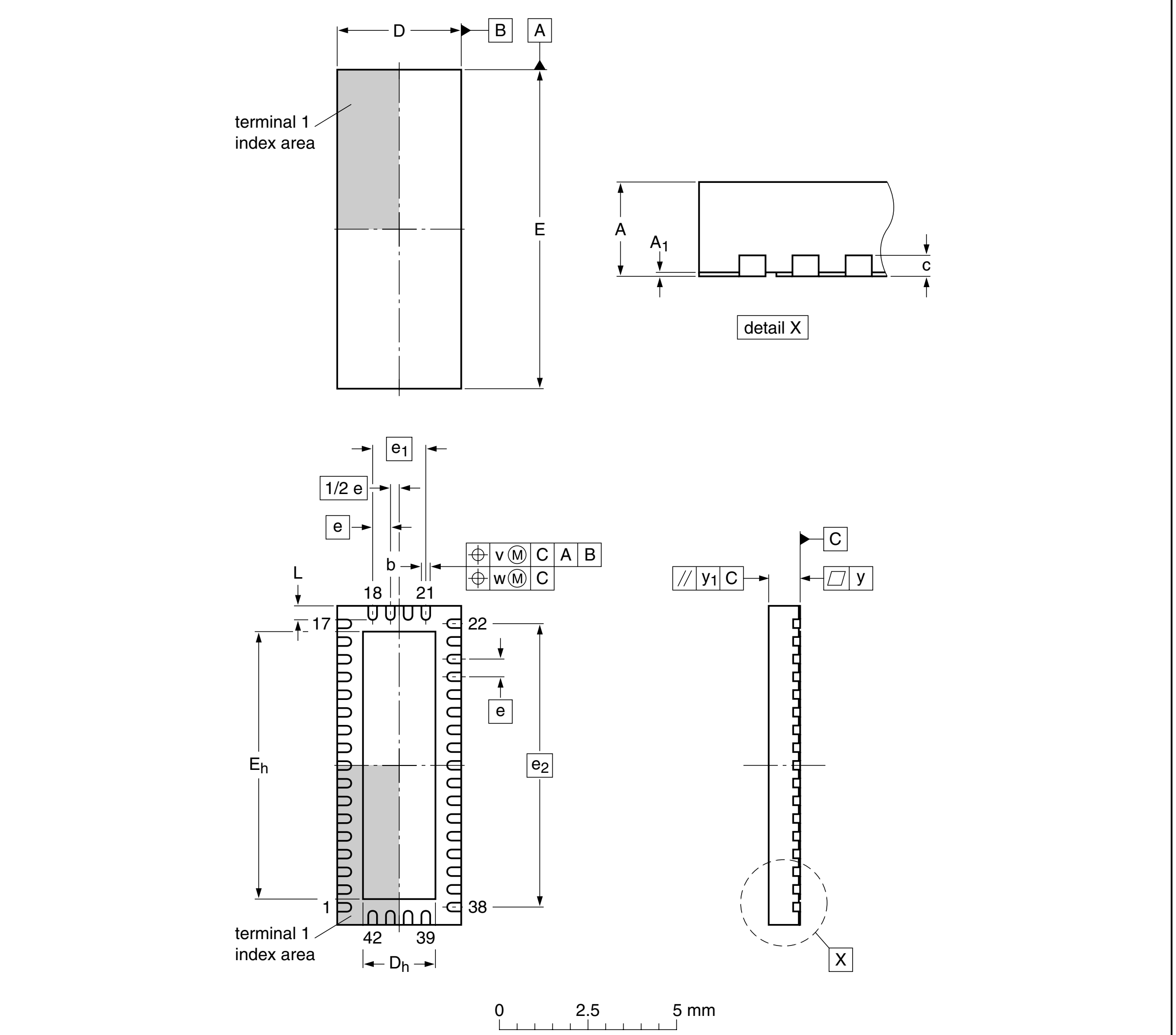
Fig 6. Test circuit

Table 9. Test data

Test	Load		Switch
	C_L	R_L	
t_{PLZ}, t_{PZL} (output on B side)	50 pF	200 Ω	2 × V_{IC}
t_{PHZ}, t_{PZH} (output on B side)	50 pF	200 Ω	GND
t_{PD}	-	200 Ω	open

14. Package outline

HVQFN42: plastic thermal enhanced very thin quad flat package; no leads; 42 terminals; body 3.5 x 9 x 0.85 mm **SOT1144-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30		3.6	2.30	9.1	7.70				0.5				
mm	nom	0.85	0.02	0.25	0.2	3.5	2.05	9.0	7.55	0.5	1.5	8.0	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.20		3.4	1.90	8.9	7.40				0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1144-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1144-1	- - -	- - -	- - -			~~09-08-26~~ 09-08-28

Fig 7. Package outline SOT1144-1 (HVQFN42)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

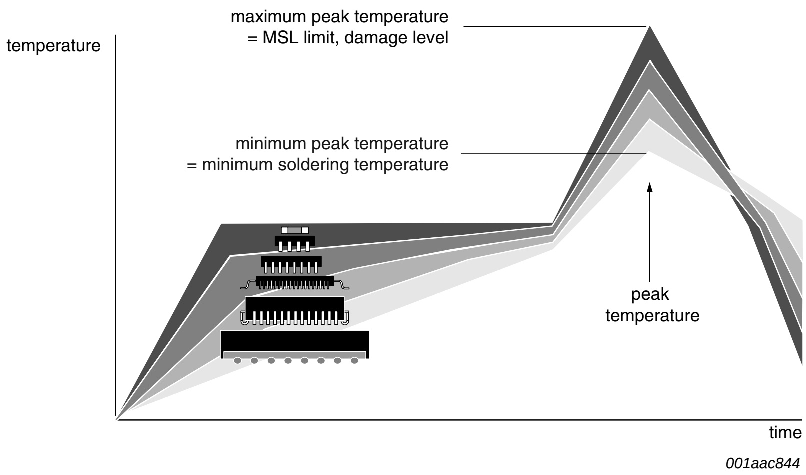
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
PCI	Peripheral Component Interconnect
PCIe	PCI express
PRR	Pulse Repetition Rate
SATA	Serial Advanced Technology Attachment
USB	Universal Serial Bus

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTL04082A_CBTL04082B v.1	20110228	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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20. Contents

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