CMOS 1.8 V to 5.5 V, 2.5 Ω SPDT Switch/2:1 Mux in Tiny SC70 Package

ADG779

FEATURES

1.8 V to 5.5 V single supply
2.5 Ω on resistance
0.75 Ω on-resistance flatness
−3 dB bandwidth >200 MHz
Rail-to-rail operation
6-lead SC70 package
Fast switching times
t_{ON} 20 ns
t_{OFF} 6 ns
Typical power consumption (<0.01 μW)
TTL/CMOS compatible

APPLICATIONS

Battery-powered systems
Communication systems
Sample hold systems
Audio signal routing
Video switching
Mechanical reed relay replacements

FUNCTIONAL BLOCK DIAGRAM

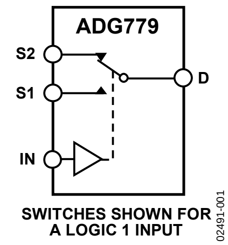

Figure 1.

GENERAL DESCRIPTION

The ADG779 is a monolithic CMOS SPDT (single-pole, double-throw) switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

The ADG779 operates from a single supply range of 1.8 V to 5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices, Inc.

Each switch of the ADG779 conducts equally well in both directions when on. The ADG779 exhibits break-before-make switching action.

Because of the advanced submicron process, −3 dB bandwidth of greater than 200 MHz can be achieved.

The ADG779 is available in a 6-lead SC70 package.

PRODUCT HIGHLIGHTS

1. Tiny 6-Lead SC70 Package.
2. 1.8 V to 5.5 V Single-Supply Operation. The ADG779 offers high performance, including low on resistance and fast switching times, and is fully specified and guaranteed with 3 V and 5 V supply rails.
3. Very Low R_{ON} (5 Ω max at 5 V, 10 Ω max at 3 V). At 1.8 V operation, R_{ON} is typically 40 Ω over the temperature range.
4. On-Resistance Flatness ($R_{FLAT (ON)}$) (0.75 Ω typ).
5. −3 dB Bandwidth > 200 MHz.
6. Low Power Dissipation. CMOS construction ensures low power dissipation.
7. 14 ns Switching Times.

Rev. A

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REVISION HISTORY

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7/01—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5 V ± 10%, GND = 0 V[1]

Table 1.

Parameter	B Version 25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA, see Figure 12
	5	6	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	0.75		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		1.2	Ω max	
LEAKAGE CURRENTS[2]				V_{DD} = 5.5 V
Source Off Leakage I_S (Off)	±0.01	±0.05	nA typ	V_S = 4.5 V/1 V, V_D = 1 V/4.5 V, see Figure 13
Channel On Leakage I_D, I_S (On)	±0.01	±0.05	nA typ	V_S = V_D = 1 V, or V_S = V_D = 4.5 V, see Figure 14
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	14		ns typ	R_L = 300 Ω, C_L = 35 pF
		20	ns max	V_S = 3 V, see Figure 15
t_{OFF}	3		ns typ	R_L = 300 Ω, C_L = 35 pF
		6	ns max	V_S = 3 V, see Figure 15
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 3 V, see Figure 16
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 17
Channel-to-Channel Crosstalk	−62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 18
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 19
C_S (Off)	7		pF typ	f = 1 MHz
C_D, C_S (On)	27		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
				Digital Inputs = 0 V or 5 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

[1] Temperature range is B Version, −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V[1]

Table 2.

Parameter	B Version 25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	
On Resistance (R_{ON})	6	7	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA, see Figure 12
		10	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.1		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
		0.8	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	2.5		Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS[2]				V_{DD} = 3.3 V
Source Off Leakage I_S (Off)	±0.01	±0.05	nA typ	V_S = 3 V/1 V, V_D = 1 V/3 V, see Figure 13
Channel On Leakage I_D, I_S (On)	±0.01	±0.05	nA typ	V_S = V_D = 1 V, or V_S = V_D = 3 V, see Figure 14
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	16		ns typ	R_L = 300 Ω, C_L = 35 pF
		24	ns max	V_S = 2 V, see Figure 15
t_{OFF}	4		ns typ	R_L = 300 Ω, C_L = 35 pF
		7	ns max	V_S = 2 V, see Figure 15
Break-Before-Make Time Delay, t_D	8		ns typ	R_L = 300 Ω, C_L = 35 pF
		1	ns min	V_{S1} = V_{S2} = 2 V, see Figure 16
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−87		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 17
Channel-to-Channel Crosstalk	−62		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz
	−82		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 18
Bandwidth −3 dB	200		MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 19
C_S (Off)	7		pF typ	f = 1 MHz
C_D, C_S (On)	27		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 3.3 V
				Digital Inputs = 0 V or 3 V
I_{DD}	0.001		μA typ	
		1.0	μA max	

[1] Temperature range is B Version, −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SC70 Package, Power Dissipation	315 mW
θ_{JA} Thermal Impedance	332°C/W
θ_{JC} Thermal Impedance	120°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
Reflow Soldering (Pb-free)	
Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	10 sec to 40 sec

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Truth Table

ADG779 IN	Switch S1	Switch S2
0	On	Off
1	Off	On

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

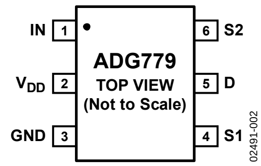

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN	Logic Control Input.
2	V_{DD}	Most Positive Power Supply Potential.
3	GND	Ground (0 V) Reference.
4	S1	Source Terminal. Can be an input or an output.
5	D	Drain Terminal. Can be an input or an output.
6	S2	Source Terminal. Can be an input or an output.

TERMINOLOGY

V_{DD}
Most positive power supply potential.

I_{DD}
Positive supply current.

GND
Ground (0 V) reference.

S
Source terminal. Can be an input or an output.

D
Drain terminal. Can be an input or an output.

IN
Logic control input.

V_D (V_S)
Analog voltage on drain (D) and source (S) terminals.

R_{ON}
Ohmic resistance between the D and S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On-resistance mismatch between any two channels.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (Off)
Off switch source capacitance. Measured with reference to ground.

C_D (Off)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another because of parasitic capacitance.

−3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of harmonic amplitudes plus noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

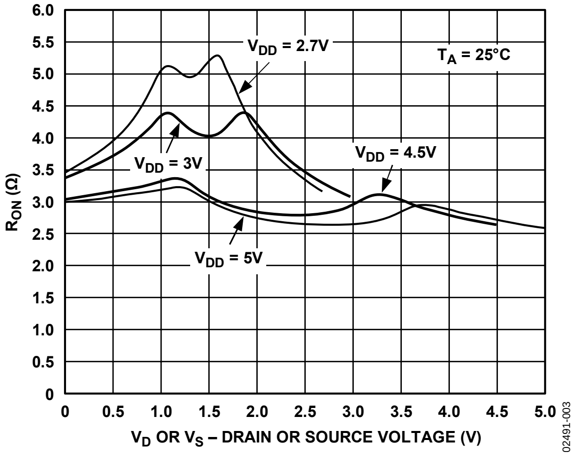

Figure 3. On Resistance as a Function of V_D (V_S) Single Supplies

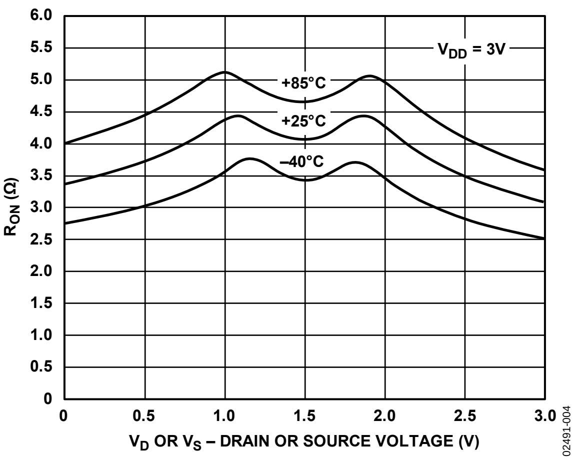

Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 3 V

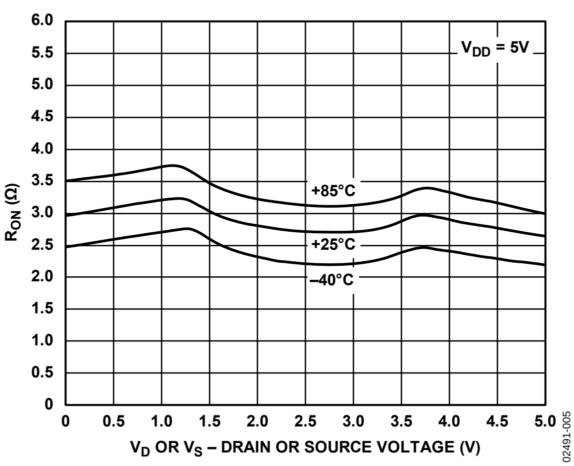

Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures V_{DD} = 5 V

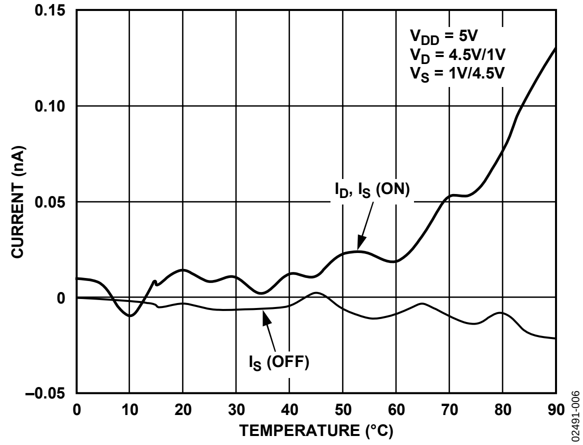

Figure 6. Leakage Currents as a Function of Temperature

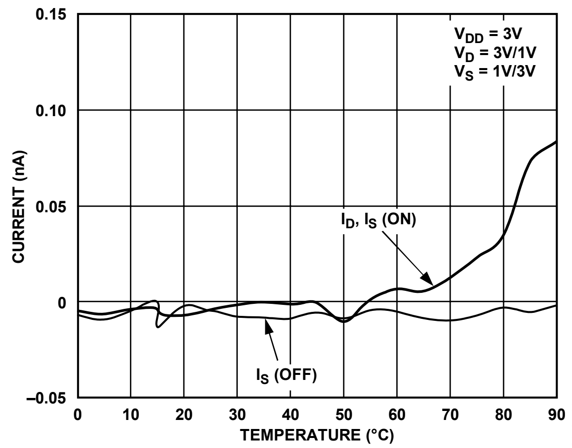

Figure 7. Leakage Currents as a Function of Temperature

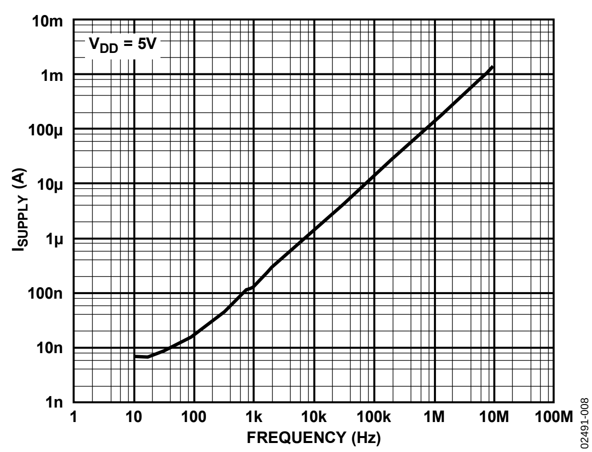

Figure 8. Supply Current vs. Input Switching Frequency

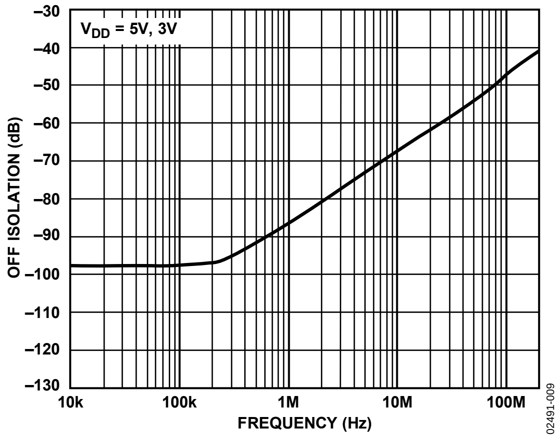

Figure 9. Off Isolation vs. Frequency

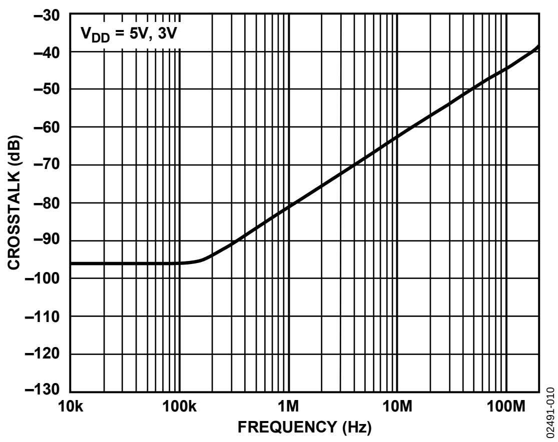

Figure 10. Crosstalk vs. Frequency

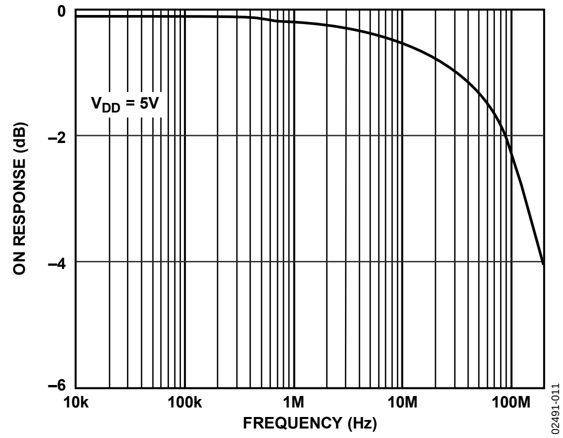

Figure 11. On Response vs. Frequency

TEST CIRCUITS

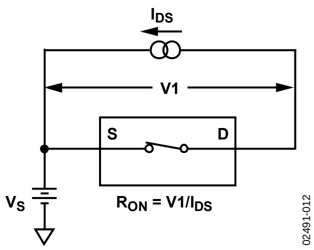

Figure 12. On Resistance

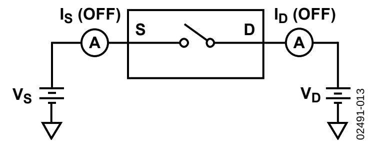

Figure 13. Off Leakage

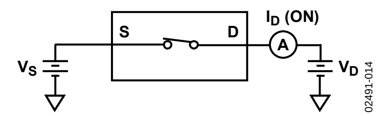

Figure 14. On Leakage

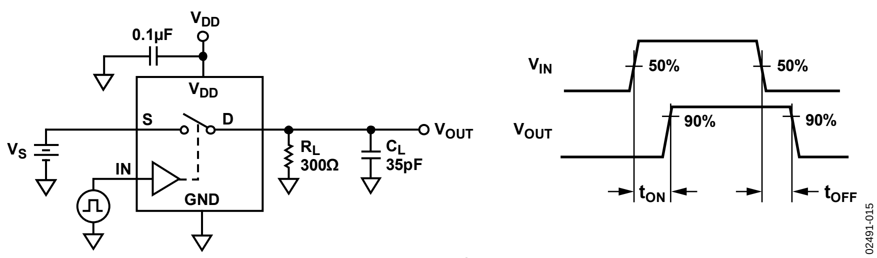

Figure 15. Switching Times

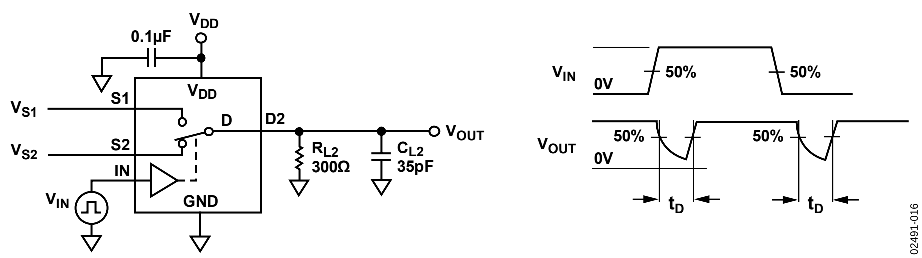

Figure 16. Break-Before-Make Time Delay, t_D

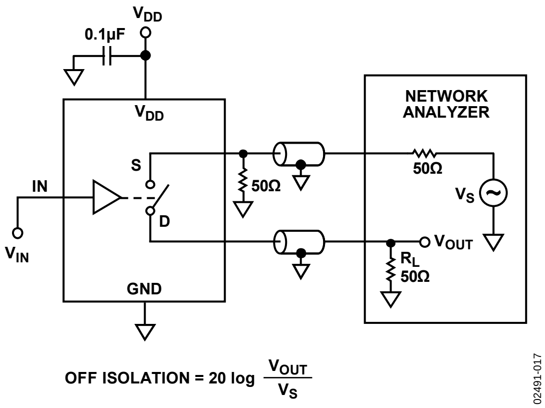

Figure 17. Off Isolation

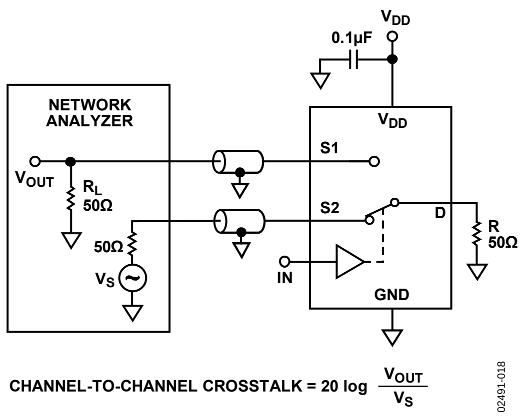

Figure 18. Channel-to-Channel Crosstalk

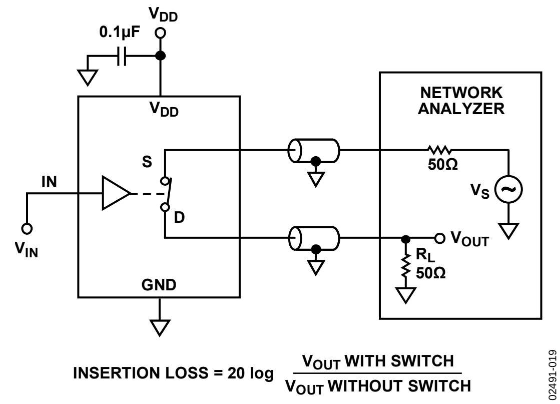

Figure 19. Bandwidth

OUTLINE DIMENSIONS

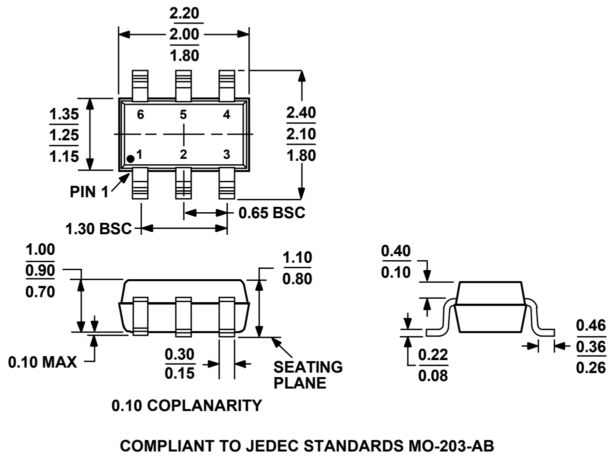

Figure 20. 6-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding[1]
ADG779BKS-R2	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SKB
ADG779BKS-REEL	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SKB
ADG779BKS-REEL7	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	SKB
ADG779BKSZ-R2[2]	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	S0M
ADG779BKSZ-REEL[2]	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	S0M
ADG779BKSZ-REEL7[2]	–40°C to +85°C	6-Lead Thin Shrink Small Outline Transistor Package (SC70)	KS-6	S0M

[1] Brand on these packages is limited to three characters due to space constraints.
[2] Z = Pb-free part.

C02491–0–10/05(A)