# ANALOG DEVICES

# CMOS
# Low Voltage 4 Ω Quad SPST Switches

# ADG711/ADG712/ADG713

## FEATURES
**1.8 V to 5.5 V Single Supply**
**Low On Resistance (2.5 Ω Typ)**
**Low On Resistance Flatness**
**–3 dB Bandwidth > 200 MHz**
**Rail-to-Rail Operation**
**16-Lead TSSOP and SOIC Packages**
**Fast Switching Times**
    $t_{ON}$  16 ns
    $t_{OFF}$  10 ns
**Typical Power Consumption (< 0.01 μW)**
**TTL/CMOS Compatible**

## APPLICATIONS
**USB 1.1 Signal Switching Circuits**
**Cell Phones**
**PDAs**
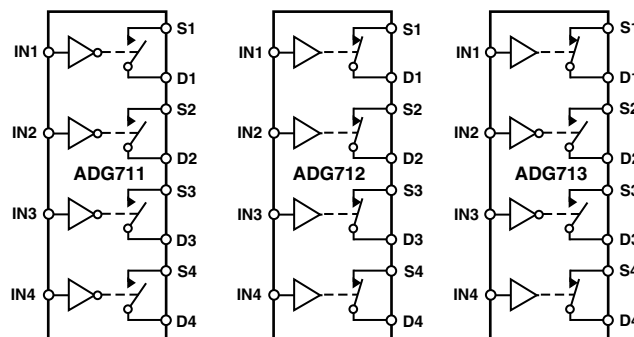**Battery-Powered Systems**
**Communication Systems**
**Sample Hold Systems**
**Audio Signal Routing**
**Video Switching**
**Mechanical Reed Relay Replacement**

## FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

## GENERAL DESCRIPTION
The ADG711, ADG712, and ADG713 are monolithic CMOS devices containing four independently selectable switches. These switches are designed on an advanced submicron process that provides low power dissipation yet gives high switching speed, low on resistance, low leakage currents, and high bandwidth.

They are designed to operate from a single 1.8 V to 5.5 V supply, making them ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices. Fast switching times and high bandwidth make the parts suitable for switching USB 1.1 data signals and video signals.

The ADG711, ADG712, and ADG713 contain four independent single-pole/single-throw (SPST) switches. The ADG711 and ADG712 differ only in that the digital control logic is inverted. The ADG711 switches are turned on with a logic low on the appropriate control input, while a logic high is required to turn on the switches of the ADG712. The ADG713 contains two switches whose digital control logic is similar to the ADG711, while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON. The ADG713 exhibits break-before-make switching action.

The ADG711/ADG712/ADG713 are available in 16-lead TSSOP and 16-lead SOIC packages.

## PRODUCT HIGHLIGHTS
1. 1.8 V to 5.5 V Single-Supply Operation.
   The ADG711, ADG712, and ADG713 offer high performance and are fully specified and guaranteed with 3 V and 5 V supply rails.

2. Very Low $R_{ON}$ (4.5 Ω max at 5 V, 8 Ω max at 3 V). At supply voltage of 1.8 V, $R_{ON}$ is typically 35 Ω over the temperature range.

3. Low On Resistance Flatness.

4. –3 dB Bandwidth >200 MHz.

5. Low Power Dissipation.
   CMOS construction ensures low power dissipation.

6. Fast $t_{ON}/t_{OFF}$.

7. Break-Before-Make Switching.
   This prevents channel shorting when the switches are configured as a multiplexer (ADG713 only).

8. 16-Lead TSSOP and 16-Lead SOIC Packages.

REV. A

| Parameter | B Version +25°C | −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| **ANALOG SWITCH** | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 2.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA; |
| | 4 | 4.5 | Ω max | Test Circuit 1 |
| On Resistance Match Between | | 0.05 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA |
| Channels ($\Delta R_{ON}$) | | 0.3 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA |
| | | 1.0 | Ω max | |
| **LEAKAGE CURRENTS** | | | | $V_{DD}$ = +5.5 V; |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 4.5 V/1 V, $V_D$ = 1 V/4.5 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.01 | | nA typ | $V_S$ = 4.5 V/1 V, $V_D$ = 1 V/4.5 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 2 |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_S$ = $V_D$ = 1 V, or 4.5 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 3 |
| **DIGITAL INPUTS** | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | µA max | |
| **DYNAMIC CHARACTERISTICS[2]** | | | | |
| $t_{ON}$ | 11 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| | | 16 | ns max | $V_S$ = 3 V; Test Circuit 4 |
| $t_{OFF}$ | 6 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| | | 10 | ns max | $V_S$ = 3 V; Test Circuit 4 |
| Break-Before-Make Time Delay, $t_D$ | 6 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| (ADG713 Only) | | 1 | ns min | $V_{S1}$ = $V_{S2}$ = 3 V; Test Circuit 5 |
| Charge Injection | 3 | | pC typ | $V_S$ = 2 V; $R_S$ = 0 Ω, $C_L$ = 1 nF; Test Circuit 6 |
| Off Isolation | −58 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −78 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Test Circuit 7 |
| Channel-to-Channel Crosstalk | −90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; Test Circuit 8 |
| Bandwidth −3 dB | 200 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Test Circuit 9 |
| $C_S$ (OFF) | 10 | | pF typ | |
| $C_D$ (OFF) | 10 | | pF typ | |
| $C_D$, $C_S$ (ON) | 22 | | pF typ | |
| **POWER REQUIREMENTS** | | | | $V_{DD}$ = +5.5 V |
| $I_{DD}$ | 0.001 | | µA typ | Digital Inputs = 0 V or 5 V |
| | | 1.0 | µA max | |

NOTES
[1]Temperature range: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

REV. A

# SPECIFICATIONS[1] ($V_{DD}$ = +3 V ± 10%, GND = 0 V. All specifications −40°C to +85°C unless otherwise noted.)

| Parameter | B Version +25°C | −40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 5 | 5.5 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA; |
| | | 8 | Ω max | Test Circuit 1 |
| On Resistance Match Between | 0.1 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA |
| Channels ($\Delta R_{ON}$) | | 0.3 | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | | 2.5 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = −10 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = +3.3 V; |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 2 |
| Drain OFF Leakage $I_D$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 2 |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_S$ = $V_D$ = 1 V, or 3 V; |
| | ±0.1 | ±0.2 | nA max | Test Circuit 3 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.4 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | ±0.1 | µA max | |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{ON}$ | 13 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| | | 20 | ns max | $V_S$ = 2 V; Test Circuit 4 |
| $t_{OFF}$ | 7 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| | | 12 | ns max | $V_S$ = 2 V; Test Circuit 4 |
| Break-Before-Make Time Delay, $t_D$ | 7 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, |
| (ADG713 Only) | | 1 | ns min | $V_{S1}$ = $V_{S2}$ = 2 V; Test Circuit 5 |
| Charge Injection | 3 | | pC typ | $V_S$ = 1.5 V; $R_S$ = 0 Ω, $C_L$ = 1 nF; |
| | | | | Test Circuit 6 |
| Off Isolation | −58 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz |
| | −78 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | Test Circuit 7 |
| Channel-to-Channel Crosstalk | −90 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; |
| | | | | Test Circuit 8 |
| Bandwidth −3 dB | 200 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Test Circuit 9 |
| $C_S$ (OFF) | 10 | | pF typ | |
| $C_D$ (OFF) | 10 | | pF typ | |
| $C_D$, $C_S$ (ON) | 22 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = +3.3 V |
| $I_{DD}$ | 0.001 | | µA typ | Digital Inputs = 0 V or 3 V |
| | | 1.0 | µA max | |

NOTES
[1]Temperature range: B Version: −40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

# ADG711/ADG712/ADG713

**ABSOLUTE MAXIMUM RATINGS**[1]

($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{DD}$ to GND | –0.3 V to +6 V |
| Analog, Digital Inputs[2] | –0.3 V to $V_{DD}$ +0.3 V or |
| | 30 mA, Whichever Occurs First |
| Continuous Current, S or D | 30 mA |
| Peak Current, S or D | 100 mA |

(Pulsed at 1 ms, 10% Duty Cycle max)

Operating Temperature Range
Industrial (B Version) ................ –40°C to +85°C
Storage Temperature Range ........... –65°C to +150°C
Junction Temperature ......................... 150°C
TSSOP Package, Power Dissipation ............. 430 mW
  $\theta_{JA}$ Thermal Impedance ..................... 150°C/W
  $\theta_{JC}$ Thermal Impedance ..................... 27°C/W

SOIC Package, Power Dissipation .............. 520 mW
  $\theta_{JA}$ Thermal Impedance .................... 125°C/W
  $\theta_{JC}$ Thermal Impedance ..................... 42°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) ...................... 215°C
  Infrared (15 sec) ......................... 220°C
ESD ......................................... 2 kV

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG711/ADG712/ADG713 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**WARNING!**

**ESD SENSITIVE DEVICE**

## ORDERING GUIDE

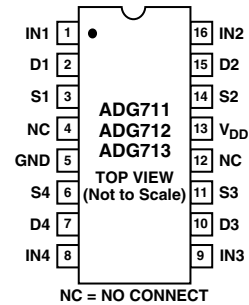| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG711BR | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG711BR-REEL | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG711BR-REEL7 | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG711BRU | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG711BRU-REEL | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG711BRU-REEL7 | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BR | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG712BR-REEL | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG712BR-REEL7 | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG712BRU | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BRU-REEL | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BRU-REEL7 | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BRUZ* | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BRUZ-REEL* | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG712BRUZ-REEL7* | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG713BR | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG713BR-REEL | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG713BR-REEL7 | –40°C to +85°C | Standard Small Outline (SOIC) | R-16 |
| ADG713BRU | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG713BRU-REEL | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |
| ADG713BRU-REEL7 | –40°C to +85°C | Thin Shrink Small Outline (TSSOP) | RU-16 |

*Z = Pb-free part.

REV. A

# ADG711/ADG712/ADG713

**Table I. Truth Table (ADG711/ADG712)**

| ADG711 In | ADG712 In | Switch Condition |
|---|---|---|
| 0 | 1 | ON |
| 1 | 0 | OFF |

**Table II. Truth Table (ADG713)**

| Logic | Switch 1, 4 | Switch 2, 3 |
|---|---|---|
| 0 | OFF | ON |
| 1 | ON | OFF |

**PIN CONFIGURATION (TSSOP/SOIC)**

ADG711 / ADG712 / ADG713 TOP VIEW (Not to Scale)

IN1 1 / IN2 16
D1 2 / D2 15
S1 3 / S2 14
NC 4 / VDD 13
GND 5 / NC 12
S4 6 / S3 11
D4 7 / D3 10
IN4 8 / IN3 9

NC = NO CONNECT

## TERMINOLOGY

| | |
|---|---|
| $V_{DD}$ | Most positive power supply potential. |
| GND | Ground (0 V) reference. |
| S | Source terminal. May be an input or output. |
| D | Drain terminal. May be an input or output. |
| IN | Logic control input. |
| $R_{ON}$ | Ohmic resistance between D and S. |
| $\Delta R_{ON}$ | On resistance match between any two channels, i.e., $R_{ON}$max–$R_{ON}$min. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $I_S$ (OFF) | Source leakage current with the switch "OFF." |
| $I_D$ (OFF) | Drain leakage current with the switch "OFF." |
| $I_D, I_S$ (ON) | Channel leakage current with the switch "ON." |
| $V_D (V_S)$ | Analog voltage on terminals D, S. |
| $C_S$ (OFF) | "OFF" switch source capacitance. |
| $C_D$ (OFF) | "OFF" switch drain capacitance. |
| $C_D, C_S$ (ON) | "ON" switch capacitance. |
| $t_{ON}$ | Delay between applying the digital control input and the output switching on. |
| $t_{OFF}$ | Delay between applying the digital control input and the output switching off. |
| $t_D$ | "OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another. (ADG713 only). |
| Crosstalk | A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. |
| Off Isolation | A measure of unwanted signal coupling through an "OFF" switch. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Bandwidth | The frequency at which the output is attenuated by 3 dB. |
| On Response On Loss | The frequency response of the "ON" switch. The voltage drop across the "ON" switch, seen on the on response vs. frequency plot as how many dBs the signal is away from 0 dB at very low frequencies. |

REV. A –5–

Downloaded from Elcodis.com electronic components distributor

# ADG711/ADG712/ADG713 –Typical Performance Characteristics
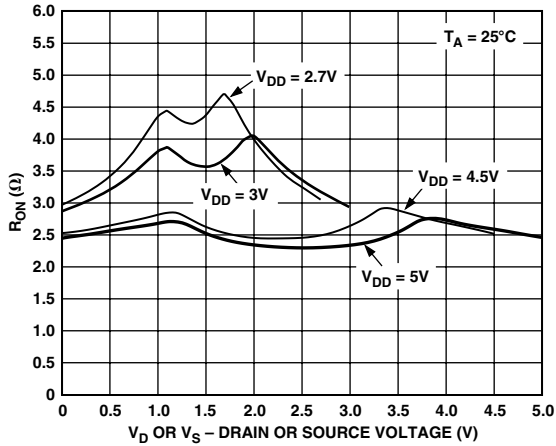


Figure 1. On Resistance as a Function of $V_D$ ($V_S$)



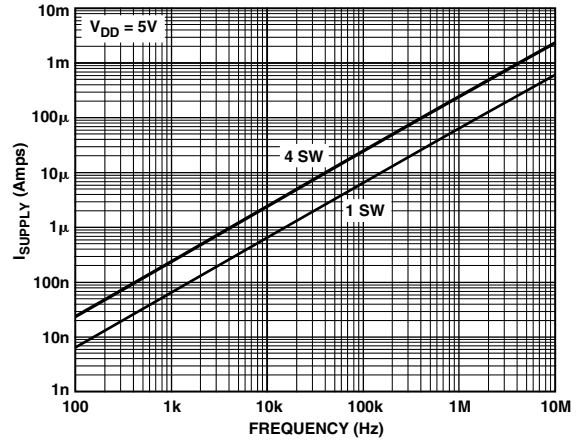Figure 2. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures $V_{DD}$ = 3 V



Figure 3. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures $V_{DD}$ = 5 V



Figure 4. Supply Current vs. Input Switching Frequency



Figure 5. Off Isolation vs. Frequency
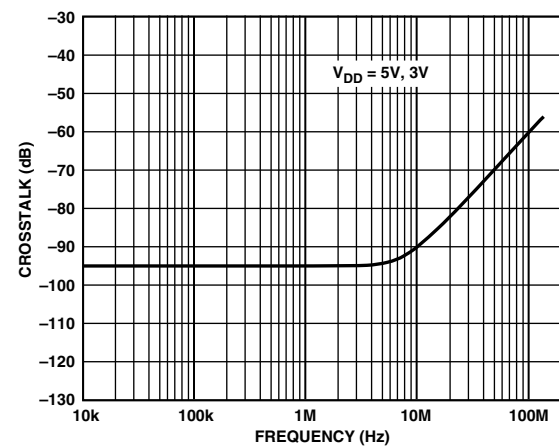


Figure 6. Crosstalk vs. Frequency

–6–

REV. A
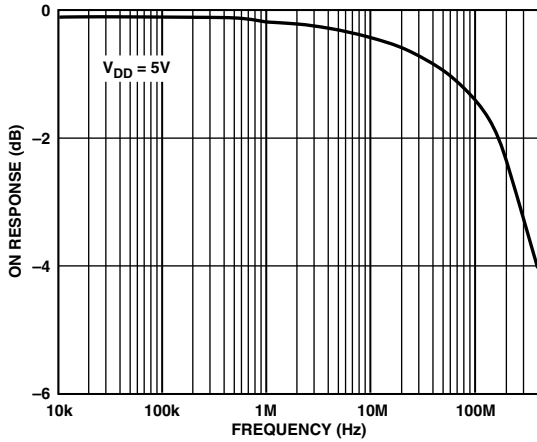
Figure 7. On Response vs. Frequency
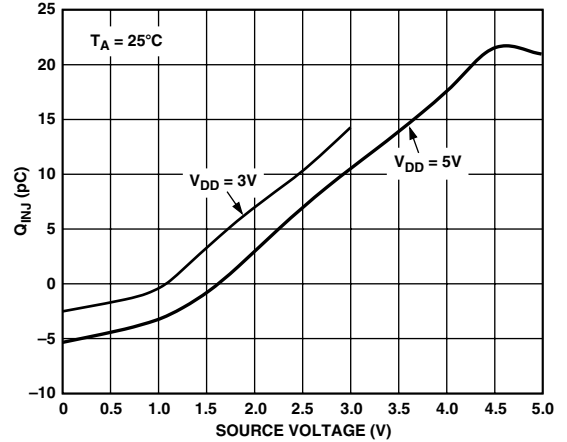


Figure 8. Charge Injection vs. Source Voltage

**APPLICATIONS**

Figure 9 illustrates a photodetector circuit with programmable gain. An AD820 is used as the output operational amplifier. With the resistor values shown in the circuit, and using different combinations of the switches, gain in the range of 2 to 16 can be achieved.
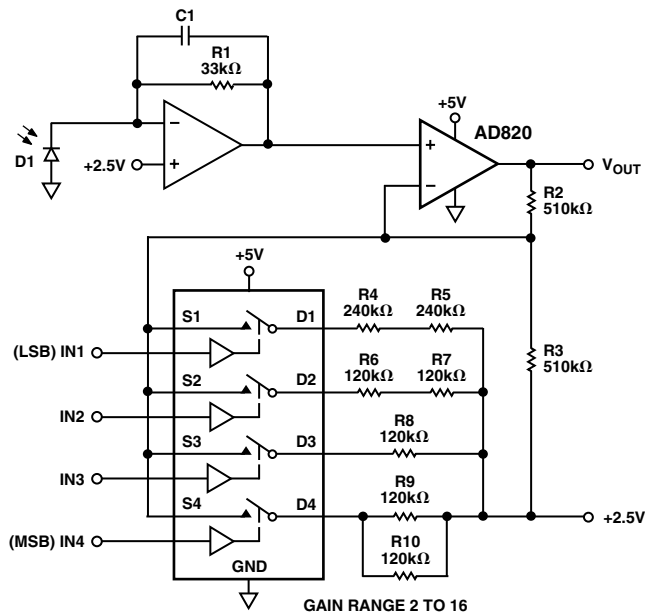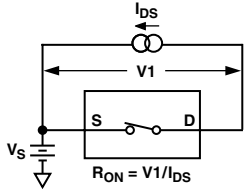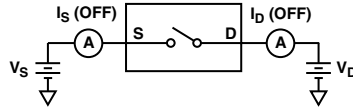


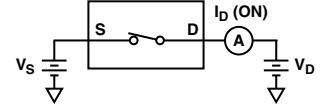Figure 9. Photodetector Circuit with Programmable Gain
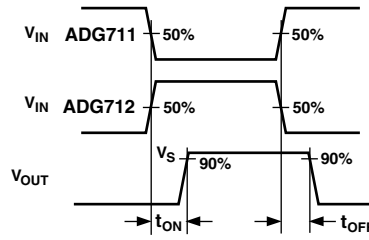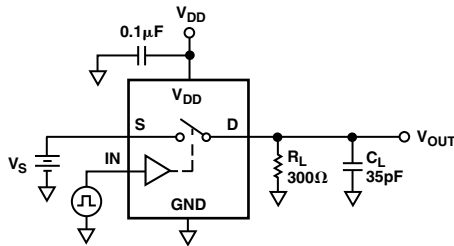
REV. A

–7–

# ADG711/ADG712/ADG713
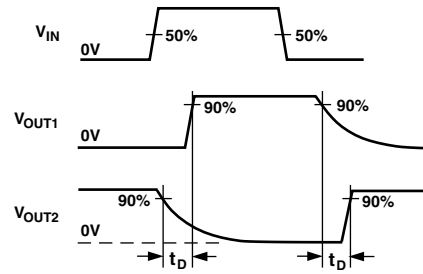
## Test Circuits



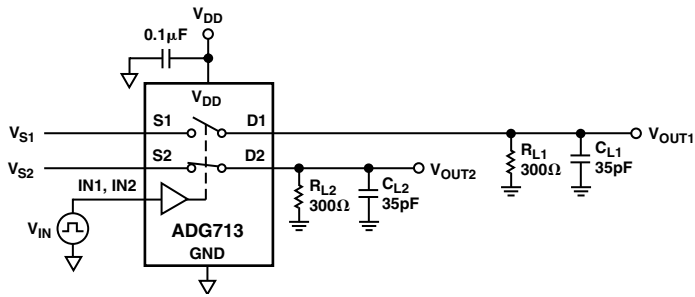Test Circuit 1.  On Resistance



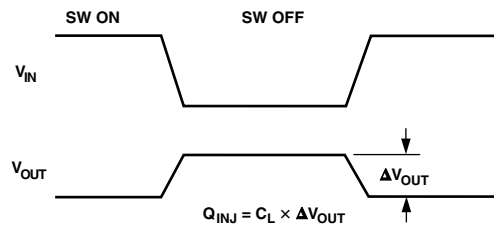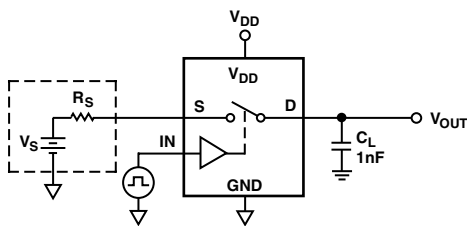Test Circuit 2.  Off Leakage



Test Circuit 3.  On Leakage



Test Circuit 4.  Switching Times



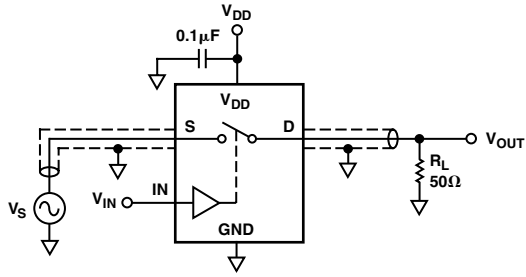Test Circuit 5.  Break-Before-Make Time Delay, $t_D$
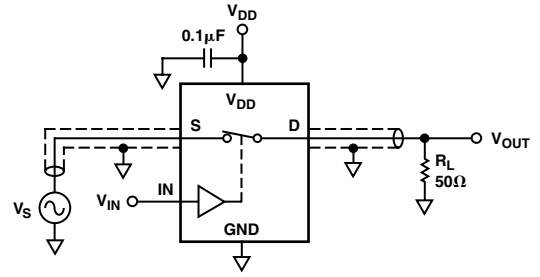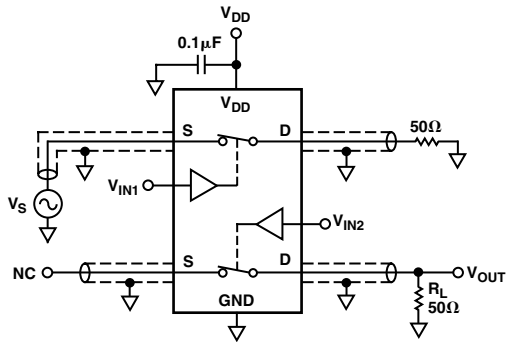


Test Circuit 6.  Charge Injection

REV. A

Test Circuit 7.  Off Isolation



Test Circuit 9.  Bandwidth



CHANNEL-TO-CHANNEL CROSSTALK = 20 × LOG $|V_S/V_{OUT}|$

Test Circuit 8.  Channel-to-Channel Crosstalk

REV. A

–9–

# ADG711/ADG712/ADG713

**16-Lead Standard Small Outline Package [SOIC]**
**Narrow Body**
**(R-16)**
Dimensions shown in millimeters and (inches)

10.00 (0.3937)
9.80 (0.3858)

4.00 (0.1575)
3.80 (0.1496)

16    9
1    8

6.20 (0.2441)
5.80 (0.2283)

1.27 (0.0500)
BSC

1.75 (0.0689)
1.35 (0.0531)

0.50 (0.0197)
0.25 (0.0098) × 45°

0.25 (0.0098)
0.10 (0.0039)

COPLANARITY
0.10

0.51 (0.0201)
0.31 (0.0122)

SEATING
PLANE

0.25 (0.0098)
0.17 (0.0067)

8°
0°

1.27 (0.0500)
0.40 (0.0157)

**COMPLIANT TO JEDEC STANDARDS MS-012AC**
**CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS**
**(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR**
**REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN**

**16-Lead Thin Shrink Small Outline Package [TSSOP]**
**(RU-16)**
Dimensions shown in millimeters

5.10
5.00
4.90

4.50
4.40
4.30

16    9
1    8

6.40
BSC

PIN 1

1.20
MAX

0.15
0.05

0.65
BSC

0.30
0.19

COPLANARITY
0.10

SEATING
PLANE

0.20
0.09

8°
0°

0.75
0.60
0.45

**COMPLIANT TO JEDEC STANDARDS MO-153AB**

–10–

REV. A

# Revision History