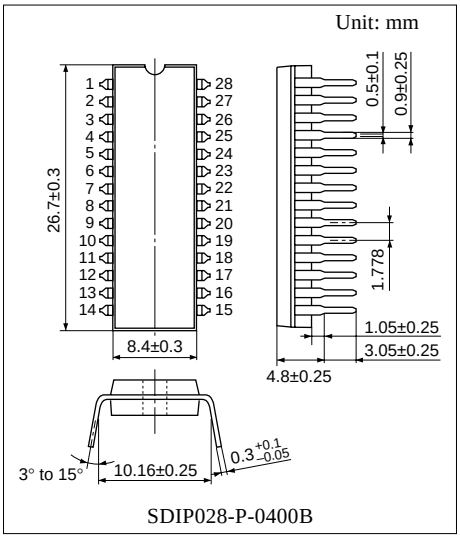
AN5819K

Sound multiplex demodulator IC for TV in the North American market

■ Overview

The AN5819K is a single chip IC, which includes a sound multiplex demodulator for Zenith TV system and the dbx TV sound noise reduction function.



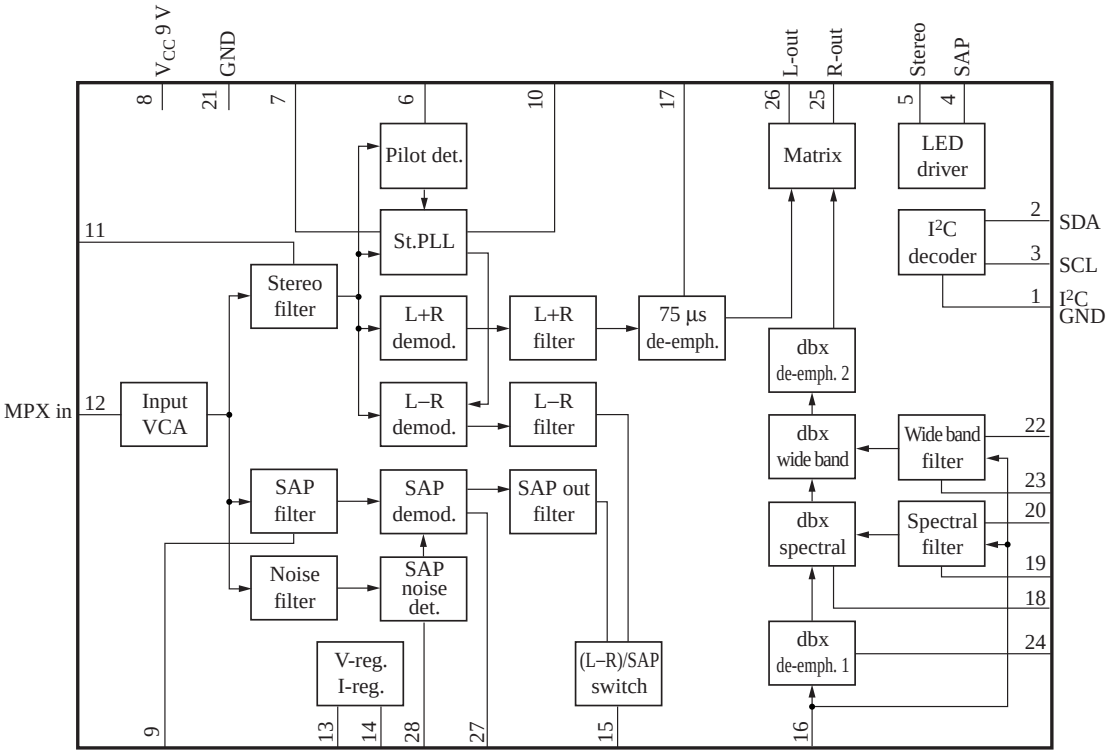
■ Features

- Stereo demodulation, SAP demodulation and dbx noise reduction are integrated into a single chip
- Enabling various kinds of adjustment and mode changeover thanks to I²C bus
- Built-in input volume (I²C control) for interface with intermediate frequency processing IC

■ Applications

- TV and VCR for the North American market
  (A licensing agreement with THAT Corporation is necessary in order to use this IC with built-in dbx-TV noise reduction function.)

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	I^2C GND	15	(L–R)/SAP demodulation output
2	SDA	16	dbx input
3	SCL	17	(L+R) demodulation output offset cancel
4	SAP LED	18	Spectral level adjustment
5	Stereo LED	19	Spectral timing
6	Pilot signal detection	20	Spectral level sensor input
7	Stereo PLL filter	21	GND
8	V_{CC}	22	Wide band level sensor input
9	SAP trap filter	23	Wide band timing
10	Quasi sine-wave filter	24	dbx offset cancel
11	Stereo filter offset cancel	25	R output
12	Composite input	26	L output
13	dbx timing current	27	SAP carrier detection
14	Reference voltage source filter	28	SAP noise level detection

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	11.0	V
Supply current	I_{CC}	75	mA
LED drive current *3	I_{LED}	10	mA
Power dissipation *2	P_D	1 143	mW
Operating ambient temperature *1	T_{opr}	–20 to +75	°C
Storage temperature *1	T_{stg}	–55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2: Power dissipation shown is for the IC package in free air at T_a = 70°C
∗3: LED drive currents are the currents flowing into pin 4 and pin 5.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	8.5 to 9.5	V

■ Electrical Characteristics at V_{CC} = 9.0 V, T_a = 25°C

- Stereo PLL VCO adjustment: 15.734 kHz ± 50 Hz
- Input level (at 100% modulation)
  L+R: 0.424 V[p-p] (pre-emphasis off)
  L–R: 0.848 V[p-p] (dbx noise reduction off)
  Pilot: 0.084 V[p-p]
  SAP: 0.254 V[p-p] (dbx noise reduction off)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Total circuit current	I_{CC}	No signal	35	55	75	mA
Mono output level	$V_{0(MON)}$	f = 1 kHz, (mono) 100%mod.	480	530	580	mV[rms]
Mono frequency characteristics-1	$V_{1(MON)}$	f = 300 Hz, (mono) 30%mod.	– 0.5	0	+0.5	dB
Mono frequency characteristics-2	$V_{2(MON)}$	f = 8 kHz, (mono) 30%mod.	–1.5	– 0.4	+0.4	dB
Mono distortion ratio	$THD_{(MON)}$	f = 1 kHz, (mono) 100%mod.	—	—	0.7	%
Mono noise level	$V_{N(MON)}$	Input short-circuit, BPF (A curve)	—	—	–60	dBV
(L), (R) output voltage difference	$V_{LR(MON)}$	f = 1 kHz, (mono) 100%mod.	– 0.5	0	+0.5	dB
Stereo output level	$V_{0(ST)}$	f = 1 kHz, (L(R)-only) 100%mod.	420	520	620	mV[rms]
Stereo frequency characteristics-1	$V_{1(ST)}$	f = 300 Hz, (L(R)-only) 30%mod.	– 0.7	0	+0.7	dB
Stereo frequency characteristics-2	$V_{2(ST)}$	f = 3 kHz, (L(R)-only) 30%mod.	–1	0	+1	dB
Stereo frequency characteristics-3	$V_{3(ST)}$	f = 8 kHz, (L(R)-only) 30%mod.	–2.5	– 0.5	+1.5	dB
Stereo distortion ratio	$THD_{(ST)}$	f = 1 kHz, (L(R)-only) 100%mod.	—	—	1	%
Stereo noise level	$V_{N(ST)}$	f = 15.73 kHz, (f_H), V= 0.084 V[p-p], BPF	—	—	–60	dBV
Stereo discrimination level	$V_{TH(ST)}$	f = 15.73 kHz (f_H)	9	17	26	mV[rms]
Stereo discrimination hysteresis	$V_{HY(ST)}$	f = 15.73 kHz (f_H)	–6	—	– 0.5	dB
SAP output level	$V_{0(SAP)}$	f = 1 kHz, (SAP) 100%mod.	350	500	700	mV[rms]
SAP frequency characteristics-1	$V_{1(SAP)}$	f = 300 Hz, (SAP) 30%mod.	–1.0	0	+1.0	dB
SAP frequency characteristics-2	$V_{2(SAP)}$	f = 3 kHz, (SAP) 30%mod.	–3	–1.5	+0.5	dB
SAP distortion ratio	$THD_{(SAP)}$	f = 1 kHz, (SAP) 100%	—	—	1.5	%
SAP noise level	$V_{N(SAP)}$	f = 78.7 kHz, ($5f_H$),V= 0.42 V[p-p], BPF	—	—	–65	dBV
SAP discrimination level	$V_{TH(SAP)}$	f = 78.7 kHz, ($5f_H$)	22	—	53	mV[rms]
SAP discrimination hysteresis	$V_{HY(SAP)}$	f = 78.7 kHz, ($5f_H$)	–4	—	– 0.5	dB
SAP → Stereo crosstalk	CT_1	(SAP) 1 kHz, 100%mod. (Stereo) pilot-signal	—	—	–50	dB
Stereo → SAP crosstalk	CT_2	(Stereo) 1 kHz, 100%mod. (SAP) carrier-signal	—	—	–50	dB
Noise discrimination level	$V_{TH(NOI)}$	Pin 27: f = 240 kHz at 5 V applied	38	—	84	mV[rms]
Noise discrimination hysteresis	$V_{HY(NOI)}$	Pin 27: f = 240 kHz at 5 V applied	–5.5	—	– 0.3	dB

■ Electrical Characteristics at V_{CC} = 9.0 V, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface						
Sink current at ACK	I_{ACK}	Maximum pin-2 sink current at ACK	2.0	10	20	mA
SCL, SDA signal input high level	V_{IHI}	—	3.5	—	5.0	V
SCL, SDA signal input low level	V_{ILO}	—	0	—	0.9	V
Input available maximum frequency	f_{IMAX}	—	—	—	100	kbit/s

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Stereo separation (30%)-1	$Sep_{30\text{-}1}$	f = 300 Hz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-2	$Sep_{30\text{-}2}$	f = 1 kHz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-3	$Sep_{30\text{-}3}$	f = 3 kHz, (L(R)-only) 30%mod.	22	30	—	dB
Stereo separation (30%)-4	$Sep_{30\text{-}4}$	f = 8 kHz, (L(R)-only) 30%mod.	12	18	—	dB
Stereo separation (100%)-1	$Sep_{100\text{-}1}$	f = 300 Hz, (L(R)-only) 100%mod.	20	30	—	dB
Stereo separation (100%)-2	$Sep_{100\text{-}2}$	f = 1 kHz, (L(R)-only) 100%mod.	20	25	—	dB
Stereo separation (100%)-3	$Sep_{100\text{-}3}$	f = 3 kHz, (L(R)-only) 100%mod.	20	30	—	dB
Stereo separation (100%)-4	$Sep_{100\text{-}4}$	f = 8 kHz, (L(R)-only) 100%mod.	8	11	—	dB
Stereo separation (10%)-1	$Sep_{10\text{-}1}$	f = 300 Hz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-2	$Sep_{10\text{-}2}$	f = 1 kHz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-3	$Sep_{10\text{-}3}$	f = 3 kHz, (L(R)-only) 10%mod.	20	30	—	dB
Stereo separation (10%)-4	$Sep_{10\text{-}4}$	f = 8 kHz, (L(R)-only) 10%mod.	12	18	—	dB
SAP → Mono crosstalk	CT_3	(SAP) 1 kHz, 100%mod. (Mono)1 kHz, 0%mod.	—	—	–53	dB
Mono → SAP crosstalk	CT_4	(SAP) 1 kHz, 0%mod. (Mono) 1 kHz, 100%mod.	—	—	–56	dB
I²C interface						
Bus free before start	t_{BUF}	—	4.0	—	—	µs
Start condition set-up time	$t_{SU.STA}$	—	4.0	—	—	µs
Start condition hold time	$t_{HD.STA}$	—	4.0	—	—	µs
Low period SCL, SDA	t_{LO}	—	4.0	—	—	µs
High period SCL	t_{HI}	—	4.0	—	—	µs
Rise time SCL, SDA	t_r	—	—	—	1.0	µs
Fall time SCL, SDA	t_f	—	—	—	0.35	µs
Data set-up time (write)	$t_{SU.DAT}$	—	0.25	—	—	µs
Data hold time (write)	$t_{HD.DAT}$	—	0	—	—	µs

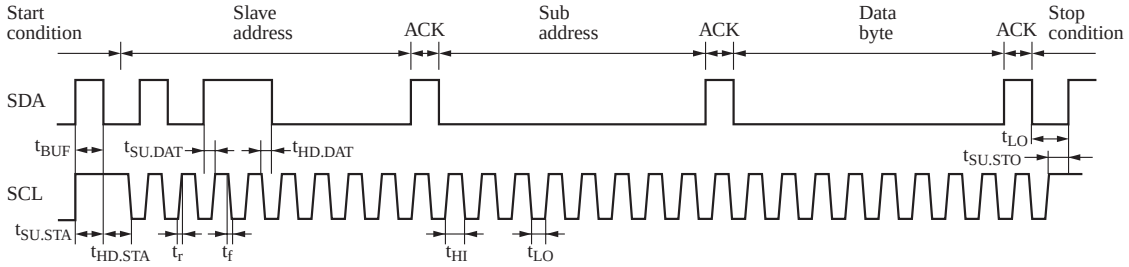
■ Electrical Characteristics at V_{CC} = 9.0 V, T_a = 25°C (continued)

• Design reference data

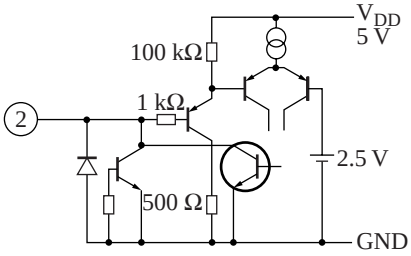
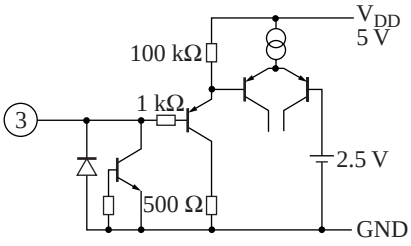
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface (continued)						
Acknowledge set-up time	$t_{SU.ACK}$	—	—	—	3.5	µs
Acknowledge hold time	$t_{HD.ACK}$	—	0	—	—	µs
Stop condition set-up time	$t_{SU.STO}$	—	4.0	—	—	µs
DAC						
6-bit DAC DNLE	L_6	1LSB = (data (max.)–data (00))/63	0.1	1.0	1.9	LSB/Step

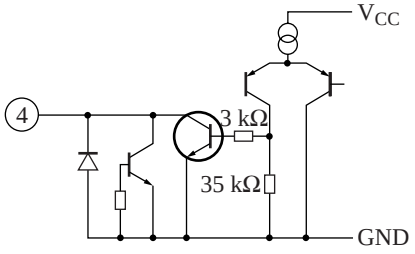
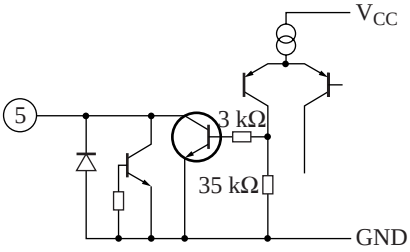
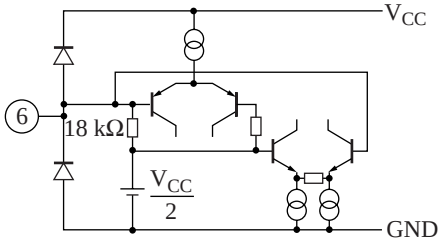
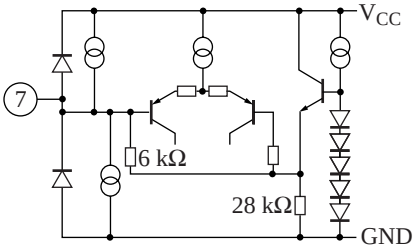
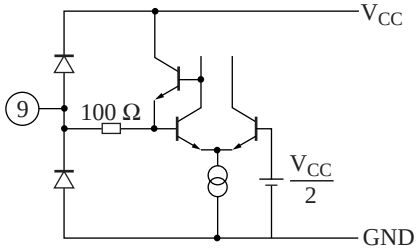
• DAC timing chart



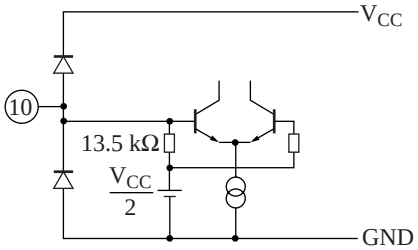
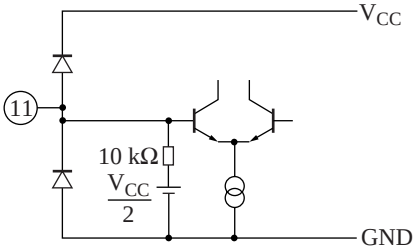
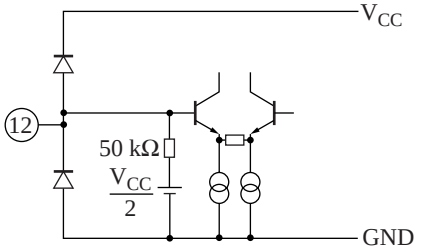
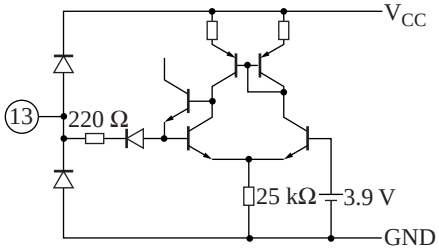
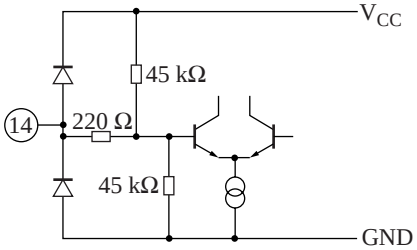
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage (V)
1	—	I²C GND: • I²C bus DAC GND pin	0
2		SDA: • I²C bus data input pin	—
3		SCL: • I²C bus clock input pin	—

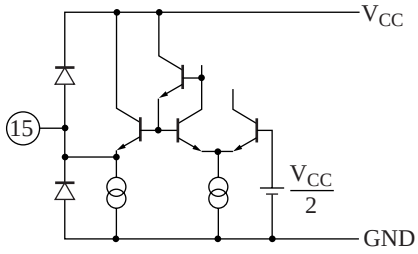
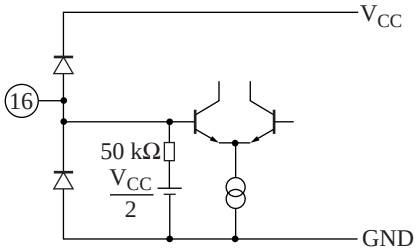
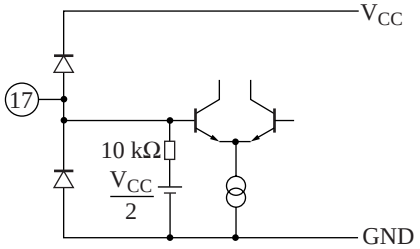
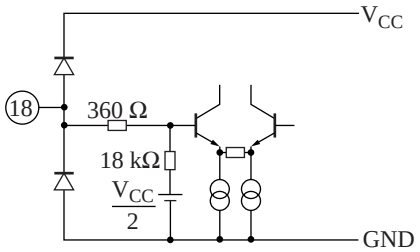
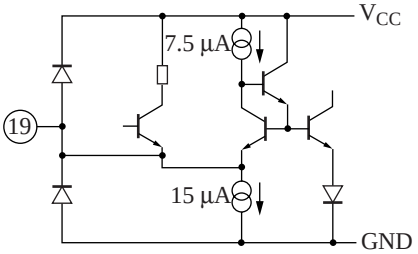
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
4		SAP LED: • SAP LED connection pin	—
5		Stereo LED: • Stereo LED connection pin	—
6		Pilot signal detection: • Stereo pilot signal detection pin	$\frac{V_{CC}}{2}$
7		Stereo PLL filter: • Stereo PLL low-pass filter connection pin	2.8
8	—	V_{CC}: • V_{CC} pin	V_{CC}
9		SAP trap filter: • SAP trap filter	$\frac{V_{CC}}{2}$

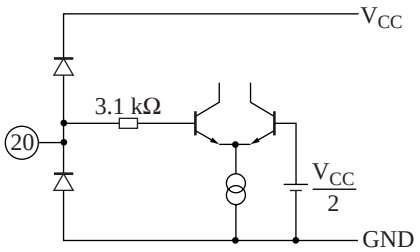
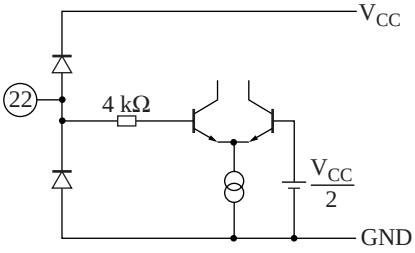
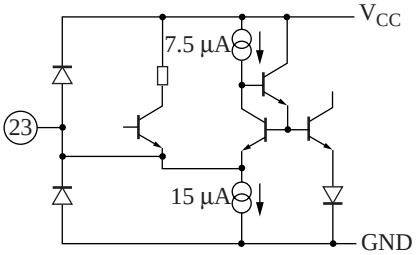
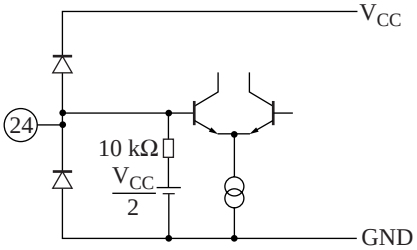
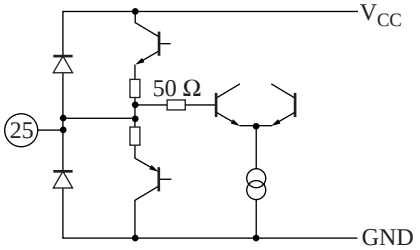
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
10		Quasi sine-wave filter: • Low-pass filter pin in quasi-sine wave circuit	$\frac{V_{CC}}{2}$
11		Stereo filter offset cancel: • Offset cancel pin for stereo filter output	$\frac{V_{CC}}{2}$
12		Composite input: • Composite signal input pin	$\frac{V_{CC}}{2}$
13		dbx timing current: • Timing current setting pin for dbx RMS detection	1.3
14		Reference: • Reference power supply stabilization pin	$\frac{V_{CC}}{2}$

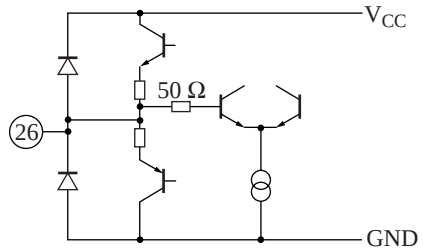
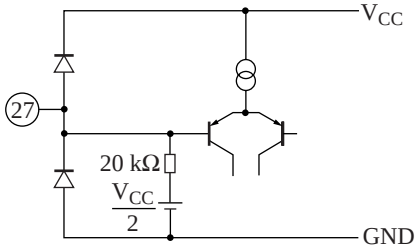
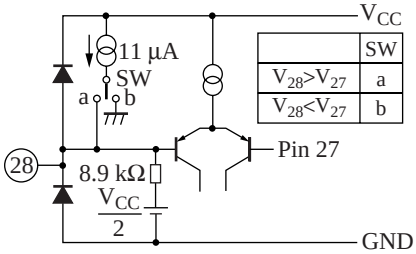
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
15		(L-R)/SAP demodulation output: • (L-R)/SAP demodulation signal output pin	$\frac{V_{CC}}{2} - 0.7$
16		dbx input: • Input signal of (L-R)/SAP signal to dbx NR	$\frac{V_{CC}}{2}$
17		(L+R) demodulation output offset cancel: • (L+R) demodulation signal offset cancel pin	$\frac{V_{CC}}{2}$
18		Spectral level adjustment: • Variable emphasis level adjustment pin	$\frac{V_{CC}}{2}$
19		Spectral timing: • RMS detection recovery time setting pin for variable emphasis	0.2

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
20		Spectral level sensor input: • RMS detection circuit input pin for variable emphasis	$\frac{V_{CC}}{2}$
21	—	GND: • GND pin	0
22		Wideband level sensor input: • RMS detection circuit input pin for wide band expander	$\frac{V_{CC}}{2}$
23		Wideband timing: • RMS detection recovery time setting pin for wide band expander	0.2
24		dbx offset cancel: • dbx NR output offset cancel pin	$\frac{V_{CC}}{2}$
25		R output: • R line-out output pin	$\frac{V_{CC}}{2}$

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage (V)
26		L output: • L line-out output pin	$\frac{V_{CC}}{2}$
27		SAP carrier detection: • SAP signal carrier level detection pin	$\frac{V_{CC}}{2}$
28		SAP noise level setting: • Noise detection pin for SAP mal-function prevention circuit (Mute SAP demodulation at detecting noise)	$\frac{V_{CC}}{2}$

■ Application Circuit Example