

Low-Voltage Dual SPST Analog Switch

FEATURES

- Wide Operation Voltage (+2.7 to +12 V)
- Low Charge Injection - Q_{INJ} : 1 pC
- Low Power Consumption
- TTL/CMOS Logic Compatible Over The Full Operating Voltage range
- Available in MSOP-8 and SOT23-8

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

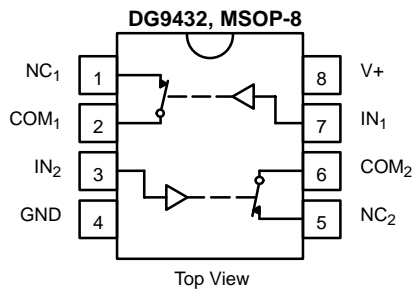
DESCRIPTION

The DG9432/9433/9434 is a dual single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 25 ns, t_{OFF} : 20 ns), the DG9432/9433/9434 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

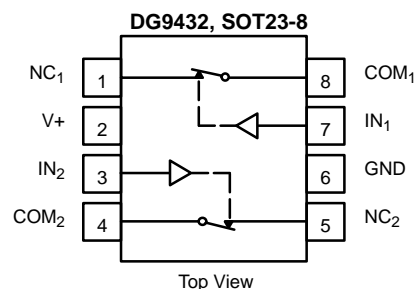
The DG9432/9433/9434 is built on Vishay Siliconix's low voltage BCD-15 process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9432/9433/9434.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9432



Device Marking: 9432



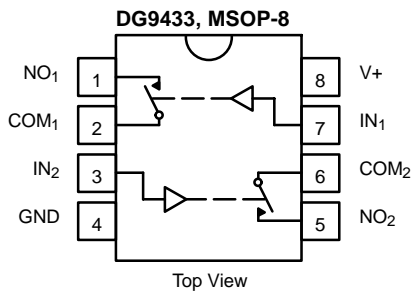
Device Marking: 4G

TRUTH TABLE DG9432

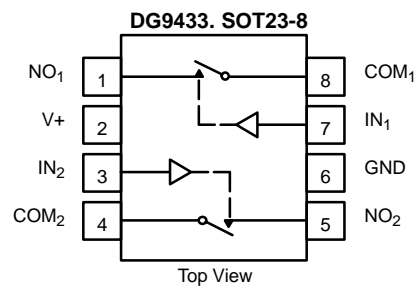
Logic	Switch
0	On
1	Off



FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9433/DG9434

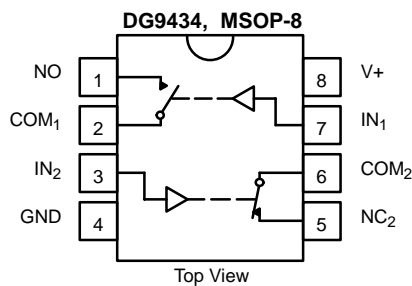


Device Marking: 9433

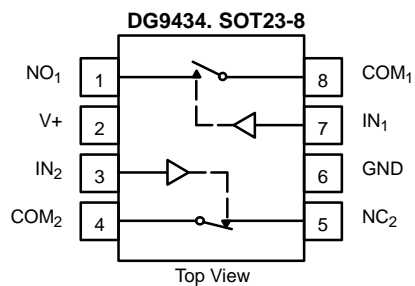


Device Marking: 4H

TRUTH TABLE DG9433	
Logic	Switch
0	Off
1	On



Device Marking: 9434



Device Marking: 4I

TRUTH TABLE DG9434		
Logic	Switch-1	Switch-2
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	MSOP-8	DG9432DQ
		DG9433DQ
		DG9434DQ
	SOT23-8	DG9432DS
		DG9433DS
		DG9434DS



ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +13.5 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±10 mA
Peak Current	±20 mA
(Pulsed at 1ms, 10% duty cycle)		
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages)^b

MSOP-8 ^c	320 mW
SOT23-8 ^c	515 mW

Notes:

- a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 6.5 mW/°C above 75°C

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3.3 V, ±10%, V _{IN} = 0.4 or 1.8 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	V _{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	r _(on)	V+ = 2.7 V, I _{COM} = 1 mA, V _{COM} = 1.5 V	Room		81	100	Ω
r _(on) Match ^d	Δr _(on)		Room		0.4	3.0	
Digital Control							
Input, High Voltage	V _{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V _{INL}		Full			0.4	
Input Current	I _{INH}			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	t _{OPEN}	V+ = 3 V, R _L = 300 Ω V _{NO} = V _{NC} = 1.5 V C _L = 35 pF, V _{IN} = 0 V, 3 V	Room	1			ns
Turn-On Time ^d	t _{ON}		Full		60	80	
Turn-Off Time ^d	t _{OFF}		Full		14	25	
Charge Injection ^d	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _g = 0 V	Room		0.16		pC
Off-Isolation ^d	OIRR	C _L = 5 pF, R _L = 50 Ω, f = 1 MHz	Room		77		dB
		C _L = 5 pF, R _L = 50 Ω, f = 10 MHz	Room		55		
Crosstalk ^d	X _{TALK}	R _L = 50 Ω, f = 1 MHz, V+ = 2.5 V	Room		98		
Source Off Capacitance ^d	C _{NC/NO(off)}	f = 1 MHz, V _{NC/NO} = 0 V	Room		7.5		pF
Drain Off Capacitance ^d	C _{COM(off)}	f = 1 MHz, V _{COM} = 0 V	Room		7.8		
Drain On Capacitance ^d	C _{COM(on)}		Room		22		
Supply Current	I ₊	V+ = 3.3 V, V _{IN} = 0 or V+	Room	-1		-1	μA

Notes:

- a. Room = 25°C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 12-V leakage testing, not production tested.
- g. Applies for DG9434 only.

SPECIFICATIONS (V ₊ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V ₊ = 5 V, ± 10%, V _{IN} = 0.4 or 1.8 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	V _{ANALOG}		Full	V ₋		V ₊	V
Drain-Source On-Resistance	r _(on)	V ₊ = 4.5 V, I _{COM} = 1 mA, V _{COM} = 2.5 or 3.5 V	Room Full		39	60 70	Ω
r _{DS(on)} Match	Δr _(on)	V ₊ = 4.5 V, I _{COM} = 1 mA, V _{COM} = 3.5 V	Room		0.3	3.0	
Switch Off Leakage Current ^f	I _{NC/NO(off)}	V ₊ = 5 V, V _{COM} = 0.5 V, 4.5 V V _{NC/NO} = 4.5 V, 0.5 V	Room Full	-1 -10	0.3	1 10	nA
	I _{COM(off)}		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current ^f	I _{COM(on)}		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	V _{INH}	V ₊ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V _{INL}		Full			0.4	
Input Current	I _{INH}			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	t _{OPEN}	V ₊ = 5 V, R _L = 300 Ω V _{NO} = V _{NC} = 3 V C _L = 35 pF, V _{IN} = 0 V, 5 V	Room Full	1			ns
Turn-On Time	t _{ON}		Room Full		33	60 70	
Turn-Off Time	t _{OFF}		Room Full		10	20 30	
Charge Injection ^d	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _g = 0 V	Room		0.56		pC
Off-Isolation ^d	OIRR	C _L = 5 pF, R _L = 50 Ω, f = 1 MHz	Room		76		dB
		C _L = 5 pF, R _L = 50 Ω, f = 10 MHz, V ₊ = 5 V	Room		54		
Crosstalk ^d	X _{TALK}	R _L = 50 Ω, f = 1 MHz, V ₊ = 5 V	Room		96		
Source Off Capacitance ^d	C _{NC/NO(off)}	f = 1 MHz, V _{NO/NC} = 0 V	Room		7.5		pF
Drain Off Capacitance ^d	C _{COM(off)}	f = 1 MHz, V _{COM} = 0 V	Room		7.8		
Drain On Capacitance ^d	C _{COM(on)}		Room		22		
Supply Current	I ₊	V ₊ = 5.5 V, V _{IN} = 0 or V ₊	Room	-1		-1	μA

Notes:

- a. Room = 25°C, Full = as determined by the operating suffix.
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- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, not subjected to production test.
- e. V_{IN} = input voltage to perform proper function.
- f. Guaranteed by 12-V leakage testing, not production tested.
- g. Applies to DG9434 only.



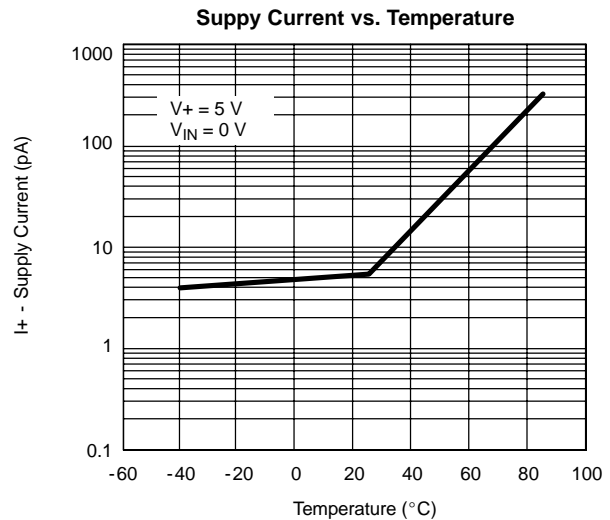
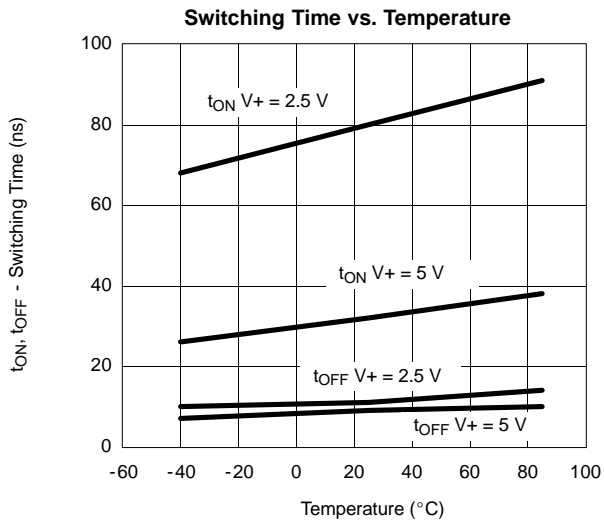
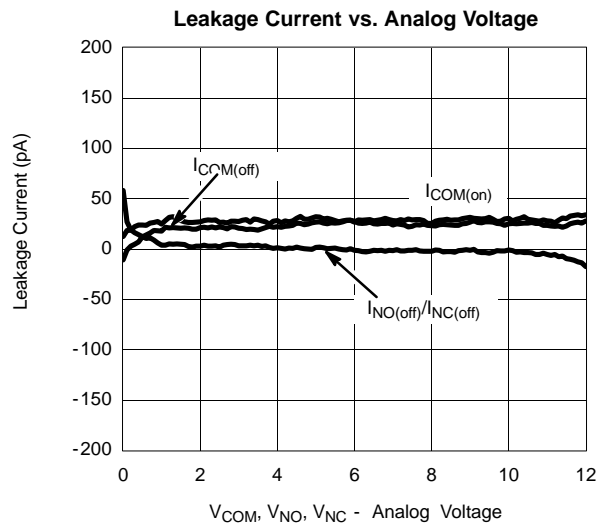
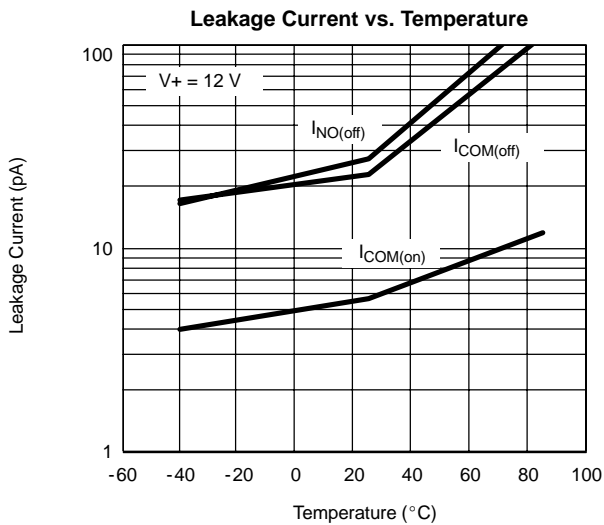
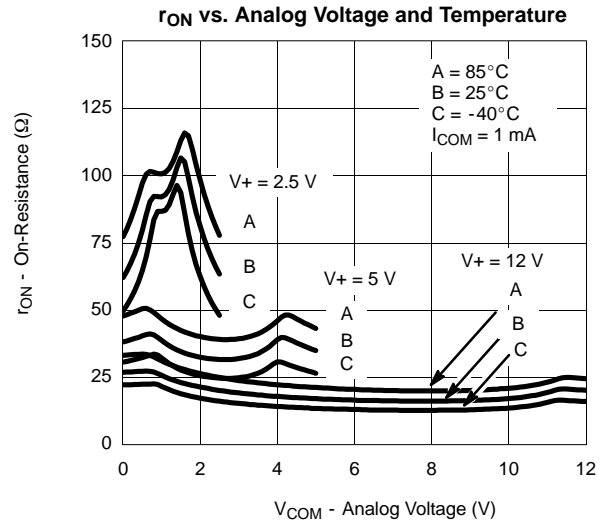
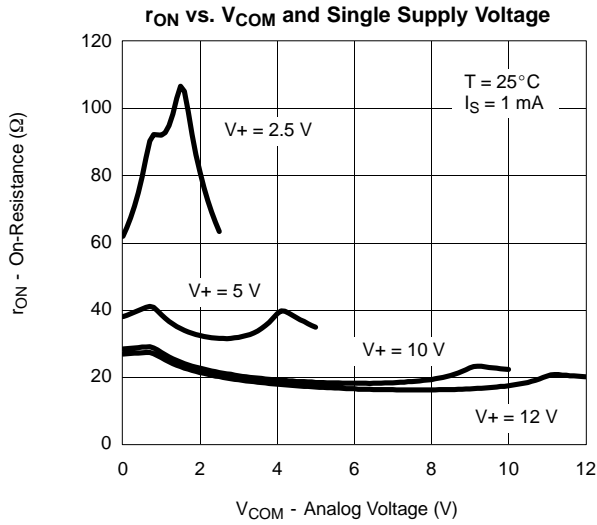
SPECIFICATIONS (V ₊ = 12 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V ₊ = 12 V, ±10%, V _{IN} = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	V _{ANALOG}		Full	V ₋		V ₊	V
Drain-Source On-Resistance	r _(on)	V ₊ = 10.8 V, I _{COM} = 1 mA, V _{COM} = 9 V	Room Full		19	30 40	Ω
r _{DS(on)} Match	Δr _(on)	V ₊ = 10.8 V, I _{COM} = 1 mA, V _{COM} = 9 V	Room		0.3	3.0	
Switch Off Leakage Current ^a	I _{NC/NO(off)}	V ₊ = 12 V, V _S = 1/11 V, V _{COM} = 11/1 V	Room Full	-1 -10	0.3	1 10	nA
	I _{COM(off)}		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current ^a	I _{COM(on)}		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	V _{INH}	V ₊ = 12 V	Full			2.4	V
Input, Low Voltage	V _{INL}		Full	0.8			
Input Current	I _{INH}			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	t _{OPEN}	V ₊ = 12 V, R _L = 300 Ω V _{NO} = V _{NC} = 8 V C _L = 35 pF, V _{IN} = 0 V, 12 V	Room Full	1			ns
Turn-On Time	t _{ON}		Room Full		21	35 40	
Turn-Off Time	t _{OFF}		Room Full		6	18 25	
Charge Injection ^d	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _G = 0 V, V ₊ = 5 V	Room		0.36		pC
Off-Isolation ^d	OIRR	C _L = 5 pF, R _L = 50 Ω, f = 1 MHz	Room		75		dB
		C _L = 5 pF, R _L = 50 Ω, f = 10 MHz	Room		53		
Crosstalk ^d	X _{TALK}	R _L = 50 Ω, f = 1 MHz, V ₊ = 5 V	Room		96		
Source Off Capacitance ^d	C _{NC/NO(off)}	f = 1 MHz, V _{NC/NO} = 0 V	Room		7.5		pF
Drain Off Capacitance ^d	C _{COM(off)}	f = 1 MHz, V _{COM} = 0 V	Room		7.8		
Drain On Capacitance ^d	C _{COM(on)}		Room		22		
Supply Current	I ₊	V ₊ = 12 V, V _{IN} = 0 or V ₊	Room	-1		-1	μA

Notes:

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- g. Applies for DG9434 only.

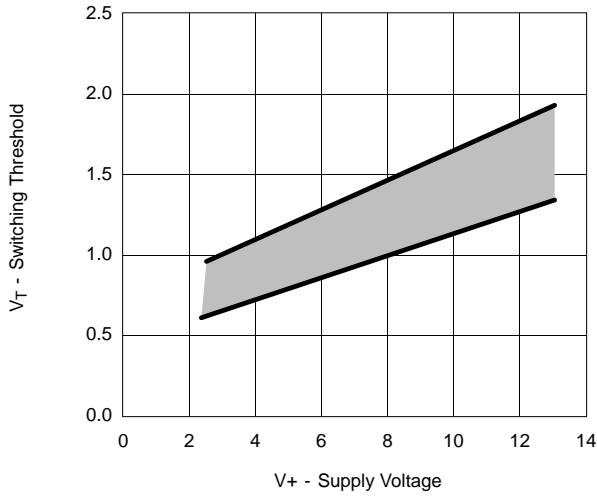


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

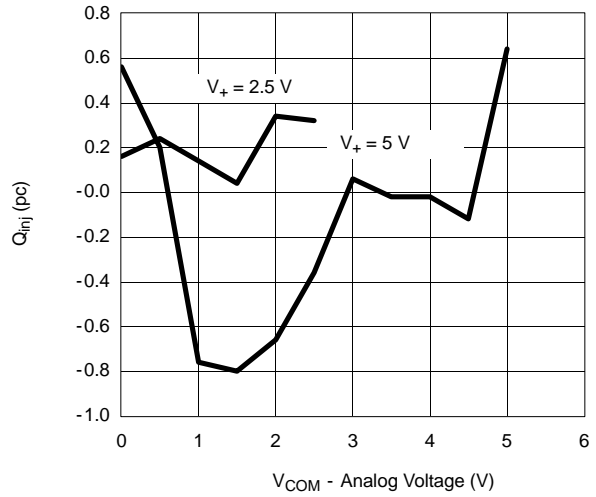


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

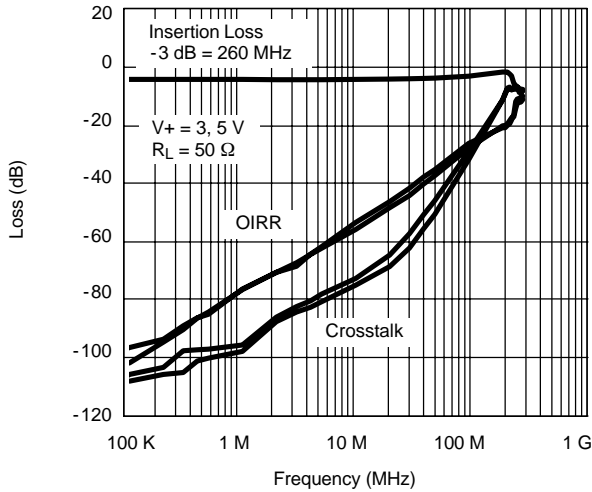
Switching Threshold vs. Supply Voltage



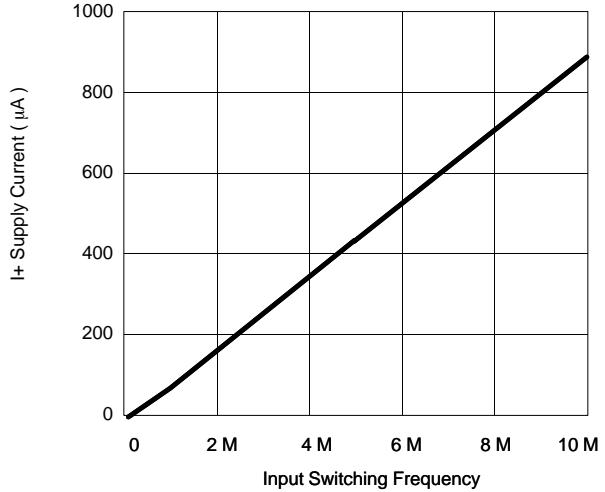
Charge Injection at Source



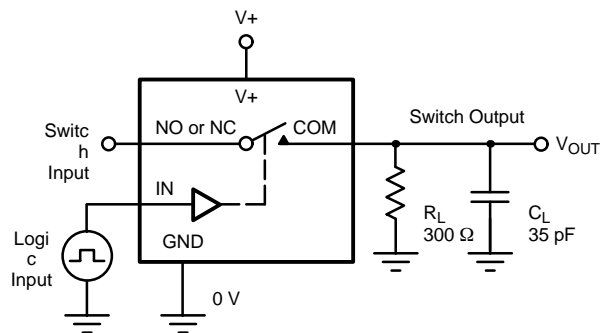
Insertion Loss, Off Isolation and Crosstalk vs. Frequency



Supply Current vs. Input Switching Frequency

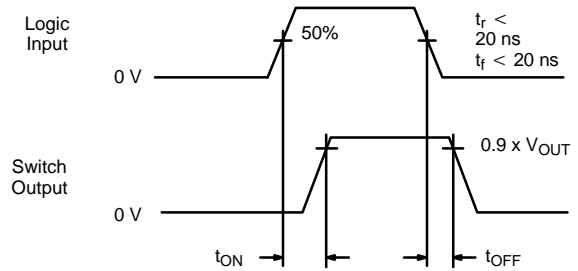


TEST CIRCUITS



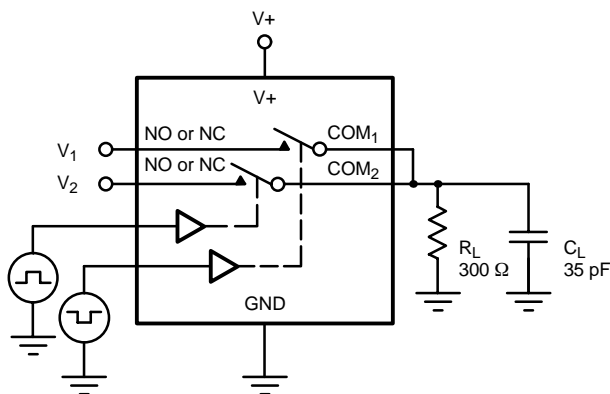
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

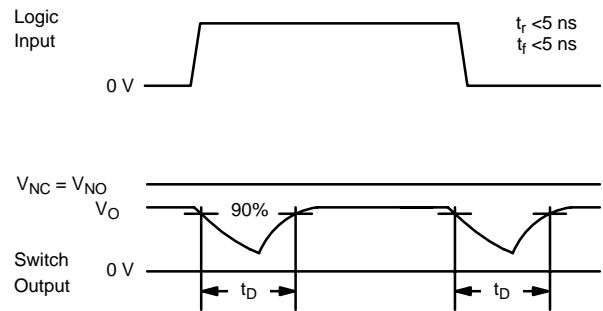
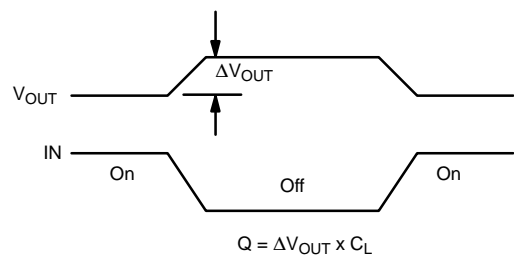
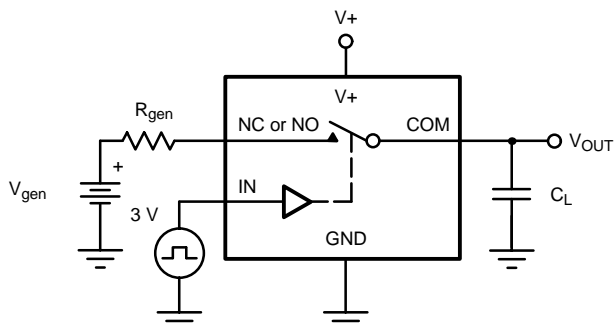


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

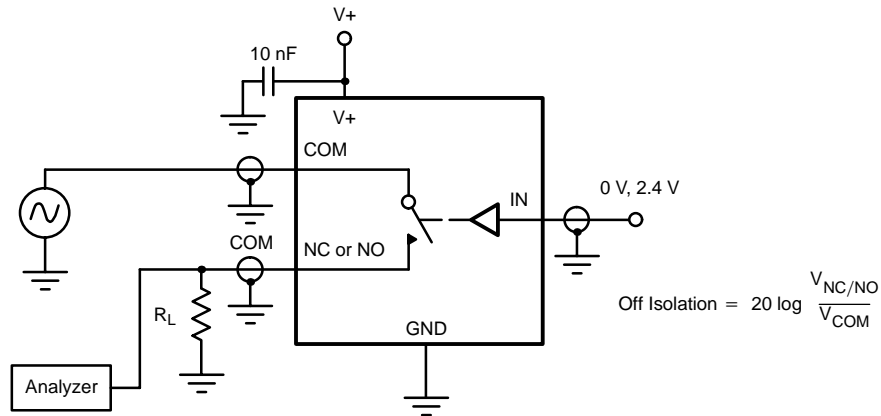


FIGURE 4. Off-Isolation

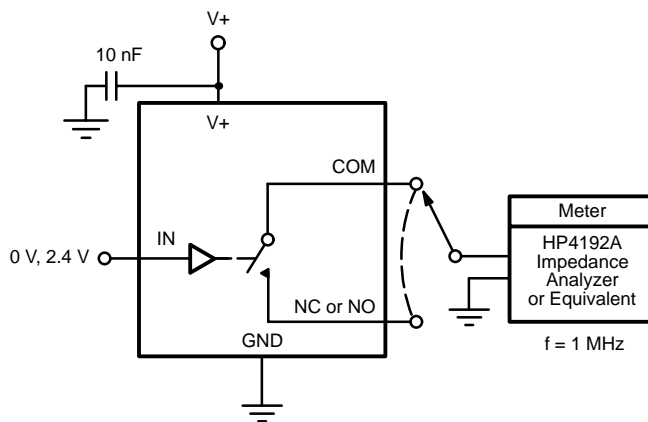


FIGURE 5. Channel Off/On Capacitance



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