

FEATURES

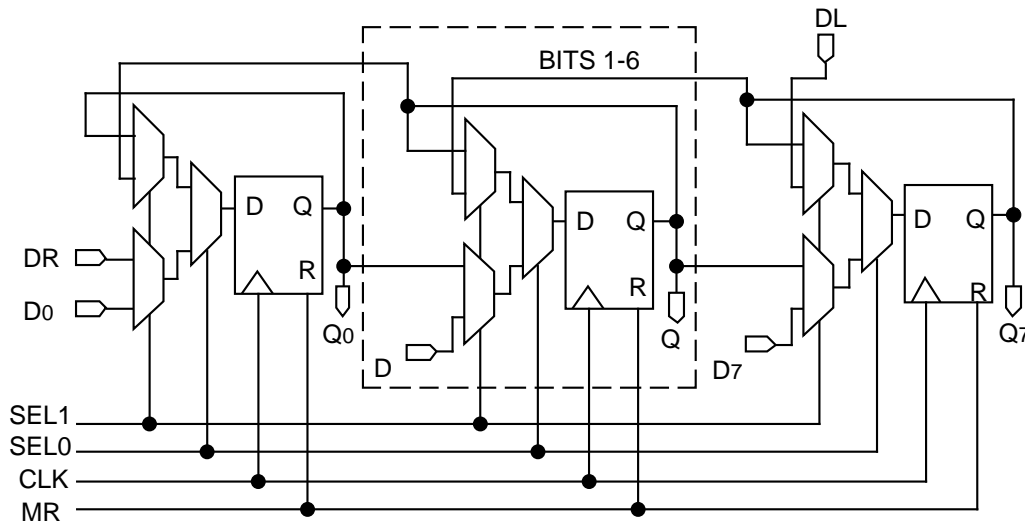
- 700MHz min. shift frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 8 bits wide
- Bi-directional
- Four selectable modes for full functionality
- Asynchronous Master Reset
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E141
- Pin-compatible with E241
- Available in 28-pin PLCC package

DESCRIPTION

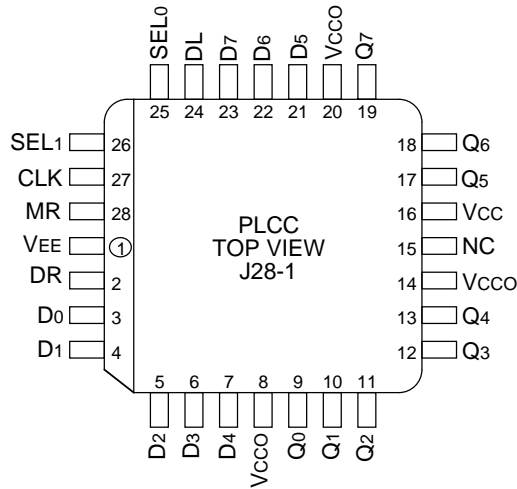
The SY10/100E141 are 8-bit, full-function shift registers designed for use in new, high-performance ECL systems. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D₀-D₇ accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The two select pins, SEL₀ and SEL₁ permit four modes of operation: Load, Hold, Shift Left and Shift Right, as shown in the Truth Table. Input data is clocked into the register on the rising clock edge after meeting the minimum set-up time. A logic HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

| Pin | Function |
|------------|----------------------|
| D0-D7 | Parallel Data Inputs |
| DL, DR | Serial Data Inputs |
| SEL0, SEL1 | Mode Select Inputs |
| CLK | Clock |
| Q0-Q7 | Data Outputs |
| MR | Master Reset |
| VCCO | Vcc to Output |

TRUTH TABLE

| Function | DL | DR | SEL0 | SEL1 | MR | CLK | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 |
|-------------|----|----|------|------|----|-----|----|----|----|----|----|----|----|----|
| Load | X | X | L | L | L | Z | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| Shift Right | X | L | L | H | L | Z | L | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 |
| | X | H | L | H | L | Z | H | L | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 |
| Shift Left | L | X | H | L | L | Z | L | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | L |
| | H | X | H | L | L | Z | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | L | H |
| Hold | X | X | H | H | L | Z | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | L | H |
| | X | X | H | H | L | Z | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | L | H |
| Reset | X | X | X | X | H | X | L | L | L | L | L | L | L | L |

DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

| Symbol | Parameter | TA = 0°C | | | TA = +25°C | | | TA = +85°C | | | Unit | Condition | |
|-----------------|----------------------|----------|------|------|------------|------|------|------------|------|------|------|-----------|-----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | | |
| I _{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA | — | |
| I _{EE} | Power Supply Current | — | 131 | 157 | — | 131 | 157 | — | 131 | 157 | mA | — | |
| | | 10E | — | 131 | 157 | — | 131 | 157 | — | 131 | | | 157 |
| | | 100E | — | 131 | 157 | — | 131 | 157 | — | 151 | | | 181 |

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

| Symbol | Parameter | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit | Condition |
|----------------------------------|--|----------------------|---------------------|-------------|------------------------|---------------------|-------------|------------------------|---------------------|-------------|------|-----------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| fSHIFT | Max. Shift Frequency | 700 | 900 | — | 700 | 900 | — | 700 | 900 | — | MHz | — |
| tPLH tPHL | Propagation Delay to Output CLK MR | 625 600 | 750 725 | 975 975 | 625 600 | 750 725 | 975 975 | 625 600 | 750 725 | 975 975 | ps | — |
| tS | Set-up Time D SEL ₀ SEL ₁ | 175 350 300 | 25 200 150 | — — — | 175 350 300 | 25 200 150 | — — — | 175 350 300 | 25 200 150 | — — — | ps | — |
| tH | Hold Time D SEL ₀ SEL ₁ | 200 100 100 | -25 -200 -150 | — — — | 200 100 100 | -25 -200 -150 | — — — | 200 100 100 | -25 -200 -150 | — — — | ps | — |
| tRR | Reset Recovery Time | 900 | 700 | — | 900 | 700 | — | 900 | 700 | — | ps | — |
| tPW | Minimum Pulse Width CLK, MR | 400 | — | — | 400 | — | — | 400 | — | — | ps | — |
| tSkew | Within-Device Skew | — | 60 | — | — | 60 | — | — | 60 | — | ps | 1 |
| t _r t _f | Rise/Fall Time 20% to 80% | 300 | 525 | 800 | 300 | 525 | 800 | 300 | 525 | 800 | ps | — |

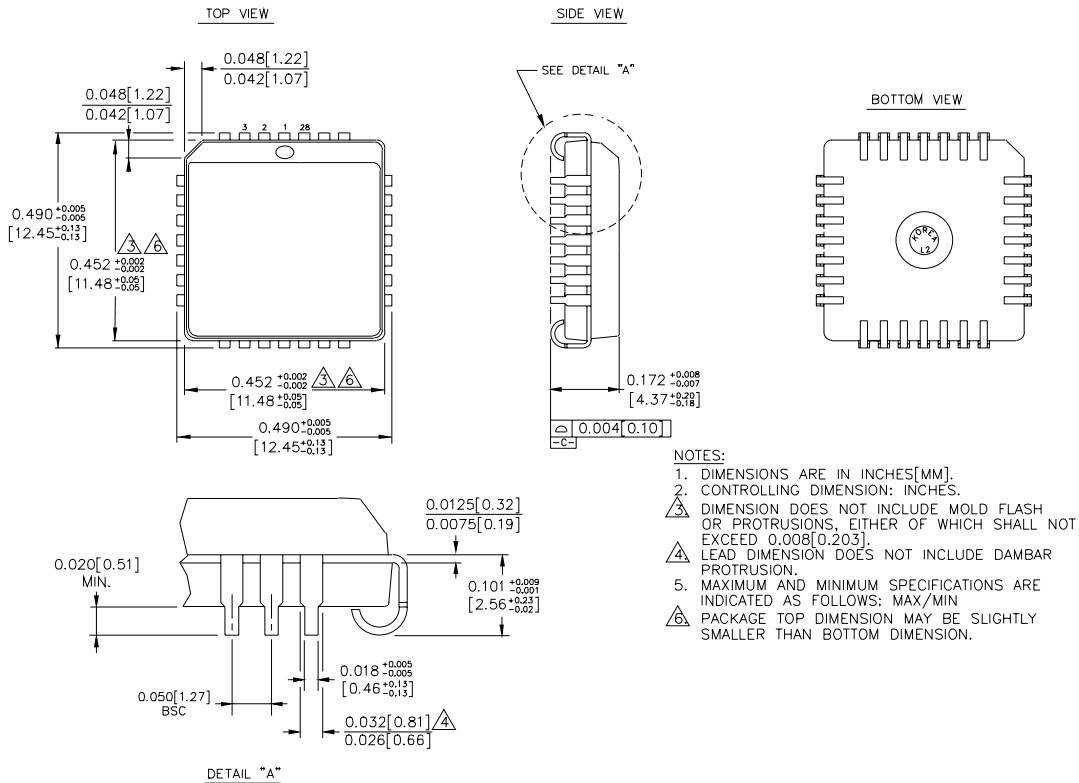
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

| Ordering Code | Package Type | Operating Range |
|---------------|--------------|-----------------|
| SY10E141JC | J28-1 | Commercial |
| SY10E141JCTR | J28-1 | Commercial |
| SY100E141JC | J28-1 | Commercial |
| SY100E141JCTR | J28-1 | Commercial |

28 LEAD PLCC (J28-1)



Rev. 03

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