

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## General Description

The MAX5387 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$ . Operating from a single +2.6V to +5.5V power supply, the device provides a low 35ppm/ $^{\circ}$ C end-to-end temperature coefficient. The device features an I<sup>2</sup>C interface.

The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5387 make the device uniquely suitable for the portable consumer market, battery backup industrial applications, and the automotive market.

The MAX5387 is specified over the automotive -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range and is available in a 14-pin TSSOP package.

## Features

- ◆ Dual, 256-Tap Linear Taper Positions
- ◆ Single +2.6V to +5.5V Supply Operation
- ◆ Low < 1 $\mu$ A Quiescent Supply Current
- ◆ 10k $\Omega$ , 50k $\Omega$ , 100k $\Omega$  End-to-End Resistance Values
- ◆ I<sup>2</sup>C-Compatible Interface
- ◆ Power-On Sets Wiper to Midscale
- ◆ -40 $^{\circ}$ C to + 125 $^{\circ}$ C Operating Temperature Range

## Applications

Low-Voltage Battery Applications  
 Portable Electronics  
 Mechanical Potentiometer Replacement  
 Offset and Gain Control  
 Adjustable Voltage References/Linear Regulators  
 Automotive Electronics

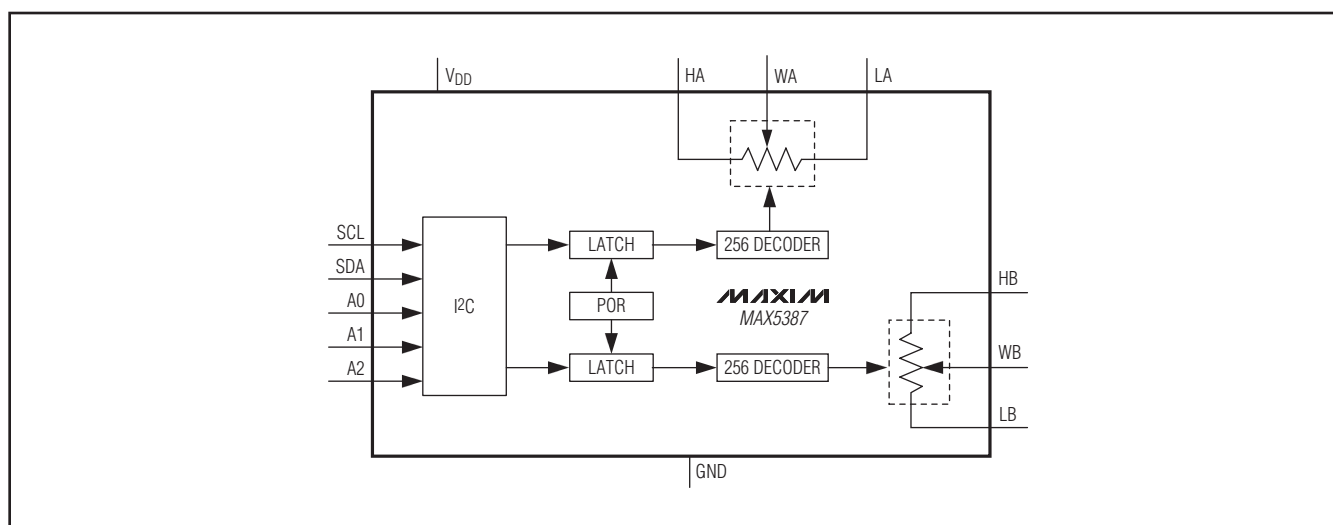
## Ordering Information

| PART         | PIN-PACKAGE | END-TO-END RESISTANCE (k $\Omega$ ) |
|--------------|-------------|-------------------------------------|
| MAX5387LAUD+ | 14 TSSOP    | 10                                  |
| MAX5387MAUD+ | 14 TSSOP    | 50                                  |
| MAX5387NAUD+ | 14 TSSOP    | 100                                 |

**Note:** All devices are specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C operating temperature range.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

## Functional Diagram



# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## ABSOLUTE MAXIMUM RATINGS

|  |   |   |                 |
|--|---|---|-----------------|
| V <sub>DD</sub> to GND .....   | -0.3V to +6V  | MAX5387N.....   | ±1mA            |
| H <sub>-</sub> , W <sub>-</sub> , L <sub>-</sub> to GND .....                | -0.3V to the lower of<br>(V <sub>DD</sub> + 0.3V) and +6V | Continuous Power Dissipation (T <sub>A</sub> = +70°C) |                 |
| All Other Pins to GND .....  | -0.3V to +6V  | 14-Pin TSSOP (derate 10mW/°C above +70°C) .....       | 796.8mW         |
| Continuous Current into H <sub>-</sub> , W <sub>-</sub> , and L <sub>-</sub> |   | Operating Temperature Range .....                     | -40°C to +125°C |
| MAX5387L .....   | ±5mA  | Junction Temperature .....                            | +150°C          |
| MAX5387M .....   | ±2mA  | Storage Temperature Range.....                        | -65°C to +150°C |
|  |   | Lead Temperature (soldering, 10s) .....               | +300°C          |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +2.6V to +5.5V, V<sub>H-</sub> = V<sub>DD</sub>, V<sub>L-</sub> = GND, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>DD</sub> = +5V, T<sub>A</sub> = +25°C.) (Note 1)

| PARAMETER  | SYMBOL                            | CONDITIONS   | MIN      | TYP  | MAX   | UNITS  |     |
|--|-----------------------------------|--|----------|------|-------|--------|-----|
| Resolution                                       | N                                 |  | 256      |      |       | Tap    |     |
| <b>DC PERFORMANCE (Voltage-Driver Mode)</b>      |                                   |  |          |      |       |        |     |
| Integral Nonlinearity                            | INL                               | (Note 2)   | -0.5     |      | +0.5  | LSB    |     |
| Differential Nonlinearity                        | DNL                               | (Note 2)   | -0.5     |      | +0.5  | LSB    |     |
| Dual Code Matching                               |                                   | Register A = register B                              | -0.5     |      | +0.5  | LSB    |     |
| Ratiometric Resistor Tempco                      |                                   | ( $\Delta V_W/V_W$ )/ $\Delta T$ ; no load           |          | +5   |       | LSB    |     |
| Full-Scale Error                                 |                                   | Code = FFH   | MAX5387L | -3   | -2.5  | LSB    |     |
|  |                                   |  | MAX5387M | -1   | -0.5  |        |     |
|  |                                   |  | MAX5387N | -0.5 | -0.25 |        |     |
| Zero-Scale Error                                 |                                   | Code = 00H   | MAX5387L |      | +2.5  | LSB    |     |
|  |                                   |  | MAX5387M |      | +0.5  |        |     |
|  |                                   |  | MAX5387N |      | +0.25 |        |     |
| <b>DC PERFORMANCE (Variable-Resistor Mode)</b>   |                                   |  |          |      |       |        |     |
| Integral Nonlinearity                            | R-INL                             | V <sub>DD</sub> > +2.6V                              | MAX5387L |      | ±1.0  | ±2.5   | LSB |
|  |                                   |  | MAX5387M |      | ±0.5  | ±1.0   |     |
|  |                                   |  | MAX5387N |      | ±0.25 | ±0.8   |     |
|  |                                   | V <sub>DD</sub> > +4.75V                             | MAX5387L |      | ±0.4  | ±1.5   |     |
|  |                                   |  | MAX5387M |      | ±0.3  | ±0.75  |     |
|  |                                   |  | MAX5387N |      | ±0.25 | ±0.5   |     |
| Differential Nonlinearity                        | R-DNL                             | V <sub>DD</sub> > 2.6V (Note 3)                      | -0.5     |      | +0.5  | LSB    |     |
| <b>DC PERFORMANCE (Resistor Characteristics)</b> |                                   |  |          |      |       |        |     |
| Wiper Resistance (Note 4)                        | R <sub>WL</sub>                   | V <sub>DD</sub> > 2.6V                               |          | 250  | 600   | Ω      |     |
|  |                                   | V <sub>DD</sub> > 4.75V                              |          | 150  | 200   |        |     |
| Terminal Capacitance                             | C <sub>H-</sub> , C <sub>L-</sub> | Measured to GND                                      |          | 10   |       | pF     |     |
| Wiper Capacitance                                | C <sub>W-</sub>                   | Measured to GND                                      |          | 50   |       | pF     |     |
| End-to-End Resistor Tempco                       | T <sub>CR</sub>                   | No load  |          | 35   |       | ppm/°C |     |
| End-to-End Resistor Tolerance                    | $\Delta R_{HL}$                   | Wiper not connected                                  | -25      |      | +25   | %      |     |
| <b>AC PERFORMANCE</b>                            |                                   |  |          |      |       |        |     |
| Crosstalk  |                                   | (Note 5)   |          | -90  |       | dB     |     |
| -3dB Bandwidth                                   | BW                                | Code = 08H,<br>10pF load,<br>V <sub>DD</sub> = +2.6V | MAX5387L |      | 600   | kHz    |     |
|  |                                   |  | MAX5387M |      | 150   |        |     |
|  |                                   |  | MAX5387N |      | 75    |        |     |

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +2.6V$  to  $+5.5V$ ,  $V_{H\_} = V_{DD}$ ,  $V_{L\_} = GND$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $V_{DD} = +5V$ ,  $T_A = +25^{\circ}C$ .) (Note 1)

| PARAMETER                                       | SYMBOL              | CONDITIONS                                  | MIN | TYP   | MAX | UNITS             |
|---|---------------------|---|-----|-------|-----|-------------------|
| Total Harmonic Distortion Plus Noise            | THD+N               | Measured at W; $V_{H\_} = 1V_{RMS}$ at 1kHz |     | 0.015 |     | %                 |
| Wiper Settling Time (Note 6)                    | ts                  | MAX5387L                                    |     | 300   |     | ns                |
|   |                     | MAX5387M                                    |     | 1000  |     |                   |
|   |                     | MAX5387N                                    |     | 2000  |     |                   |
| <b>POWER SUPPLIES</b>                           |                     |   |     |       |     |                   |
| Supply-Voltage Range                            | $V_{DD}$            |   | 2.6 |       | 5.5 | V                 |
| Standby Current                                 |                     | Digital inputs = $V_{DD}$ or GND            |     | 1     |     | $\mu A$           |
| <b>DIGITAL INPUTS</b>                           |                     |   |     |       |     |                   |
| Minimum Input High Voltage                      | $V_{IH}$            |   | 70  |       |     | % $\times V_{DD}$ |
| Maximum Input Low Voltage                       | $V_{IL}$            |   |     |       | 30  | % $\times V_{DD}$ |
| Input Leakage Current                           |                     |   | -1  |       | +1  | $\mu A$           |
| Input Capacitance                               |                     |   |     | 5     |     | pF                |
| <b>TIMING CHARACTERISTICS (Notes 7, 8)</b>      |                     |   |     |       |     |                   |
| Maximum SCL Frequency                           | f <sub>SCL</sub>    |   |     |       | 400 | kHz               |
| Setup Time for START Condition                  | t <sub>SU:STA</sub> |   | 0.6 |       |     | $\mu s$           |
| Hold Time for START Condition                   | t <sub>HD:STA</sub> |   | 0.6 |       |     | $\mu s$           |
| SCL High Time                                   | t <sub>HIGH</sub>   |   | 0.6 |       |     | $\mu s$           |
| SCL Low Time                                    | t <sub>LOW</sub>    |   | 1.3 |       |     | $\mu s$           |
| Data Setup Time                                 | t <sub>SU:DAT</sub> |   | 100 |       |     | ns                |
| Data Hold Time                                  | t <sub>HD:DAT</sub> |   | 0   |       |     | $\mu s$           |
| SDA, SCL Rise Time                              | t <sub>R</sub>      |   |     |       | 0.3 | $\mu s$           |
| SDA, SCL Fall                                   | t <sub>F</sub>      |   |     |       | 0.3 | $\mu s$           |
| Setup Time for STOP Condition                   | t <sub>SU:STO</sub> |   | 0.6 |       |     | $\mu s$           |
| Bus Free Time Between STOP and START Conditions | t <sub>BUF</sub>    | Minimum power-up rate = $0.2V/\mu s$        | 1.3 |       |     | $\mu s$           |
| Pulse-Suppressed Spike Width                    | t <sub>SP</sub>     |   |     |       | 50  | ns                |
| Capacitive Load for Each Bus                    | C <sub>B</sub>      |   |     |       | 400 | pF                |

**Note 1:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Specifications overtemperature limits are guaranteed by design and characterization.

**Note 2:** DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with  $H\_ = V_{DD}$  and  $L\_ = 0V$ . The wiper terminal is unloaded and measured with an ideal voltmeter.

**Note 3:** R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with the potentiometer configured as a variable resistor.  $H\_$  is unconnected and  $L\_ = GND$ . For  $V_{DD} = +5V$ , the wiper terminal is driven with a source current of  $400\mu A$  for the  $10k\Omega$  configuration,  $80\mu A$  for the  $50k\Omega$  configuration, and  $40\mu A$  for the  $100k\Omega$  configuration. For  $V_{DD} = +2.6V$ , the wiper terminal is driven with a source current of  $200\mu A$  for the  $10k\Omega$  configuration,  $40\mu A$  for the  $50k\Omega$  configuration, and  $20\mu A$  for the  $100k\Omega$  configuration.

**Note 4:** The wiper resistance is the worst value measured by injecting the currents given in Note 3 into  $W\_$  with  $L\_ = GND$ .  $R_W = (V_W - V_H)/I_W$ .

**Note 5:** Drive  $H_A$  with a 1kHz GND to  $V_{DD}$  amplitude tone.  $L_A = L_B = GND$ . No load.  $W_B$  is at midscale with a 10pF load. Measure  $W_B$ .

**Note 6:** The wiper settling time is the worst-case 0 to 50% rise time, measured between tap 0 and tap 127.  $H\_ = V_{DD}$ ,  $L\_ = GND$ , and the wiper terminal is loaded with 10pF capacitance to ground.

**Note 7:** Digital timing is guaranteed by design and characterization, not production tested.

**Note 8:** The SCL clock period includes rise and fall times ( $t_R = t_F$ ). All digital input signals are specified with  $t_R = t_F = 2ns$  and timed from a voltage level of  $(V_{IL} + V_{IH})/2$ .

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

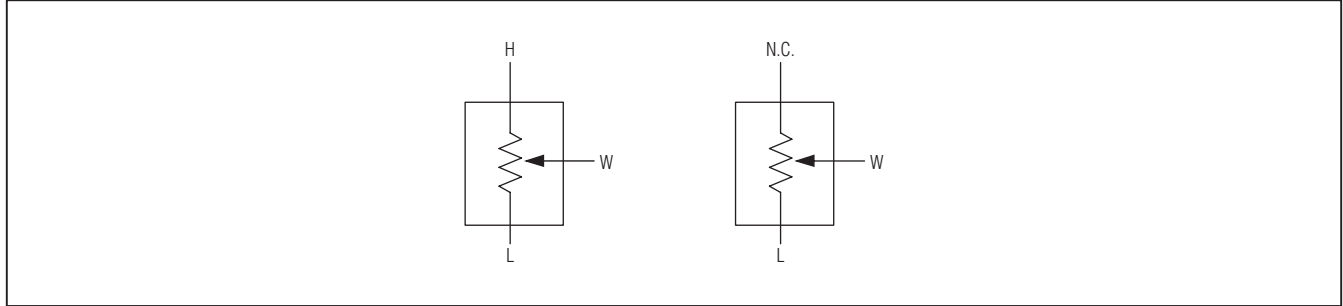
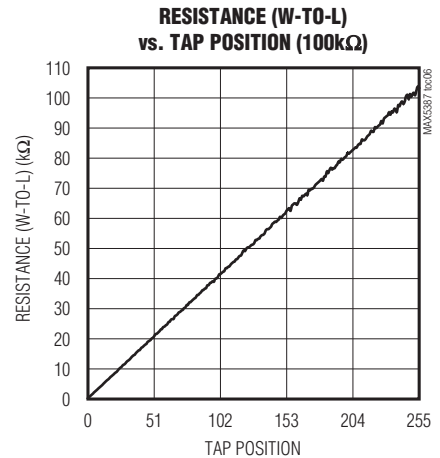
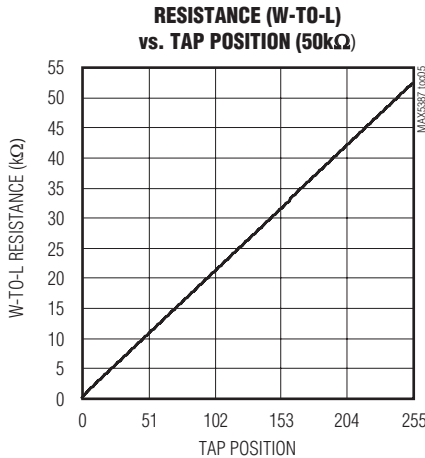
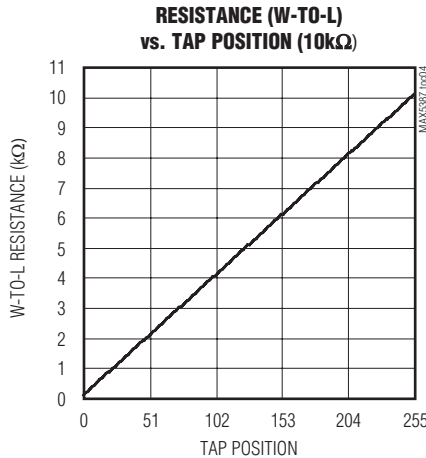
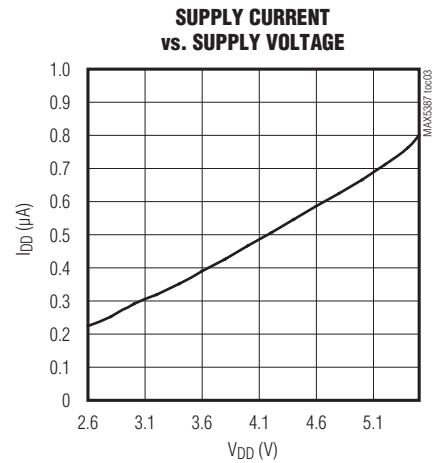
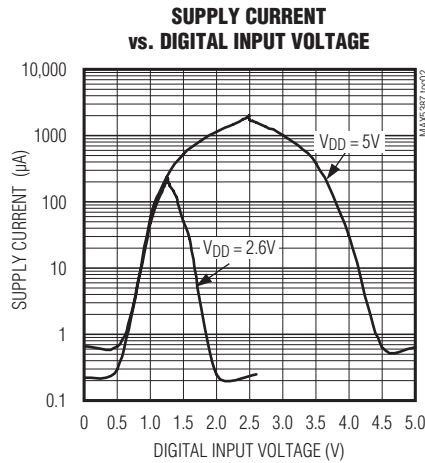
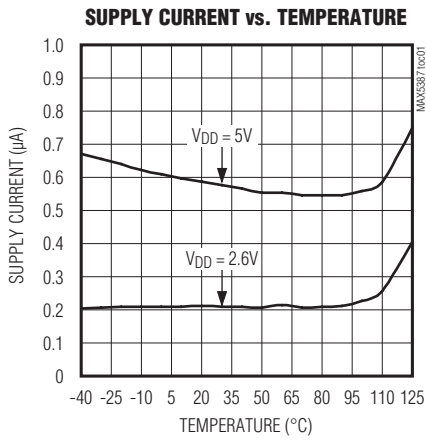


Figure 1. Voltage-Divider and Variable Resistor Configurations

## Typical Operating Characteristics

( $V_{DD} = 5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

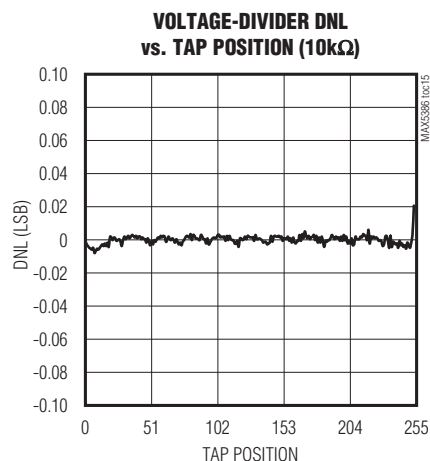
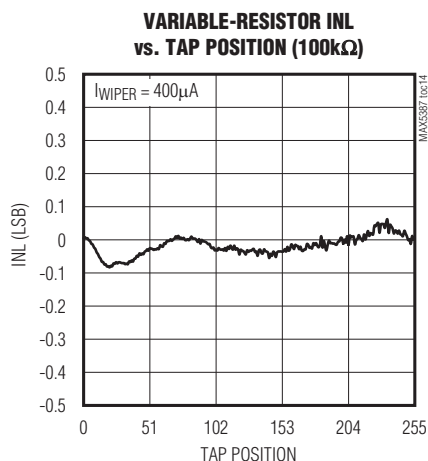
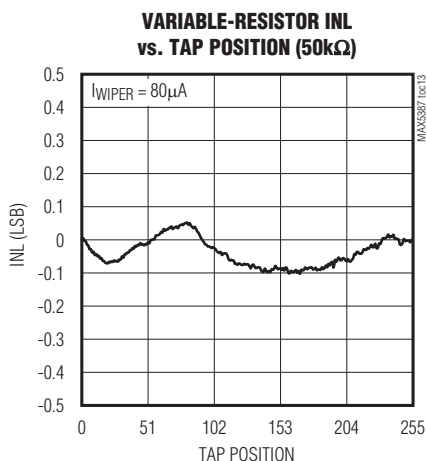
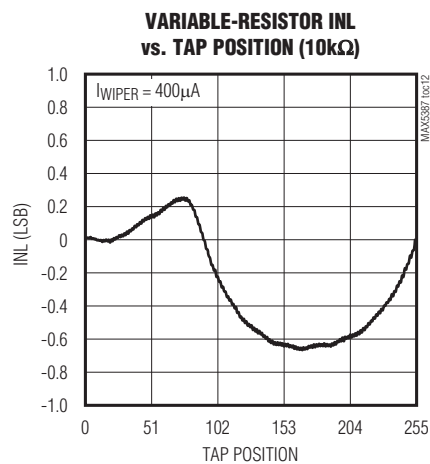
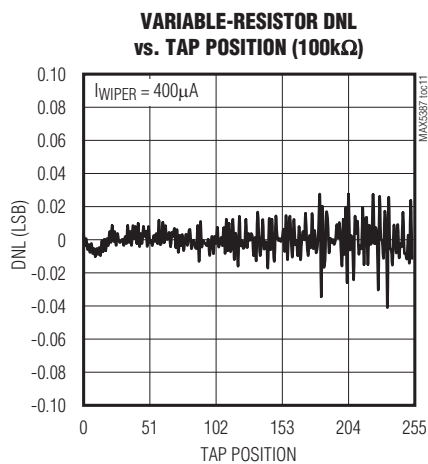
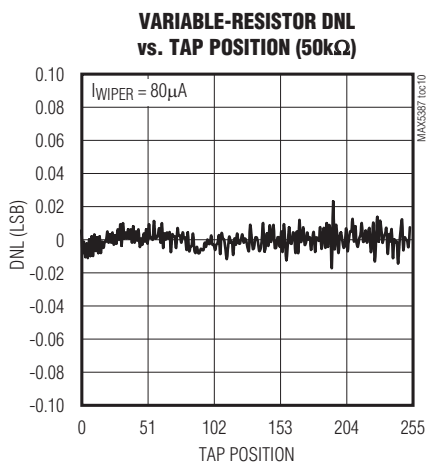
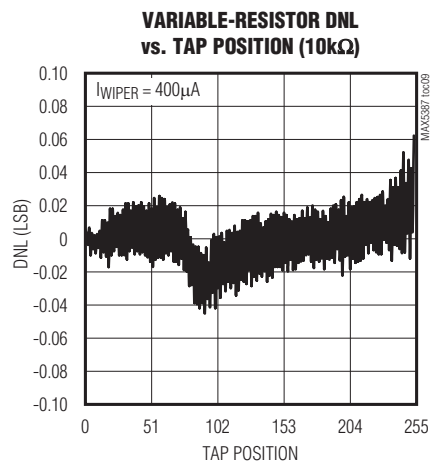
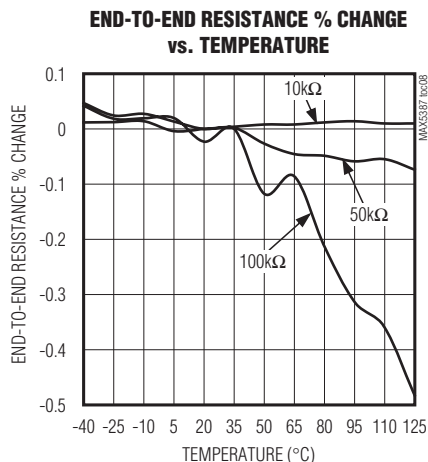
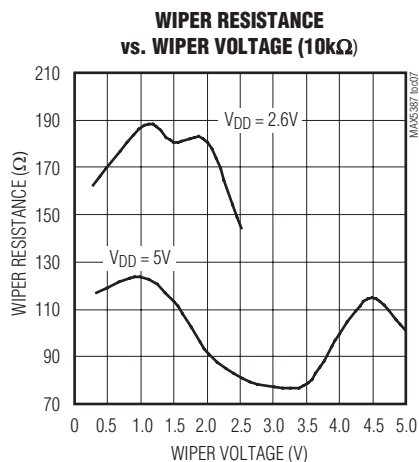


# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Typical Operating Characteristics (continued)

( $V_{DD} = 5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

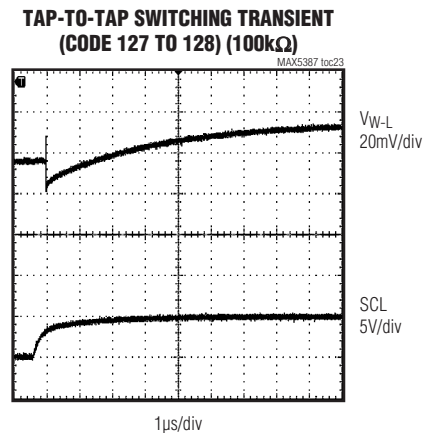
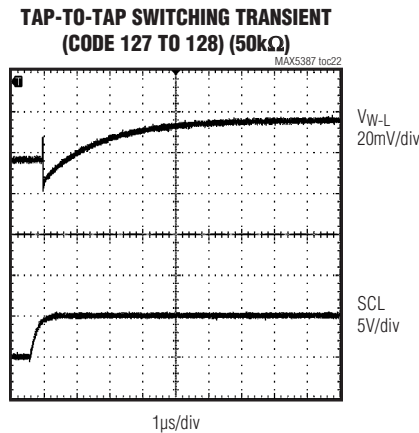
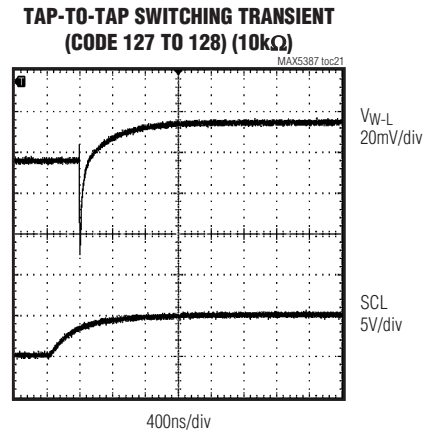
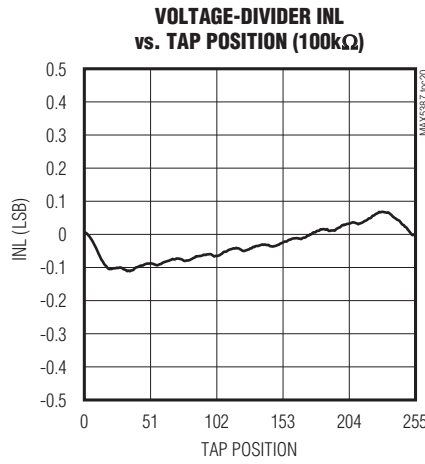
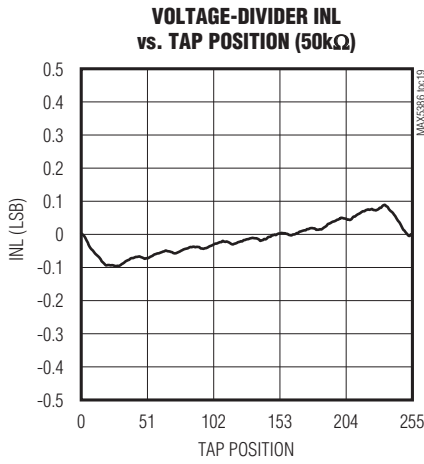
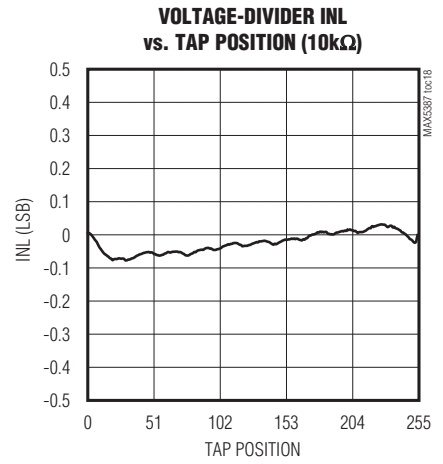
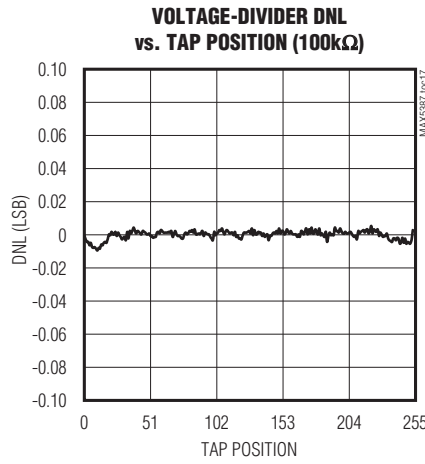
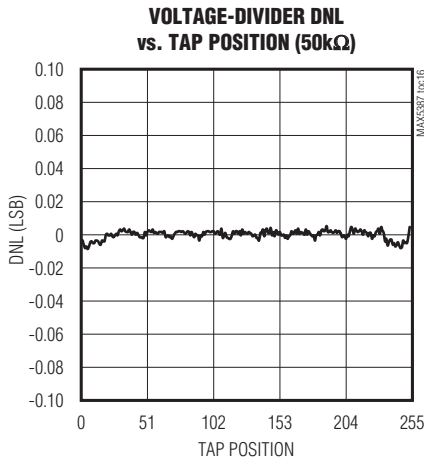
MAX5387



# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Typical Operating Characteristics (continued)

( $V_{DD} = 5V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



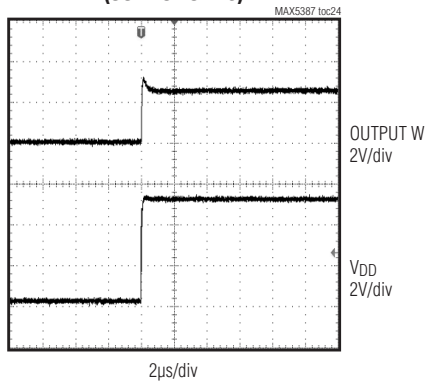
# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Typical Operating Characteristics (continued)

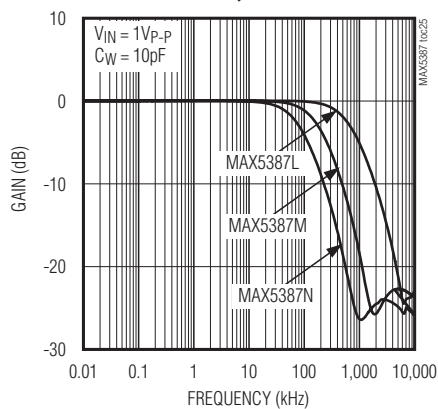
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MAX5387

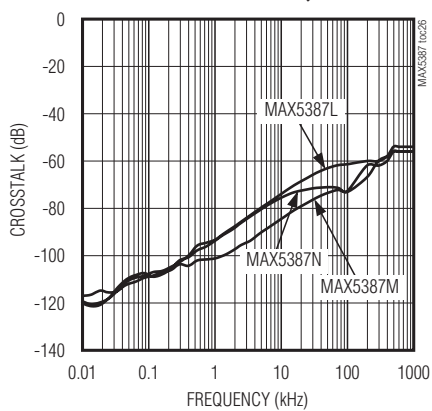
**MAX5387 POWER-ON WIPER TRANSIENT (CODE 0 TO 128)**



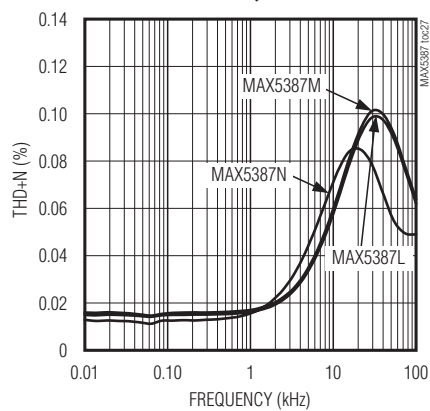
**MIDSCALE FREQUENCY RESPONSE**



**CROSSTALK vs. FREQUENCY**

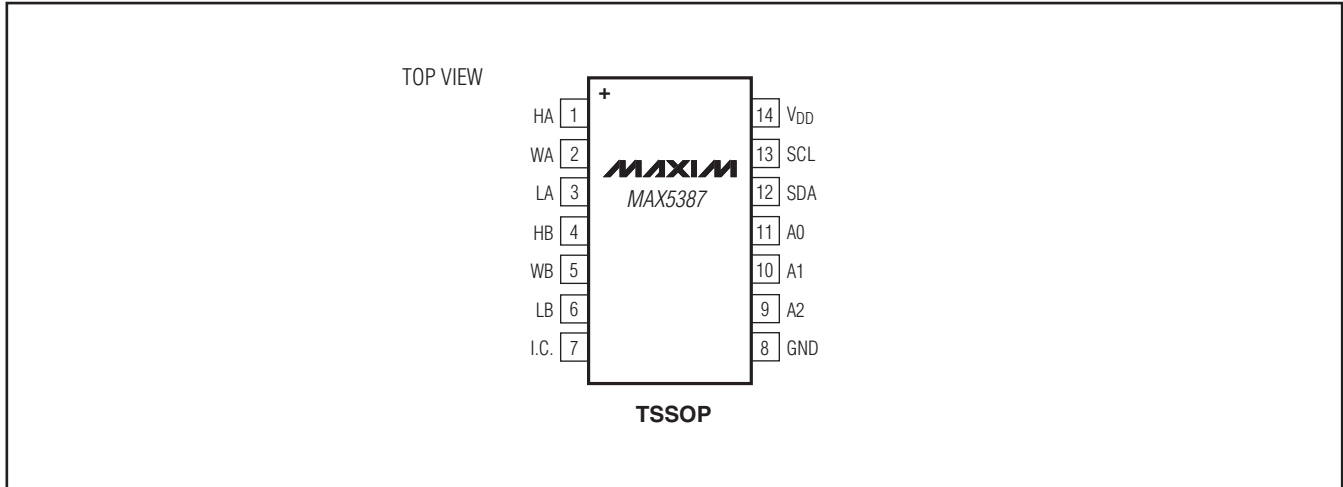


**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Pin Configuration



## Pin Description

| PIN | NAME            | FUNCTION   |
|-----|-----------------|--|
| 1   | HA              | Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA. |
| 2   | WA              | Resistor A Wiper Terminal  |
| 3   | LA              | Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA.  |
| 4   | HB              | Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB. |
| 5   | WB              | Resistor B Wiper Terminal  |
| 6   | LB              | Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB.  |
| 7   | I.C.            | Internally Connected. Connect to GND.  |
| 8   | GND             | Ground   |
| 9   | A2              | Address Input 2. Connect to V <sub>DD</sub> or GND.  |
| 10  | A1              | Address Input 1. Connect to V <sub>DD</sub> or GND.  |
| 11  | A0              | Address Input 0. Connect to V <sub>DD</sub> or GND.  |
| 12  | SDA             | I <sup>2</sup> C-Compatible Serial-Data Input/Output. A pullup resistor is required.   |
| 13  | SCL             | I <sup>2</sup> C-Compatible Serial-Clock Input. A pullup resistor is required.   |
| 14  | V <sub>DD</sub> | Power-Supply Input. Bypass V <sub>DD</sub> to GND with a 0.1μF capacitor close to the device.                                  |



# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Detailed Description

The MAX5387 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10k $\Omega$ , 50k $\Omega$ , and 100k $\Omega$ . The potentiometer consists of 255 fixed resistors in series between terminals H<sub>-</sub> and L<sub>-</sub>. The potentiometer wiper, W<sub>-</sub>, is programmable to access any one of the 256 tap points on the resistor string.

The potentiometers are programmable independently of each other. The MAX5387 features an I<sup>2</sup>C interface.

## I<sup>2</sup>C Digital Interface

The I<sup>2</sup>C interface contains a shift register that decodes the command and address bytes, routing the data to the appropriate control registers. Data written to a control register immediately updates the wiper position. Wipers A and B power up in midposition, D[7:0] = 80H.

## Serial Addressing

The MAX5387 operates as a slave device that receives data through an I<sup>2</sup>C-/SMBus™-compatible 2-wire serial interface. The interface uses a serial-data access (SDA) line and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A

master, typically a microcontroller, initiates all data transfers to the MAX5387, and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX5387 SDA line operates as both an input and an open-drain output. The SDA line requires a pullup resistor, typically 4.7k $\Omega$ . The MAX5387 SCL line operates only as an input. The SCL line requires a pullup resistor (typically 4.7k $\Omega$ ) if there are multiple masters on the 2-wire interface, or if the master in a single-master system provides an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 3) sent by a master, followed by the MAX5387 7-bit slave address plus the NOP/W bit (Figure 6), 1 command byte and 1 data byte, and finally a STOP (P) condition (Figure 3).

## START and STOP Conditions

SCL and SDA remain high when the interface is inactive. A master controller signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. The master controller issues a STOP condition by transitioning the SDA from low to high while SCL is high, after finishing communicating with the slave. The bus is then free for another transmission.

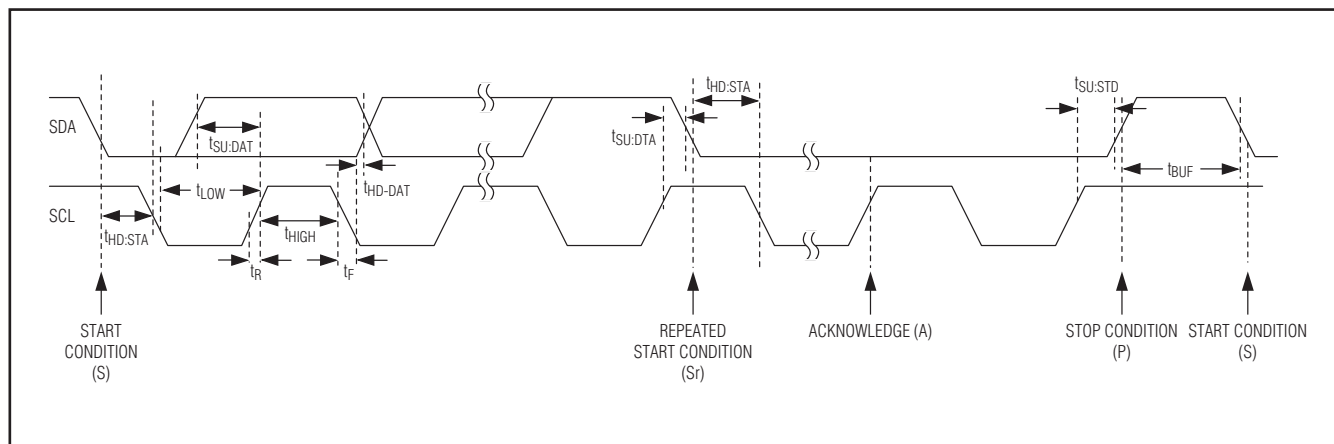


Figure 2. I<sup>2</sup>C Serial Interface Timing Diagram

SMBus is a trademark of Intel Corp.

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

### Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high. See Figure 4.

### Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data. See Figure 5. Each byte transferred requires a total of nine bits. The master controller generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line remains stable low during the high period of the clock pulse.

### Slave Address

The MAX5387 includes a 7-bit slave address (Figure 6). The 8th bit following the 7th bit of the slave address is the NOP/ $\overline{W}$  bit. Set the NOP/ $\overline{W}$  bit low for a write command and high for a no-operation command. The device does not support readback.

The device provides three address inputs (A0, A1, and A2), allowing up to eight devices to share a common bus (Table 1). The first 4 bits (MSBs) of the factory-set slave addresses are always 0101. A2, A1, and A0 set the next 3 bits of the slave address. Connect each address input to VDD or GND. Each device must have a unique address to share a common bus.

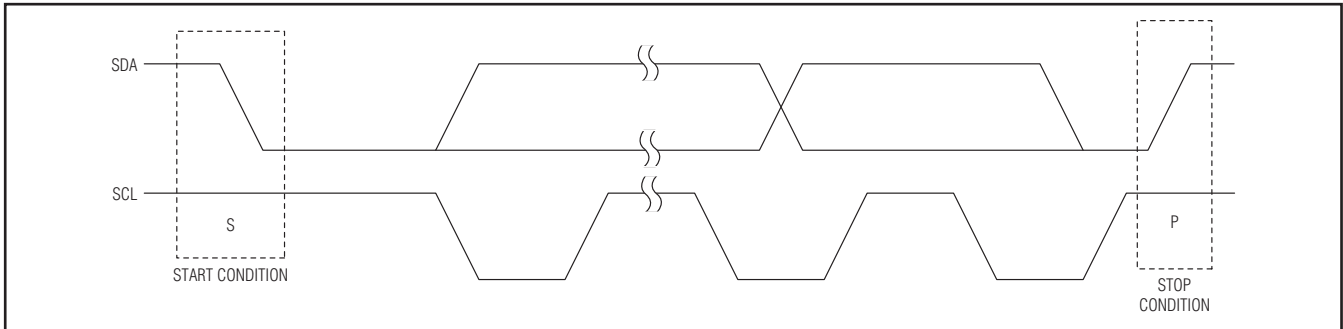


Figure 3. START and STOP Conditions

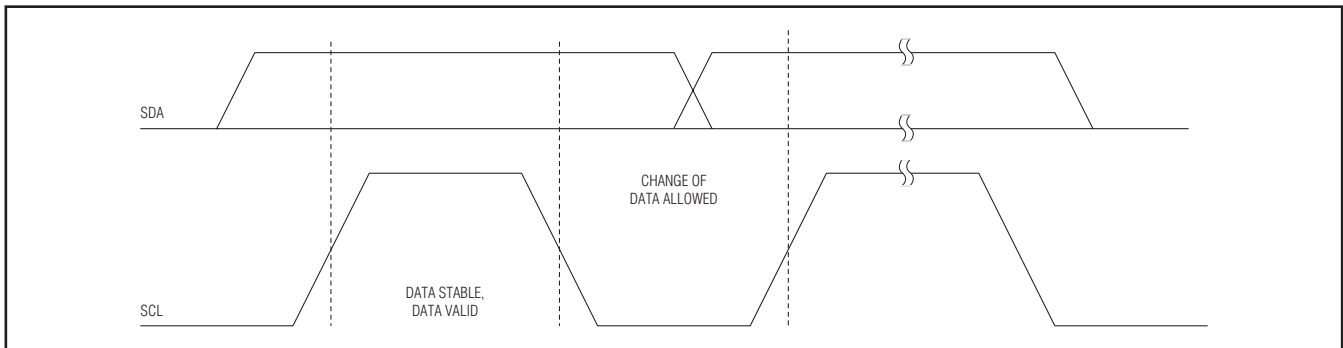


Figure 4. Bit Transfer

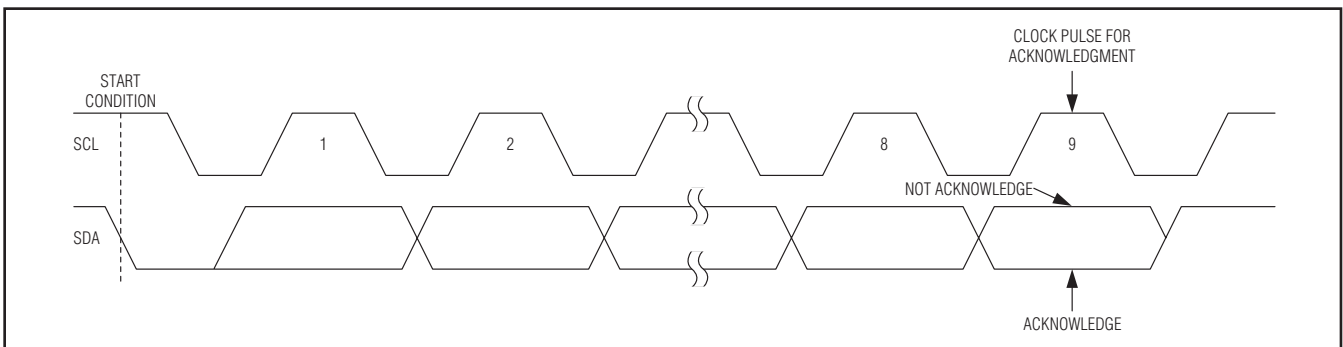


Figure 5. Acknowledge

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

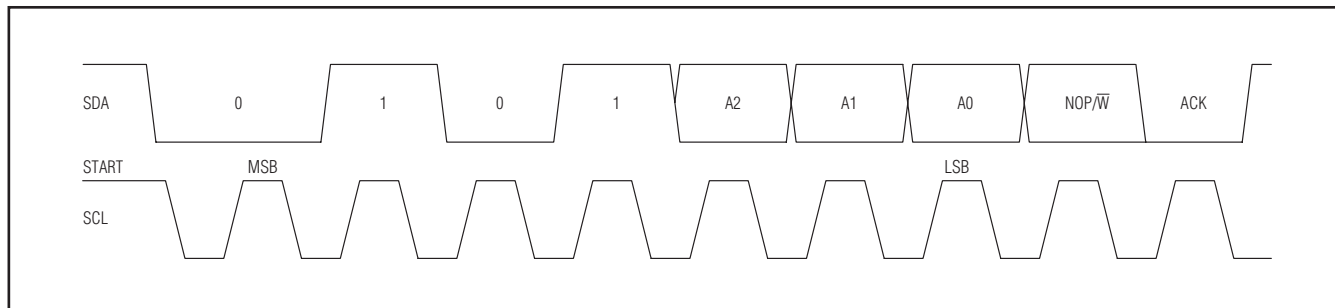


Figure 6. Slave Address

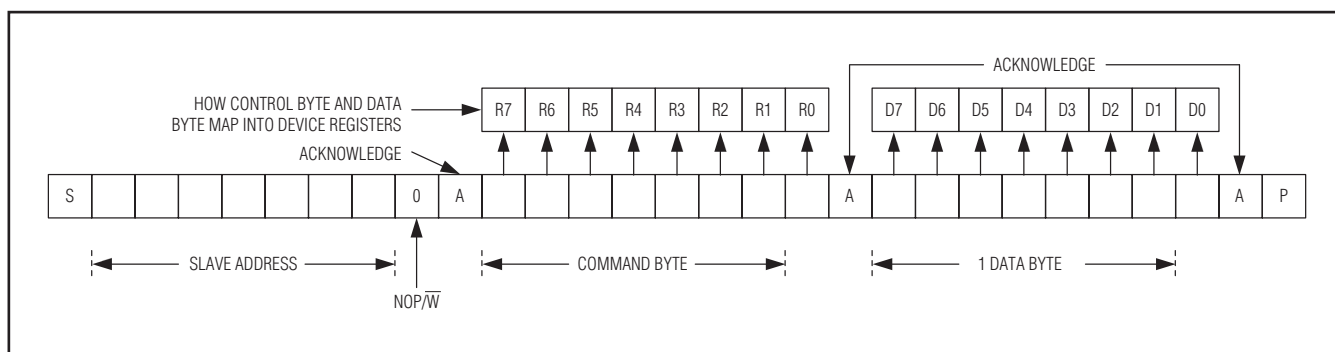


Figure 7. Command and Single Data Byte Received

### Message Format for Writing

Write to the devices by transmitting the device's slave address with  $\text{NOP}/\overline{\text{W}}$  (eighth bit) set to zero, followed by at least 2 bytes of information. The first byte of information is the command byte. The second byte is the data byte. The data byte goes into the internal register of the device as selected by the command byte (Figure 7 and Table 2).

### Command Byte

Use the command byte to select the destination of the wiper data. See Table 2.

### Command Descriptions

**REG A:** The data byte writes to register A and the wiper of potentiometer A moves to the appropriate position.  $\text{D}[7:0]$  indicates the position of the wiper.  $\text{D}[7:0] = 00\text{h}$

moves the wiper to the position closest to LA.  $\text{D}[7:0] = \text{FFh}$  moves the wiper to the position closest to HA.  $\text{D}[7:0]$  is  $80\text{h}$  following power-on.

Table 1. Slave Addresses

| ADDRESS INPUTS  |                 |                 | SLAVE ADDRESS |
|-----------------|-----------------|-----------------|---------------|
| A2              | A1              | A0              |               |
| GND             | GND             | GND             | 0101000       |
| GND             | GND             | V <sub>DD</sub> | 0101001       |
| GND             | V <sub>DD</sub> | GND             | 0101010       |
| GND             | V <sub>DD</sub> | V <sub>DD</sub> | 0101011       |
| V <sub>DD</sub> | GND             | GND             | 0101100       |
| V <sub>DD</sub> | GND             | V <sub>DD</sub> | 0101101       |
| V <sub>DD</sub> | V <sub>DD</sub> | GND             | 0101110       |
| V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | 0101111       |

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

Table 2. I<sup>2</sup>C Command Byte Summary

| SCL CYCLE NO. | START (S) | ADDRESS BYTE |    |    |    |    |    |    |           | COMMAND BYTE |    |    |    |    |    |    |    | DATA BYTE |         |    |    |    |    |    |    | STOP (P) |    |         |    |
|---------------|-----------|--------------|----|----|----|----|----|----|-----------|--------------|----|----|----|----|----|----|----|-----------|---------|----|----|----|----|----|----|----------|----|---------|----|
|               |           | 1            | 2  | 3  | 4  | 5  | 6  | 7  | 8         | 9            | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17        | 18      | 19 | 20 | 21 | 22 | 23 | 24 |          | 25 | 26      | 27 |
|               |           | A6           | A5 | A4 | A3 | A2 | A1 | A0 | $\bar{W}$ | ACK (A)      | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0        | ACK (A) | D7 | D6 | D5 | D4 | D3 | D2 | D1       | D0 | ACK (A) |    |
| REG A         |           | 0            | 1  | 0  | 1  | A2 | A1 | A0 | 0         |              | 0  | 0  | 0  | 1  | 0  | 0  | 0  | 1         |         | D7 | D6 | D5 | D4 | D3 | D2 | D1       | D0 |         |    |
| REG B         |           | 0            | 1  | 0  | 1  | A2 | A1 | A0 | 0         |              | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 0         |         | D7 | D6 | D5 | D4 | D3 | D2 | D1       | D0 |         |    |
| REGS A AND B  |           | 0            | 1  | 0  | 1  | A2 | A1 | A0 | 0         |              | 0  | 0  | 0  | 1  | 0  | 0  | 1  | 1         |         | D7 | D6 | D5 | D4 | D3 | D2 | D1       | D0 |         |    |

**REG B:** The data byte writes to register B and the wiper of potentiometer B moves to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wiper to the position closest to LB. D[7:0] = FFh moves the wiper to the position closest to HB. D[7:0] is 80h following power-on.

**REGS A and B:** The data byte writes to registers A and B and the wipers of potentiometers A and B move to the appropriate position. D[7:0] indicates the position of the wiper. D[7:0] = 00h moves the wipers to the position closest to L<sub>-</sub>. D[7:0] = FFh moves the wipers to the position closest to H<sub>-</sub>. D[7:0] is 80h following power-on.

## Applications Information

### Variable Gain Amplifier

Figure 8 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 9 shows a potentiometer adjusting the gain of an inverting amplifier.

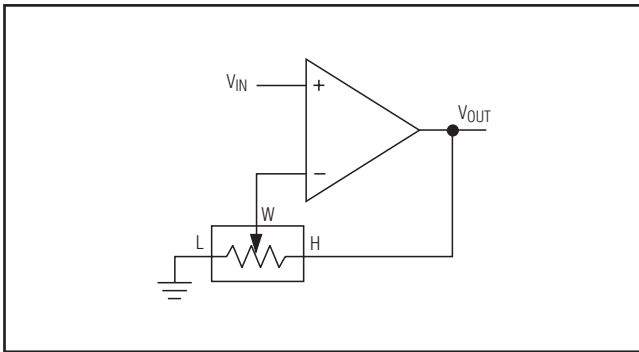


Figure 8. Variable Gain Noninverting Amplifier

### Adjustable Dual Regulator

Figure 10 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

### Adjustable Voltage Reference

Figure 11 shows an adjustable voltage reference circuit using a potentiometer as a voltage-divider.

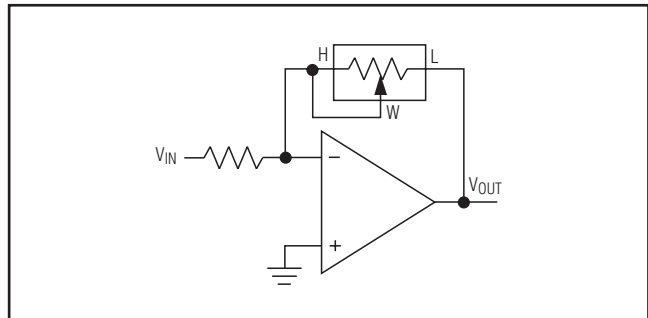


Figure 9. Variable Gain Inverting Amplifier

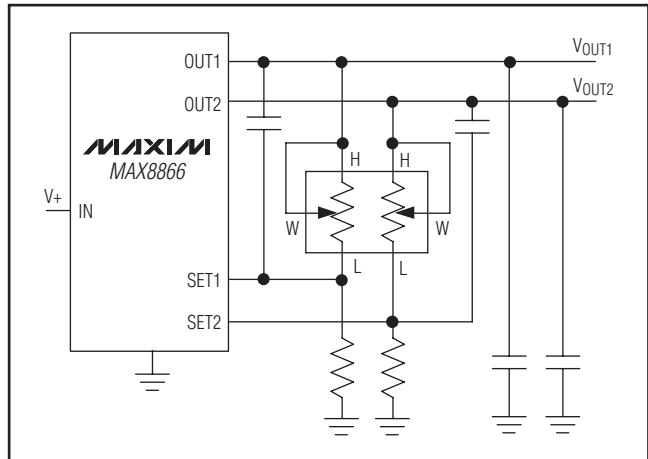


Figure 10. Adjustable Dual Linear Regulator

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

## Variable Gain Current to Voltage Converter

Figure 12 shows a variable gain current to voltage converter using a potentiometer as a variable resistor.

## LCD Bias Control

Figure 13 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

Figure 14 shows a positive LCD bias control circuit using a potentiometer as a variable resistor.

## Programmable Filter

Figure 15 shows a programmable filter using a dual potentiometer.

## Offset-Voltage Adjustment Circuit

Figure 16 shows an offset-voltage adjustment circuit using a dual potentiometer.

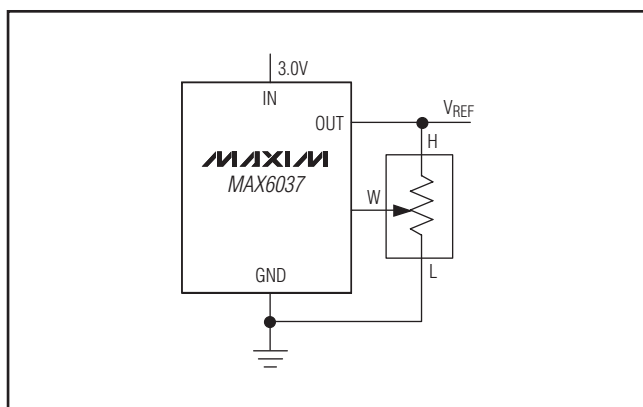


Figure 11. Adjustable Voltage Reference

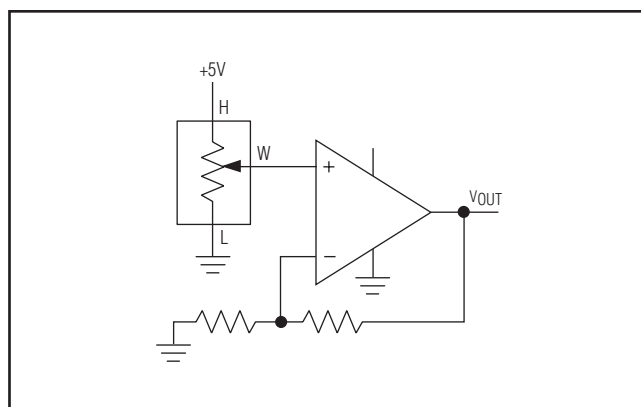


Figure 13. Positive LCD Bias Control Using a Voltage-Divider

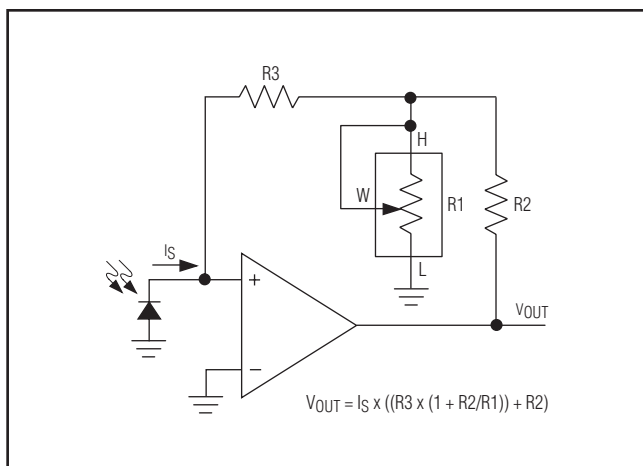


Figure 12. Variable Gain I-to-V Converter

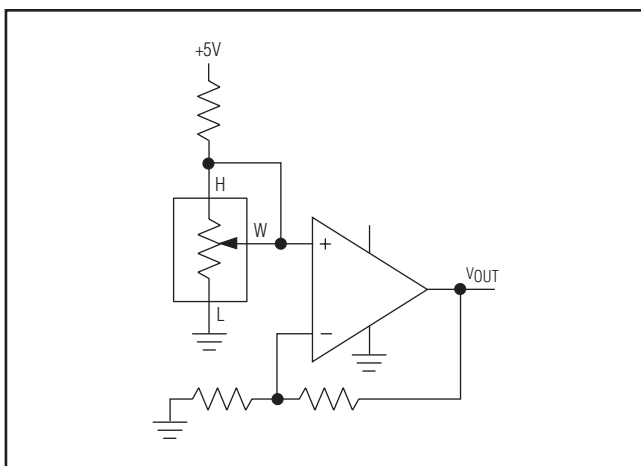


Figure 14. Positive LCD Bias Control Using a Variable Resistor

# Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

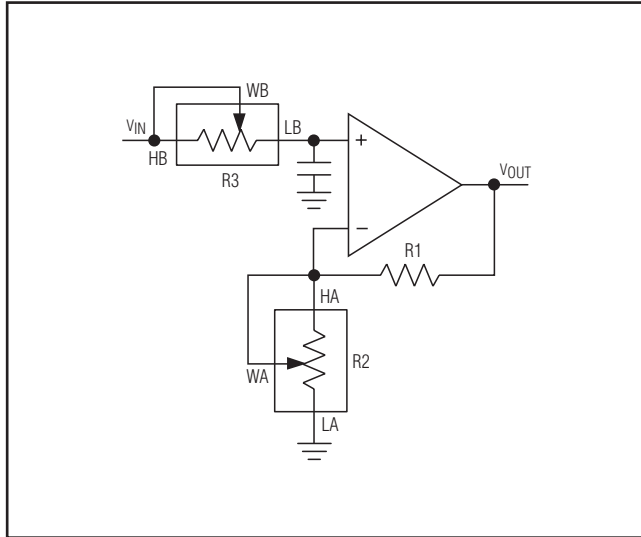


Figure 15. Programmable Filter

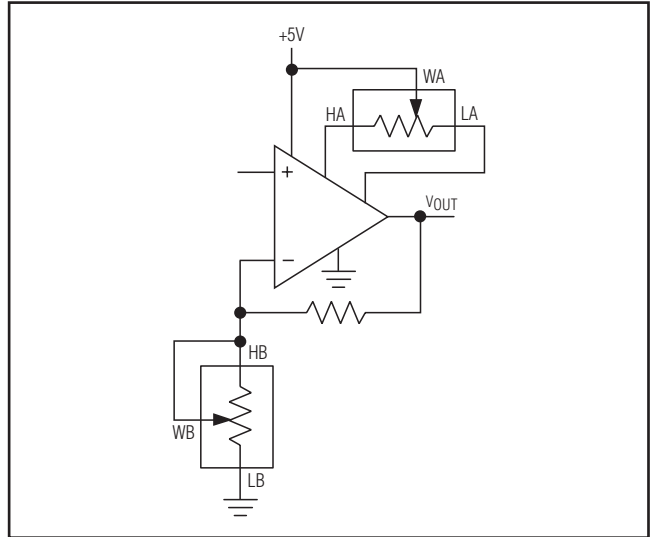


Figure 16. Offset-Voltage Adjustment Circuit

## Process Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 14 TSSOP     | U14+1        | <a href="#">21-0066</a> |

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