19-0856; Rev 0; 7/07

EVALUATION KIT AVAILABLE

Quad PCI Express, Hot-Plug Controllers

General Description

The MAX5959/MAX5960 quad hot-plug controllers are designed for PCI Express® (PCIe) applications. These devices provide hot-plug control for the main 12V, 3.3V, and 3.3V auxiliary supplies of four PCIe slots. The MAX5959/MAX5960s' logic inputs/outputs allow interfacing directly with the system hot-plug management controller or through an SMBus™ with an external I/O expander such as the MAX7313. An integrated debounced attention switch and present-detect signals simplify system design.

The MAX5959/MAX5960 drive eight external n-channel MOSFETs to control the 12V and 3.3V main outputs. The 3.3V auxiliary outputs are controlled through 0.2Ω n-channel MOSFETs. Internal charge pumps provide the gate drive for the 12V outputs while the gate drive of the 3.3V output is driven by the 12V input supply clamped to 5.5V above the respective 3.3V main supply rail. The 3.3V auxiliary outputs are completely independent from the main outputs with their own charge pumps.

At power-up, the MAX5959/MAX5960 keep all the MOSFETs off until the supplies rise above their respective undervoltage lockout (UVLO) thresholds. Upon a turn-on command, the MAX5959/MAX5960 enhance the external and internal MOSFETs slowly with a constant gate current to limit the power-supply inrush current.

The MAX5959/MAX5960 actively limit the current to protect all outputs at all times and shut down if an overcurrent condition persists longer than the programmable overcurrent timeout. After an overcurrent or overtemperature fault condition, the MAX5959L/MAX5960L latch off while the MAX5959A/MAX5960A automatically restart after a restart time delay. The MAX5959/MAX5960 are offered in latch-off or autorestart versions (see the *Selector Guide*).

The MAX5959/MAX5960 are available in an 80-pin TQFP package and operate over the -40°C to +85°C temperature range.

Applications

Servers

Desktop Mobile Server Platforms

Workstations

Features

- **PCIe Compliant**
- **Hot Swap 12V, 3.3V, and 3.3V Auxiliary for 4 PCIe Slots**
- **Integrated Power MOSFETs for Auxiliary Supply Rails**
- **Controls di/dt and dV/dt**
- **Active Current Limiting Protects Against Overcurrent/Short-Circuit Conditions**
- **Programmable Current-Limit Timeout**
- **$\overline{\text{PWRGD}}$ Signal Outputs with Programmable Power-On Reset (POR) (160ms Default)**
- **Latched $\overline{\text{FAULT}}$ Signal Output After Overcurrent or Overtemperature Fault**
- **Attention Switch Inputs/Outputs with 4ms Debounce**
- **Present-Detect Inputs**
- **Force-On Inputs Facilitate Testing/Debug**
- **Thermal Shutdown**
- **Allow Control Through SMBus with an I/O Expander**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5959AECS+	-40°C to +85°C	80 TQFP	C80-1
MAX5959LECS+	-40°C to +85°C	80 TQFP	C80-1
MAX5960AECS+	-40°C to +85°C	80 TQFP	C80-1
MAX5960LECS+	-40°C to +85°C	80 TQFP	C80-1

+Denotes a lead-free package.

Pin Configuration and Typical Application Circuit appear at end of data sheet.

PCI Express is a registered trademark of PCI-SIG Corp.
SMBus is a trademark of Intel Corp.

Selector Guide

PART	LATCH OFF	AUTORESTART	GUARANTEED AUX CURRENT (mA)
MAX5959AECS+		√	375
MAX5959LECS+	√		375
MAX5960AECS+		√	550
MAX5960LECS+	√		550

Quad PCI Express, Hot-Plug Controllers

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
12VIN.....-0.3V to +14V
12G_.....-0.3V to (V_{12VIN} + 6V)
12S_+, 12S_-, 3.3G_.....-0.3V to (V_{12VIN} + 0.3V)
3.3VAUXIN, ON_, $\overline{FAULT\_}$, $\overline{PWRGD\_}$.....-0.3V to +6V
PGND.....-0.3V to +0.3V
All Other Pins.....-0.3V to ($V_{3.3VAUXIN}$ + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
80-Pin TQFP (derate 23.3mW/°C above +70°C).....1860mW
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{12VIN} = V_{12S_+} = V_{12S_-} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
12V SUPPLY (MAIN)						
12V Supply Input-Voltage Range	V_{12VIN}		10.8	12	13.2	V
12V Undervoltage Lockout	V_{12UVLO}	V_{12VIN} rising	9.5	10	10.5	V
		Hysteresis		0.1		
12V Undervoltage Lockout Deglitch Time	$t_{DEG,UVLO}$	V_{12IN} falling below V_{12UVLO} to UVLO assertion		30		µs
12V Supply Current	I_{12VIN}	V_{12VIN} = 13.2V		1	2.5	mA
12VIN CONTROL						
12VIN Current-Limit Threshold (V_{12S+} - V_{12S-})	V_{12ILIM}		49	54	59	mV
12G_ Gate Charge Current	$I_{12G,CHG}$	$V_{12G\_}$ = GND	4	5	6	µA
12G_ Gate Discharge Current	$I_{12G\_,DIS}$	Normal turn-off, ON_ = GND, $V_{12G\_}$ = 2V	50	150	250	µA
		Output short-circuit condition, strong gate pulldown to regulation, (V_{12S+} - V_{12S-}) ≥ 1V, $V_{12G\_}$ = 5V	60	120	200	mA
12G_ Gate High Voltage ($V_{12G\_}$ - V_{12VIN})	$V_{12G,H}$	$I_{12G\_}$ = 1µA	4.8	5.3	5.8	V
12G_ Threshold Voltage for $\overline{PWRGD\_}$ Assertion	V_{PGTH12}	Referred to V_{12VIN}, $I_{12G\_}$ = 1µA (Note 2)	3	4	4.8	V
12S_- Input Bias Current					1	µA
12S_+ Input Bias Current				10	30	µA
3.3V SUPPLY (MAIN)						
3.3V Supply Voltage Range	$V_{3.3S\_+}$		3.0	3.3	3.6	V
Undervoltage Lockout (Note 3)		3.3SA+ rising	2.50	2.65	2.78	V
		Hysteresis		30		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{12VIN} = V_{12S_+} = V_{12S_-} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
3.3V CONTROL							
3.3V Current-Limit Threshold ($V_{3.3S\_+}$ - $V_{3.3S\_-}$)	$V_{3.3ILIM}$			17	20	23	mV
3.3G_ Gate Charge Current	$I_{3.3G\_,CHG}$	$V_{3.3G\_}$ = GND		4	5	6	µA
3.3G_ Gate Discharge Current	$I_{3.3G\_, DIS}$	Normal turn-off, ON_ = GND, $V_{3.3G\_}$ = 2V		50	150	250	µA
		Output short-circuit condition, strong gate pulldown to regulation, $V_{3.3S\_+}$ - $V_{3.3S\_-}$ ≥ 1V, $V_{3.3G\_}$ = 5V		90	150	250	mA
3.3G_ Gate High Voltage ($V_{3.3G\_}$ - $V_{3.3S\_+}$)	$V_{3.3G\_H}$	I_{SOURCE} = 1µA		4.5	5.5	6.8	V
3.3G_ Threshold Voltage for $\overline{PWRGD\_}$ Assertion	$V_{PGTH3.3}$	Referred to $V_{3.3AUXIN}$, $I_{3.3G\_}$ = 1µA (Note 2)		3	4	4.5	V
3.3S_- Input Bias Current						1	µA
3.3S_+ Input Bias Current					20	60	µA
3.3V AUXILIARY SUPPLY							
3.3VAUXIN Supply Input Voltage Range	$V_{3.3AUXIN}$			3.0	3.3	3.6	V
3.3VAUXIN Undervoltage Lockout	$V_{3.3VAUXUVLO}$	$V_{3.3VAUXIN}$ rising		2.50	2.65	2.78	V
		Hysteresis			30		mV
3.3VAUXIN Supply Current		$V_{3.3VAUXIN}$ = 3.6V			2.5	5	mA
3.3VAUXIN to 3.3VAUXO_ Maximum Dropout		$I_{3.3VAUXO\_}$ = 550mA (MAX5960)				280	mV
		$I_{3.3VAUXO\_}$ = 375mA (MAX5959)				225	
3.3VAUXO_ Current-Limit Threshold		3.3VAUXO_ shorted to GND	MAX5959	376	450	564	mA
			MAX5960	560	700	850	
3.3VAUXO_ Threshold for $\overline{PWRGD\_}$ Assertion (V3.3VAUXIN - V3.3VAUXO_)	$V_{PGTH3.3AUX}$	(Note 2)				400	mV
LOGIC SIGNALS							
Input-Logic Threshold (ON_, $\overline{FON\_}$, AUXON_, $\overline{PRES\text{-}DET\_}$, INPUT_)		Rising edge		1.0		2.0	V
		Hysteresis			25		mV
Input Bias Current (ON_, AUXON_, INPUT_)						1	µA
$\overline{FON\_}$, $\overline{PRES\text{-}DET\_}$ Internal				25	50	75	kΩ
ON_, AUXON_ High-to-Low Deglitch Time					4		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{12VIN} = V_{12S_+} = V_{12S_-} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = 12G_ = 3.3G_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND, T_A = T_J = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 1)

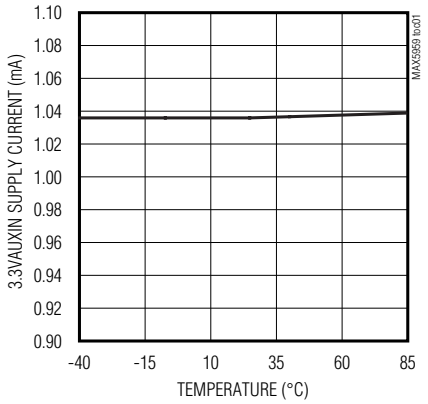
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{PRES\text{-}DET\_}$ High-to-Low Deglitch Time	t_{DEG}		3	5	7	ms
$\overline{PWRGD\_}$ Power-On Reset Deglitch Time (Note 2)	t_{POR_HL}	V_{PORADJ} = GND			1	µs
		PORADJ = unconnected	90	160	250	ms
		R_{PORADJ} = 20kΩ	35	55	75	
		R_{PORADJ} = 100kΩ	145	265	380	
		R_{PORADJ} = 200kΩ		530		
$\overline{PWRGD\_}$ Low-to-High Deglitch Time	t_{POR_LH}			4		µs
$\overline{PWRGD\_}$, $\overline{FAULT\_}$ Output Low Voltage		I_{SINK} = 2mA			0.1	V
		I_{SINK} = 30mA			0.8	
$\overline{PWRGD\_}$, $\overline{FAULT\_}$ Output High Leakage Current		$\overline{PWRGD\_}$, $\overline{FAULT\_}$ = 5.5V			1	µA
$\overline{FAULT\_}$ Timeout	t_{FAULT}	TIM = open	5.5	11	17	ms
		R_{TIM} = 15kΩ	1.4	2.6	3.8	
		R_{TIM} = 120kΩ	12	22	32	
		R_{TIM} = 300kΩ		53		
$\overline{FAULT\_}$ Timeout During Startup	t_{SU}			2 x t_{FAULT}		ms
Autorestart Delay Time	$t_{RESTART}$			64 x t_{FAULT}		ms
Fault Reset Minimum Pulse Width	t_{RESET}	(Note 4)		100		µs
Thermal Shutdown Threshold	t_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis				20		
OUT_ Debounce Time	t_{DBC}		2.6	4.4	6.2	ms
OUT_ Voltage High		I_{SOURCE} = 2mA	$V_{3.3AUXIN}$ - 0.3		$V_{3.3AUXIN}$	V

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: $\overline{PWRGD\_}$ asserts a time t_{POR_HL} after V_{PGTH12}, $V_{PGTH3.3}$, and $V_{PGTH3.3AUX}$ conditions are met.
Note 3: The UVLO for the 3.3V supply is sensed at 3.3SA+.
Note 4: This is the time that ON_ or AUXON_ must stay low when resetting a fault condition.

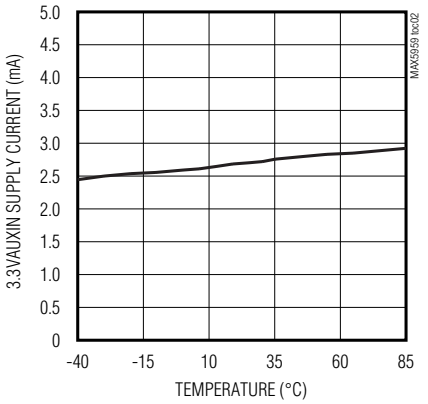
Typical Operating Characteristics

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

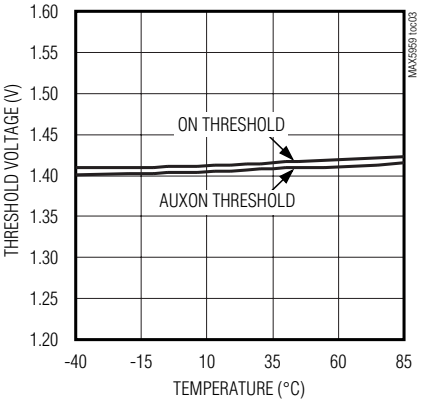
12V INPUT SUPPLY CURRENT vs. TEMPERATURE



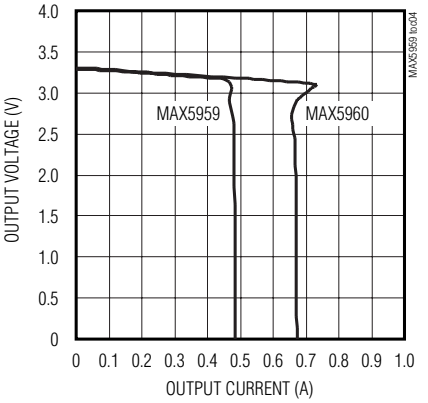
3.3VAUXIN SUPPLY CURRENT vs. TEMPERATURE



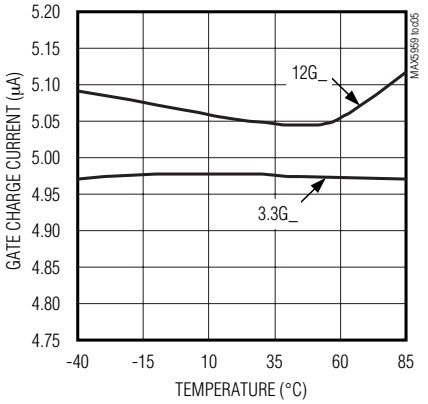
ON AND AUXON LOW-TO-HIGH THRESHOLD VOLTAGE vs. TEMPERATURE



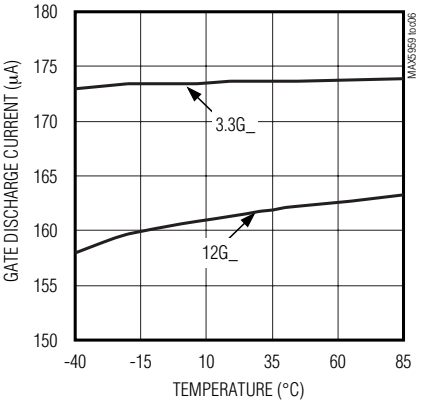
3.3VAUXO_ OUTPUT VOLTAGE vs. OUTPUT CURRENT



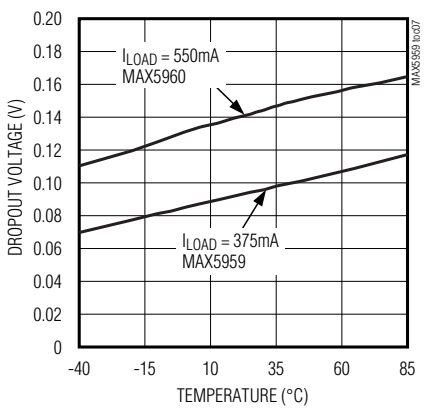
12G_ AND 3.3G_ GATE CHARGE CURRENT vs. TEMPERATURE



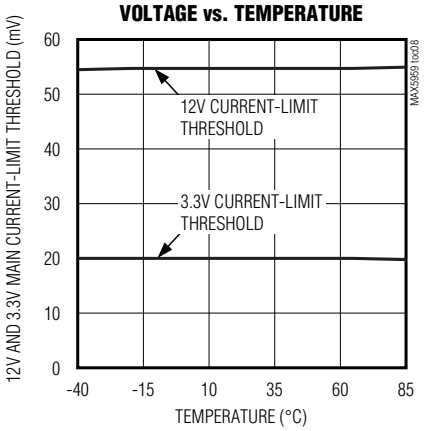
12G_ AND 3.3G_ GATE DISCHARGE CURRENT vs. TEMPERATURE



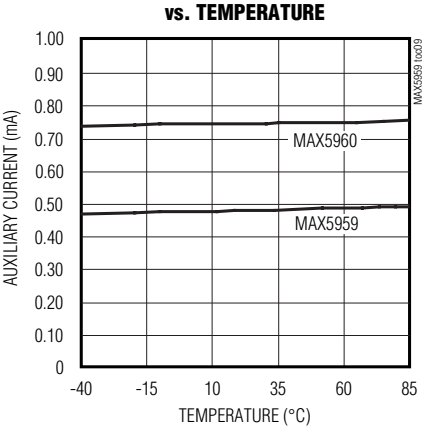
3.3VAUX INTERNAL SWITCH MAXIMUM DROPOUT vs. TEMPERATURE



12V AND 3.3V CURRENT-LIMIT THRESHOLD VOLTAGE vs. TEMPERATURE



AUXILIARY CURRENT LIMIT vs. TEMPERATURE

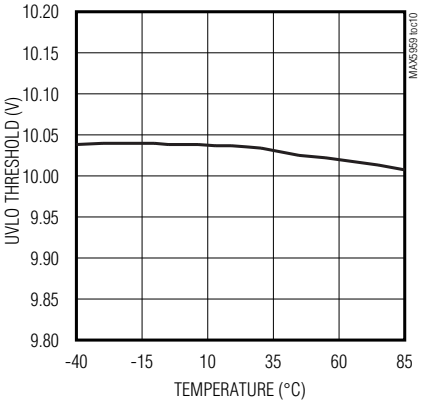


Quad PCI Express, Hot-Plug Controllers

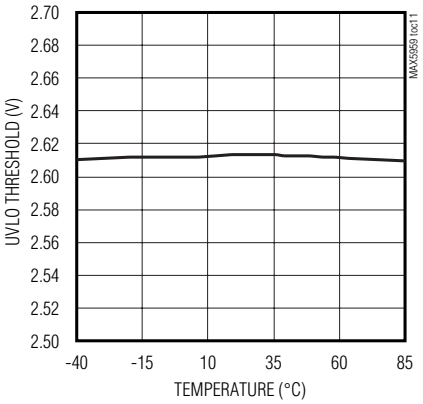
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

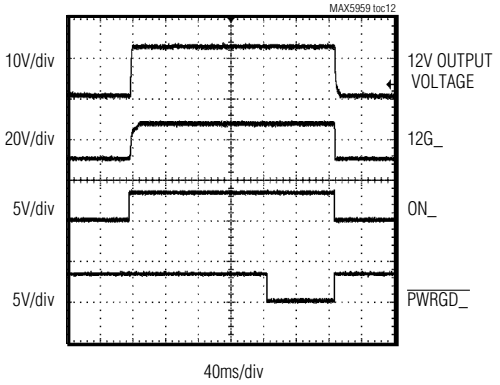
12V UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



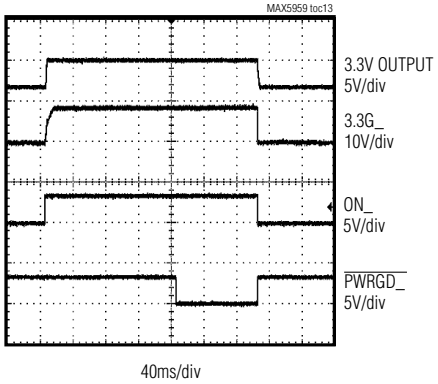
3.3VAUXON UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



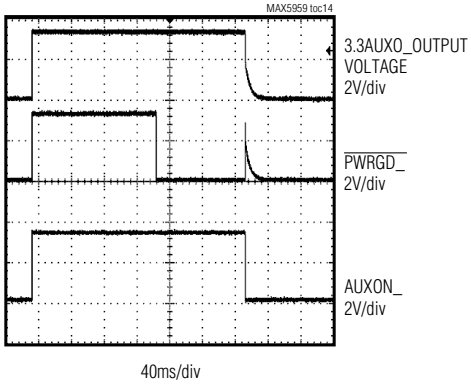
12V TURN-ON/OFF TIME



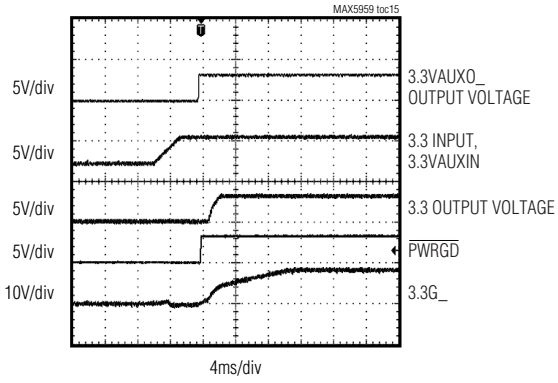
3.3V TURN-ON/OFF TIME



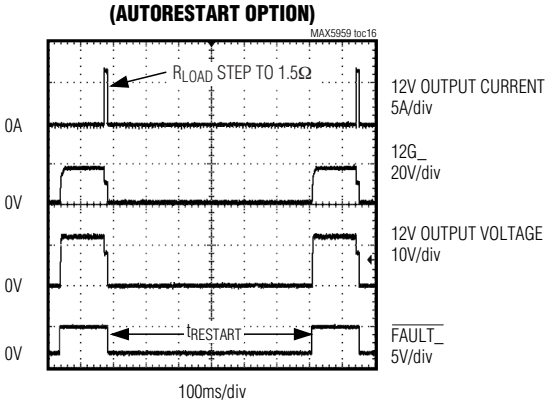
3.3V AUXILIARY TURN-ON/OFF TIME



TURN-ON DELAY 3.3V OUTPUT AND 3.3V AUXILIARY OUTPUT



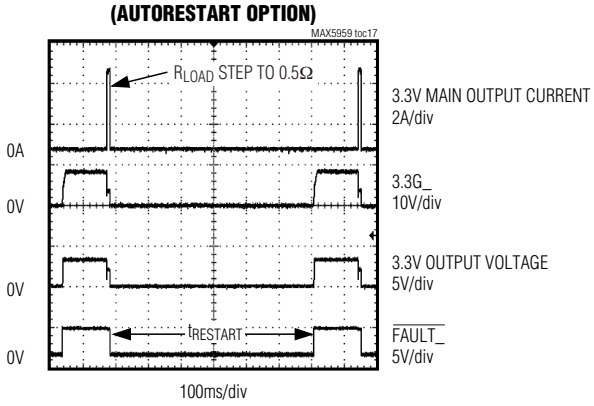
FAULT CONDITION ON 12V MAIN OUTPUT (AUTORESTART OPTION)



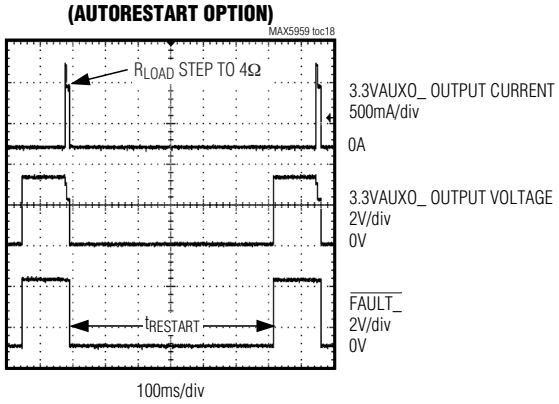
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

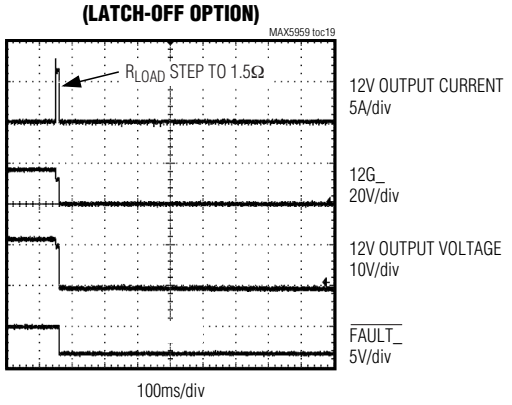
FAULT CONDITION ON 3.3V MAIN OUTPUT (AUTORESTART OPTION)



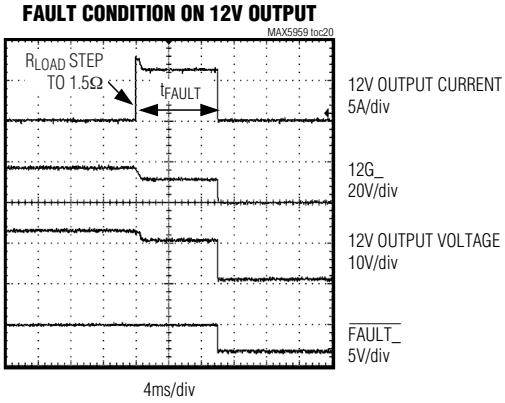
FAULT CONDITION ON AUXILIARY OUTPUT (AUTORESTART OPTION)



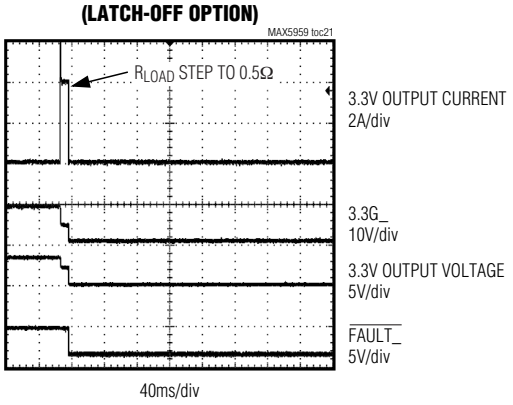
FAULT CONDITION ON 12V MAIN OUTPUT (LATCH-OFF OPTION)



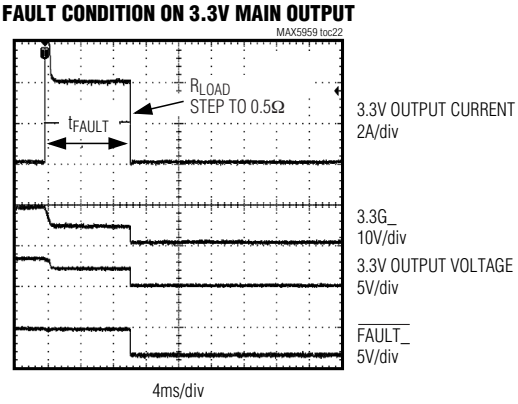
FAULT CONDITION ON 12V OUTPUT



FAULT CONDITION ON 3.3V MAIN OUTPUT (LATCH-OFF OPTION)



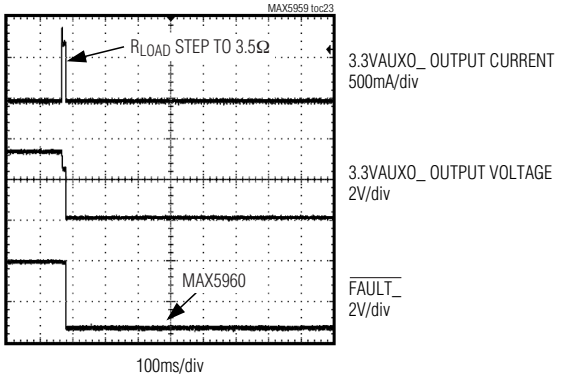
FAULT CONDITION ON 3.3V MAIN OUTPUT



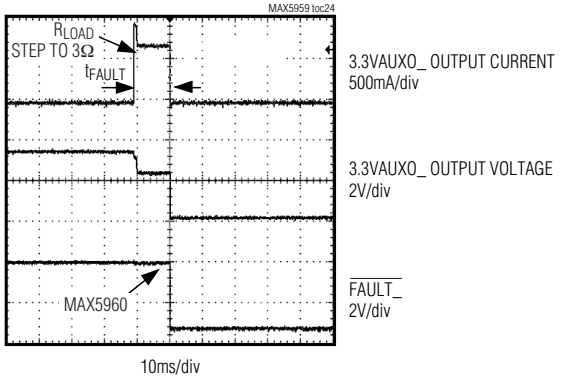
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

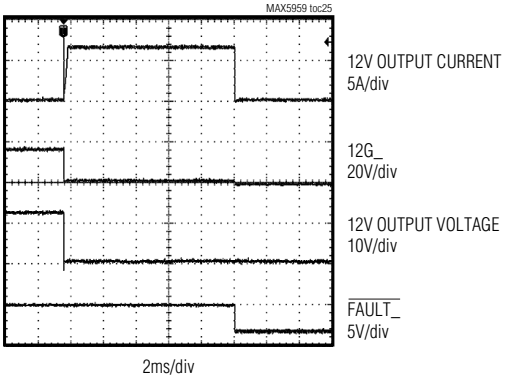
FAULT CONDITION ON AUXILIARY OUTPUT (LATCH-OFF OPTION)



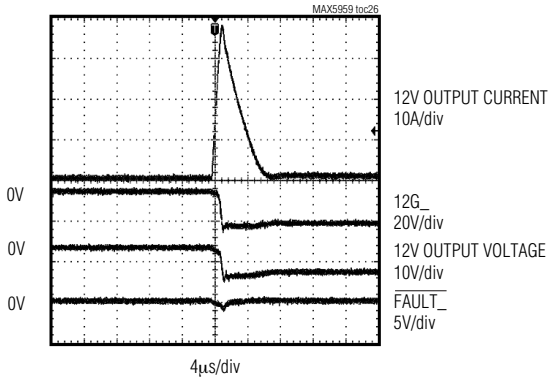
FAULT CONDITION ON AUXILIARY OUTPUT



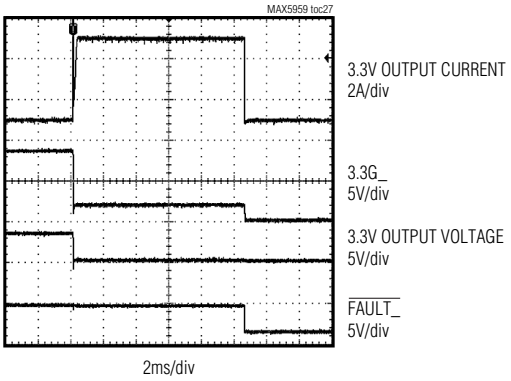
SHORT CIRCUIT ON 12V MAIN OUTPUT



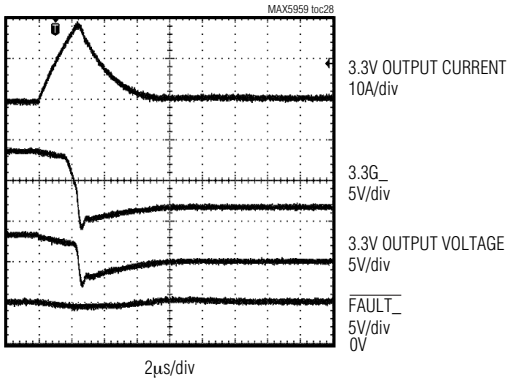
SHORT CIRCUIT ON 12V MAIN OUTPUT



SHORT CIRCUIT ON 3.3V MAIN OUTPUT



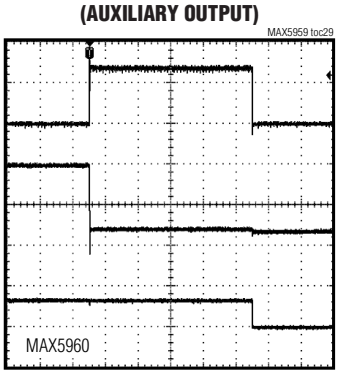
SHORT CIRCUIT ON 3.3V MAIN OUTPUT



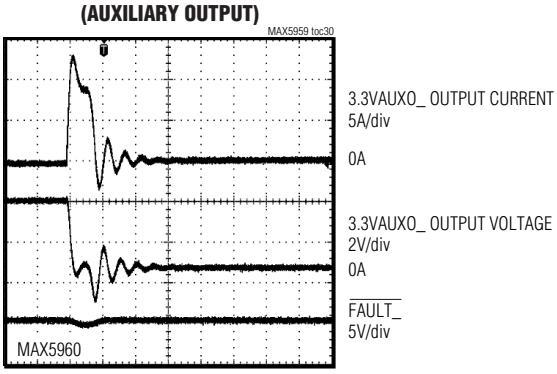
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

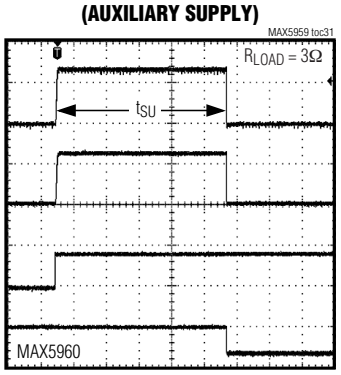
SHORT CIRCUIT ON 3.3AUXO_ (AUXILIARY OUTPUT)



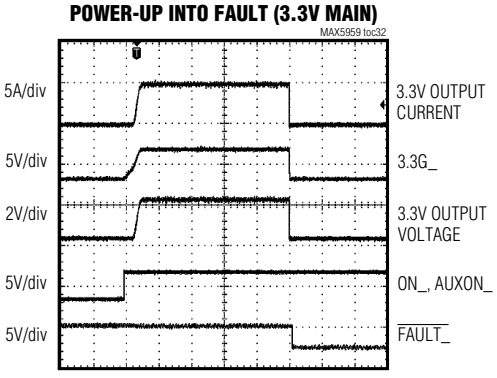
SHORT CIRCUIT ON 3.3VAUXO_ (AUXILIARY OUTPUT)



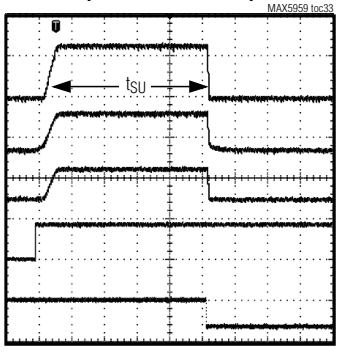
POWER-UP INTO FAULT (AUXILIARY SUPPLY)



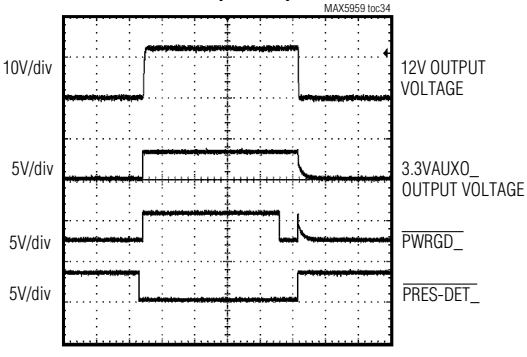
POWER-UP INTO FAULT (3.3V MAIN)



POWER-UP INTO FAULT (12V MAIN OUTPUT)



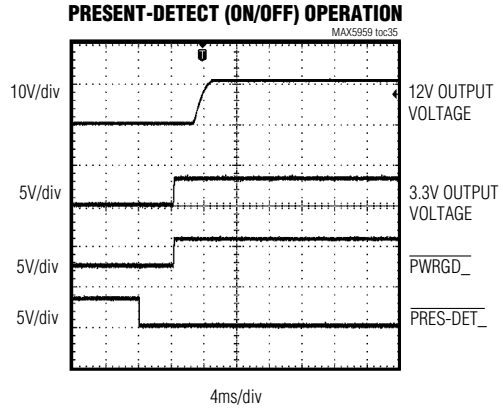
PRESENT-DETECT (ON/OFF) OPERATION



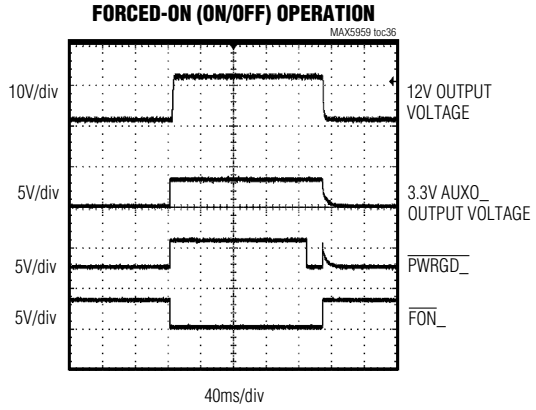
Typical Operating Characteristics (continued)

(V_{12VIN} = V_{12S_+} = 12V, $V_{3.3S\_+}$ = $V_{3.3S\_-}$ = $V_{3.3AUXIN}$ = $V_{ON\_}$ = $V_{AUXON\_}$ = $V_{\overline{FON\_}}$ = 3.3V, $\overline{PWRGD\_}$ = $\overline{FAULT\_}$ = PORADJ = TIM = OUTPUT_ = OPEN, INPUT_ = $\overline{PRES\text{-}DET\_}$ = PGND = GND. See the *Typical Application Circuit*.)

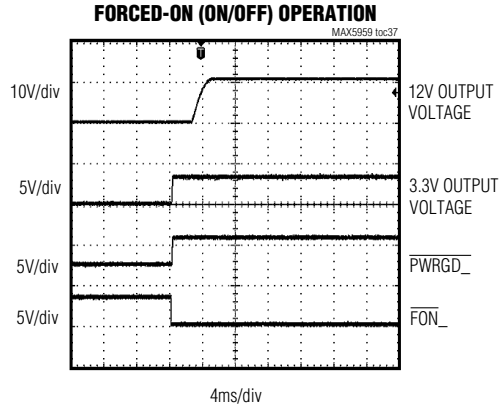
PRESENT-DETECT (ON/OFF) OPERATION



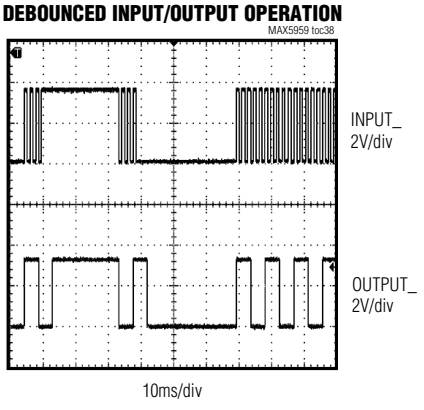
FORCED-ON (ON/OFF) OPERATION



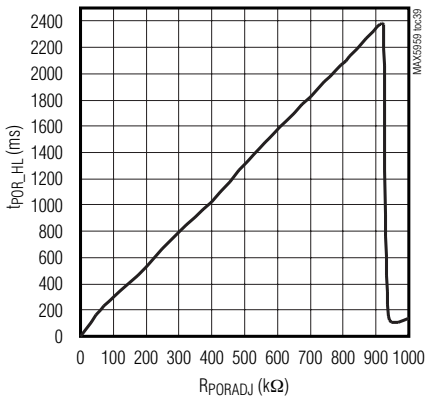
FORCED-ON (ON/OFF) OPERATION



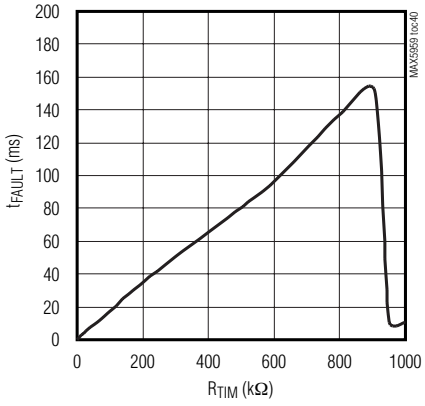
DEBOUNCED INPUT/OUTPUT OPERATION



POWER-ON-RESET TIME vs. PORADJ RESISTOR



t_{FAULT} TIME DELAY vs. TIM RESISTOR



Pin Description

PIN	NAME	FUNCTION
1	12SB-	Slot B 12V Negative Current-Sense Input. Connect 12SB- to the negative side of the current-sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
2	12SB+	Slot B 12V Positive Current-Sense Input. Connect the positive terminal of the current-sense resistor to 12SB+ using the Kelvin-sensing technique to ensure accurate current sensing.
3	AUXONB	Slot B 3.3V Auxiliary Output Enable. A logic-high at AUXONB turns on the slot B auxiliary output.
4	ONB	Slot B 12V and 3.3V Main Outputs Enable. A logic-high at ONB turns on the 12V and 3.3V main outputs of slot B (see Table 2).
5	INPUT1	Digital Logic Gate Input 1
6	OUTPUT1	Digital Output 1. 4ms debounced digital output of INPUT1.
7	INPUT2	Digital Logic Gate Input 2
8	OUTPUT2	Digital Output 2. 4ms debounced digital output of INPUT2.
9, 61, 80	N.C.	No Connection. Not internally connected. Leave unconnected.
10	$\overline{\text{FOND}}$	Slot D Forced-On Input. $\overline{\text{FOND}}$ has a 50kΩ internal pullup to 3.3VAUXIN. A logic-low on $\overline{\text{FOND}}$ turns on all slot D outputs as long as the power inputs are within their operating range, regardless of the status of the other input signals. Leave $\overline{\text{FOND}}$ unconnected for normal operation.
11	$\overline{\text{PRES-DETD}}$	Slot D Present-Detect Input. $\overline{\text{PRES-DETD}}$ accepts inputs from PRSNT#_# on a PCIe connector. $\overline{\text{PRES-DETD}}$ has an internal 50kΩ pullup to 3.3VAUXIN. When $\overline{\text{PRES-DETA}}$ is low, the outputs follow the command from OND and AUXOND after a 4ms debounced time. When $\overline{\text{PRES-DETD}}$ goes from low to high, all outputs of the respective slot shut down with no delay.
12	OND	Slot D 12V and 3.3V Main Outputs Enable. A logic-high at OND turns on the 12V and 3.3V main outputs of slot D (see Table 2).
13	AUXOND	Slot D 3.3V Auxiliary Output Enable. A logic-high at AUXOND turns on the slot D auxiliary output.
14	GND	Ground
15	$\overline{\text{FONC}}$	Slot C Forced-On Input C. $\overline{\text{FONC}}$ has a 50kΩ internal pullup to 3.3VAUXIN. A logic-low on $\overline{\text{FONC}}$ turns on all slot C outputs as long as the power inputs are within their operating range, regardless of the status of the other input signals. Leave $\overline{\text{FONC}}$ unconnected for normal operation.
16	$\overline{\text{PRES-DETC}}$	Slot C Present-Detect Input. $\overline{\text{PRES-DETC}}$ accepts inputs from PRSNT#_# on a PCIe connector. $\overline{\text{PRES-DETC}}$ has an internal 50kΩ pullup to 3.3VAUXIN. When $\overline{\text{PRES-DETC}}$ is low, the outputs follow the command from ONC and AUXONC after a 4ms debounced time. When $\overline{\text{PRES-DETC}}$ goes from low to high, all outputs of the respective slot shut down with no delay.
17	ONC	Slot C 12V And 3.3V Main Outputs Enable. A logic-high at ONC turns on the 12V and 3.3V main outputs of slot C (see Table 2).
18	AUXONC	Slot C 3.3V Auxiliary Output Enable. A logic-high at AUXONC turns on the slot C auxiliary output.
19	12SC+	Slot C 12V Positive Current-Sense Input. Connect the positive terminal of the current-sense resistor to 12SC+ using the Kelvin-sensing technique to ensure accurate current sensing.
20	12SC-	Slot C 12V Negative Current-Sense Input. Connect 12SC- to the negative side of the current-sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
21	12GC	Slot C 12V Gate-Drive Output. Connect 12GC to the gate of slot C's 12V MOSFET. At power-up, 12GC is raised to the internal charge-pump voltage level by a constant current.
22	3.3SC+	Slot C 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SC+ using the Kelvin-sensing technique to ensure accurate current sensing.

Quad PCI Express, Hot-Plug Controllers

Pin Description (continued)

PIN	NAME	FUNCTION
23	3.3SC-	Slot C 3.3V Negative Current-Sense Input. Connect to the negative side of the sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
24	3.3GC	Slot C 3.3V Gate-Drive Output. Connect 3.3GC to the gate of slot C's 3.3V MOSFET. At power-up, 3.3GC is charged to 5.5V above the 3.3V supply by a constant current derived from V_{12VIN}. $V_{3.3GC}$'s rise time is determined by the external gate capacitance.
25	$\overline{FAULTC}$	Open-Drain Fault Output Signal. $\overline{FAULTC}$ latches active-low whenever slot C outputs are shut down due to a fault. A fault is either of: • An overcurrent condition lasting longer than the overcurrent timeout. • A device over temperature condition. If the fault is detected in the main outputs, $\overline{FAULTC}$ must be reset by toggling the ONC input. If the fault is in the auxiliary output, $\overline{FAULTC}$ must be reset by toggling both ONC and AUXONC. For the autorestart version, $\overline{FAULTC}$ is reset when the part initiates the next power-on cycle.
26	$\overline{PWRGDC}$	Open-Drain Power-Good Output. $\overline{PWRGDC}$ goes low 160ms after all outputs of slot C reach their final value and the power MOSFETs are fully enhanced.
27,28	3.3AUXOC	Slot C 3.3V Auxiliary Power-Supply Output
29, 30, 31, 69, 70, 71	3.3VAUXIN	3.3V Auxiliary Supply Input. 3.3VAUXIN is the input to a charge pump that drives the internal MOSFETs connecting 3.3AUXIN to 3.3AUXO_. $V_{3.3AUXIN}$ is also used to power the internal control logic and analog references of the MAX5959/MAX5960 and must always be connected to a supply between 3V and 3.6V. Bypass 3.3AUXIN with at least a 0.1µF capacitor to GND.
32, 33	3.3AUXOD	Slot D 3.3V Auxiliary Power-Supply Output
34, 66	PGND	Power Ground. Connect externally to GND.
35	$\overline{PWRGDD}$	Open-Drain Power-Good Output. $\overline{PWRGDD}$ goes low 160ms after all outputs of slot D reach their final value and the power MOSFETs are fully enhanced.
36	$\overline{FAULTD}$	Open-Drain Fault Output Signal. $\overline{FAULTD}$ latches active-low whenever slot D outputs are shut down due to a fault. A fault is either of: • An overcurrent condition lasting longer than the overcurrent timeout. • A device over temperature condition. If the fault is detected in the main outputs, $\overline{FAULTD}$ must be reset by toggling the OND input. If the fault is in the auxiliary output, $\overline{FAULTD}$ must be reset by toggling both OND and AUXOND. For the autorestart version, $\overline{FAULTD}$ is reset when the part initiates the next power-on cycle.
37	TIM	Overcurrent Timeout Programming Input. Connect a resistor between 500Ω and 500kΩ from TIM to GND to program t_{FAULT}. Leave TIM unconnected for a default timeout of 11ms.
38	PORADJ	Power-On-Reset Programming Input. Connect a resistor between 500Ω and 500kΩ from PORADJ to GND to program the POR timing. Leave unconnected for a default value of 160ms. Connect PORADJ to GND to completely skip the POR time delay for $\overline{PWRGD\_}$ assertion.
39	GND	Ground
40	12VIN	12V Supply Input. V_{12VIN} drives the gates of the MOSFETs connected to 3.3G_. 12VIN powers an internal charge pump that drives the gates of the MOSFETs connected to 12G_. Bypass 12VIN with a 1µF capacitor to GND. See the *Typical Application Circuit* and *Input Transients* section.
41	12GD	Slot D 12V Gate-Drive Output. Connect 12GD to the gate of slot D's 12V MOSFET. At power-up, V_{12GD} is raised to the internal charge-pump voltage level by a constant current.
42	12SD-	Slot D 12V Negative Current-Sense Input. Connect 12SD- to the negative side of the current-sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
43	12SD+	Slot D 12V Positive Current-Sense Input. Connect the positive terminal of the current-sense resistor to 12SD+ using the Kelvin-sensing technique to ensure accurate current sensing.
44	3.3GD	Slot D 3.3V Gate-Drive Output. Connect 3.3GD to the gate of slot D's 3.3V MOSFET. At power-up, $V_{3.3GD}$ is charged to 5.5V above the 3.3V supply by a constant current derived from V_{12VIN}. $V_{3.3GD}$'s rise time is determined by the external gate capacitance.
45	3.3SD-	Slot D 3.3V Negative Current-Sense Input. Connect to the negative side of the sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
46	3.3SD+	Slot D 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SD+ using the Kelvin-sensing technique to ensure accurate current sensing.
47	$\overline{\text{PRES-DETB}}$	Slot B Present-Detect Input. $\overline{\text{PRES-DETB}}$ accepts inputs from PRSNT#_# on a PCIe connector. $\overline{\text{PRES-DETB}}$ has an internal 50kΩ pullup to 3.3VAUXIN. When $\overline{\text{PRES-DETB}}$ is low, the outputs follow the command from ONB and AUXONB after a 4ms debounced time. When $\overline{\text{PRES-DETB}}$ goes from low to high, all outputs of the respective slot shut down with no delay.
48	$\overline{\text{FONB}}$	Slot B Forced-On Input. $\overline{\text{FONB}}$ has a 50kΩ internal pullup to 3.3VAUXIN. A logic-low on $\overline{\text{FONB}}$ turns on all slot B outputs as long as the power inputs are within their operating range, regardless of the status of the other input signals. Leave $\overline{\text{FONB}}$ unconnected for normal operation.
49	$\overline{\text{PRES-DETA}}$	Slot A Present-Detect Input. $\overline{\text{PRES-DETA}}$ accepts inputs from PRSNT#_# on a PCIe connector. $\overline{\text{PRES-DETA}}$ has an internal 50kΩ pullup to 3.3VAUXIN. When $\overline{\text{PRES-DETA}}$ is low, the outputs follow the command from ONA and AUXONA after a 4ms debounced time. When $\overline{\text{PRES-DETA}}$ goes from low to high, all outputs of the respective slot shut down with no delay.
50	$\overline{\text{FONA}}$	Slot A Forced-On Input. $\overline{\text{FONA}}$ has a 50kΩ internal pullup to 3.3VAUXIN. A logic-low on $\overline{\text{FONA}}$ turns on all slot A outputs as long as the power inputs are within their operating range, regardless of the status of the other input signals. Leave $\overline{\text{FONA}}$ unconnected for normal operation.
51	OUTPUT4	Digital Output 4. 4ms debounced digital output of INPUT4.
52	INPUT4	Digital Logic Gate Input 4
53	OUTPUT3	Digital Output 3. 4ms debounced digital output of INPUT3.
54	INPUT3	Digital Logic Gate Input 3
55	ONA	Slot A 12V and 3.3V Outputs Enable. A logic-high at ONA turns on the 12V and 3.3V outputs of slot A (see Table 2).
56	AUXONA	Slot A 3.3V Auxiliary Output Enable. A logic-high at AUXONA turns on the slot A auxiliary output.
57	12SA+	Slot A 12V Positive Current-Sense Input. Connect the positive terminal of the current-sense resistor to 12SA+ using the Kelvin-sensing technique to ensure accurate current sensing.
58	12SA-	Slot A 12V Negative Current-Sense Input. Connect 12SA- to the negative side of the current-sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
59	12GA	Slot A 12V Gate-Drive Output. Connect 12GA to the gate of slot A's 12V MOSFET. At power-up, V_{12GA} is raised to the internal charge-pump voltage level by a constant current.
60	3.3SA+	Slot A 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SA+ using the Kelvin-sensing technique to ensure accurate current sensing.
62	3.3SA-	Slot A 3.3V Negative Current-Sense Input. Connect to the negative side of the sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
63	3.3GA	Slot A 3.3V Gate-Drive Output. Connect 3.3GA to the gate of slot A's 3.3V MOSFET. At power-up, V3.3GA is charged to 5.5V above the 3.3V supply by a constant current derived from V_{12VIN}. $V_{3.3GA}$'s rise time is determined by the external gate capacitance.
64	$\overline{FAULTA}$	Open-Drain Fault Output Signal. $\overline{FAULTA}$ latches active low whenever slot A outputs are shut down due to a fault. A fault is either of: • An overcurrent condition lasting longer than the overcurrent timeout. • A device over temperature condition. If the fault is detected in the main outputs, $\overline{FAULTA}$ must be reset by toggling the ONA input. If the fault is in the auxiliary output, $\overline{FAULTA}$ must be reset by toggling both ONA and AUXONA. For the autorestart version, $\overline{FAULTA}$ is reset when the part initiates the next power-on cycle.
65	$\overline{PWRGDA}$	Open-Drain Power-Good Output. $\overline{PWRGDA}$ goes low 160ms after all outputs of slot A reach their final value and the power MOSFETs are fully enhanced.
67, 68	3.3AUXOA	Slot A 3.3V Auxiliary Power-Supply Output
72, 73	3.3AUXOB	Slot B 3.3V Auxiliary Power-Supply Output
74	$\overline{PWRGDB}$	Open-Drain Power-Good Output. $\overline{PWRGDB}$ goes low 160ms after all outputs of slot B reach their final value and the power MOSFETs are fully enhanced.
75	$\overline{FAULTB}$	Open-Drain Fault Output Signal. $\overline{FAULTB}$ latches active-low whenever slot B outputs are shut down due to a fault. A fault is either of: • An overcurrent condition lasting longer than the overcurrent timeout. • A device over temperature condition. If the fault is detected in the main outputs, $\overline{FAULTB}$ must be reset by toggling the ONB input. If the fault is in the auxiliary output, $\overline{FAULTB}$ must be reset by toggling both ONB and AUXONB. For the autorestart version, $\overline{FAULTB}$ is reset when the part initiates the next power-on cycle.
76	3.3GB	Slot B 3.3V Gate-Drive Output. Connect 3.3GB to the gate of slot B's 3.3V MOSFET. At power-up, $V_{3.3GB}$ is charged to 5.5V above the 3.3V supply by a constant current derived from V_{12VIN}. $V_{3.3GB}$'s rise time is determined by the external gate capacitance.
77	3.3SB-	Slot B 3.3V Negative Current-Sense Input. Connect to the negative side of the sense resistor using the Kelvin-sensing technique to ensure accurate current sensing.
78	3.3SB+	Slot B 3.3V Positive Current-Sense Input. Connect the positive side of the current-sense resistor to 3.3SB+ using the Kelvin-sensing technique to ensure accurate current sensing.
79	12GB	Slot B 12V Gate-Drive Output. Connect 12GB to the gate of slot B's 12V MOSFET. At power-up, V_{12GB} is raised to the internal charge-pump voltage level by a constant current.

Detailed Description

The MAX5959/MAX5960 quad hot-plug controllers are designed for PCIe applications. The devices provide hot-plug control for 12V, 3.3V, and 3.3V auxiliary supplies for three PCIe slots. The MAX5959/MAX5960s' logic inputs/outputs allow interfacing directly with the system hot-plug-management controller or through an SMBus with an external I/O expander. An integrated debounced attention switch and present-detect signals are included to simplify system design (Figure 1).

The MAX5959/MAX5960 drive eight external n-channel MOSFETs to control the 12V and 3.3V main outputs. The 3.3V auxiliary outputs are controlled through internal 0.2Ω n-channel MOSFETs. Internal charge pumps provide a gate drive for the 12V outputs while the gate drive of the 3.3V output is driven by the 12V input supply. The 3.3V auxiliary outputs are completely independent from the main outputs with their own charge pumps.

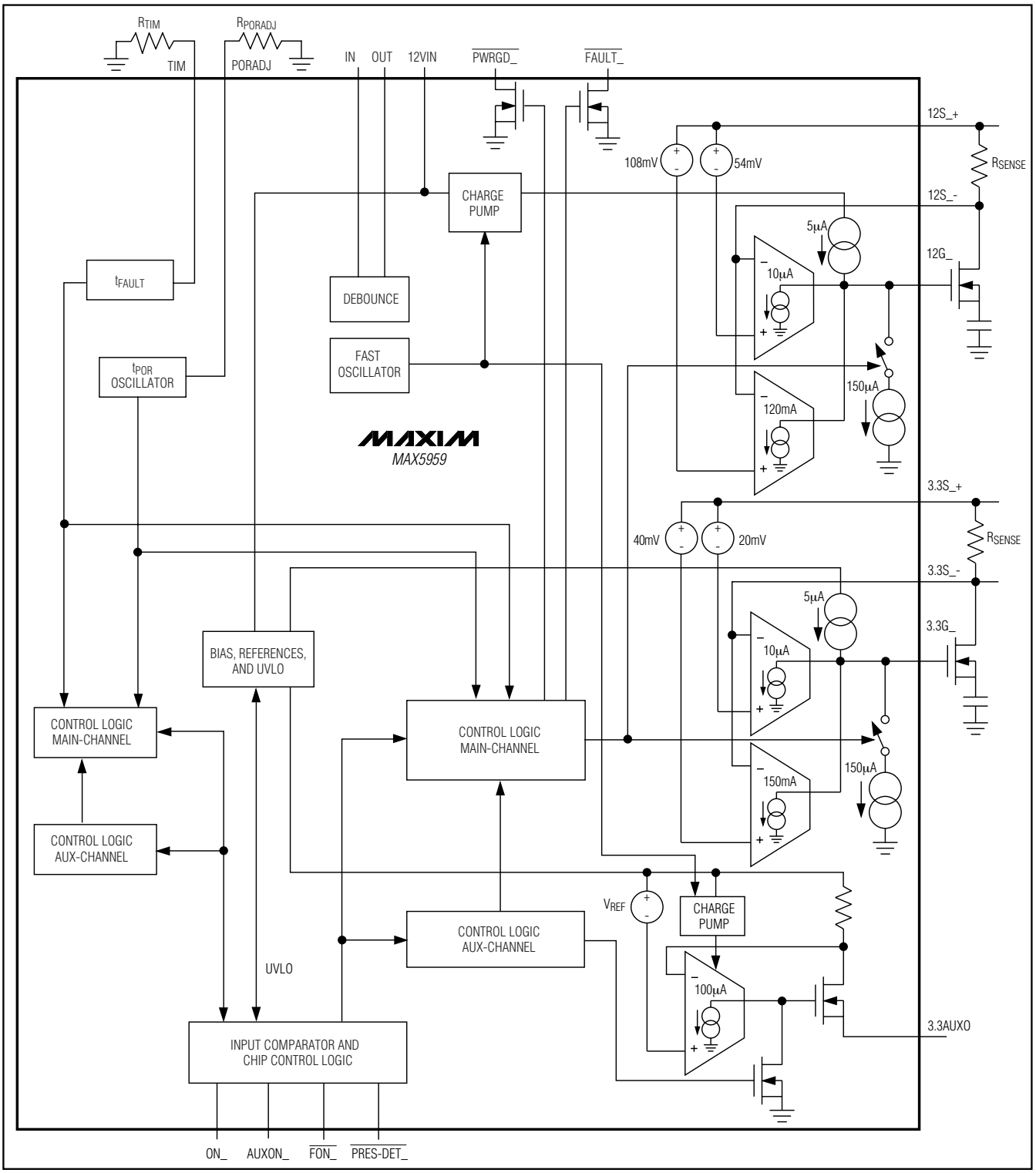


Figure 1. Single-Channel Internal Block Diagram

At power-up, the MAX5959/MAX5960 keep all the external MOSFETs off until all supplies rise above their respective UVLO thresholds. These devices keep the internal MOSFETs off only until the 3.3VAUXIN supply rises above its UVLO threshold. Upon a turn-on command, the MAX5959/MAX5960 enhance the external and internal MOSFETs slowly with a constant gate current to limit the power-supply inrush current. The MAX5959/MAX5960 actively limit the current of all outputs at all times and shut down the corresponding channel if an overcurrent condition persists for longer than a resistor-programmable overcurrent timeout (see the *Fault Management* section). Thermal protection circuitry also shuts down all outputs if the die temperature exceeds +150°C. After an overcurrent or overtemperature fault condition, the MAX5959/MAX5960 latch off or automatically restart depending on the version, after a restart time delay.

The power requirement for PCIe connectors is defined by the PCIe card specification and summarized in Table 1.

Startup

The main supply outputs can become active only after all the following events have occurred:

- $V_{3.3AUXIN}$ is above its UVLO threshold.
- V_{12VIN} and $V_{3.3SA+}$ are both above their UVLO threshold.
- ON_ is driven high.
- $\overline{\text{PRES-DET\_}}$ is low for more than 4ms.

The auxiliary supply output is made available only after the following events have occurred:

- $V_{3.3AUXIN}$ is above its UVLO threshold.
- AUXON_ is driven high.
- $\overline{\text{PRES-DET\_}}$ is low for more than 4ms.

The $\overline{\text{FON\_}}$ input overrides all other control signals and turns on the respective slot when driven low, as long as the UVLO thresholds have been reached. Table 2 summarizes the logic conditions required for startup. The auxiliary supply input powers the internal control logic and analog references of the MAX5959/MAX5960, so the main supplies cannot be enabled, if $V_{3.3VAUXIN}$ is not present. When an output is enabled, a programmable startup timer (t_{SU}) begins to count the startup time duration.

The value of t_{SU} is set to 2x the fault timeout period (t_{FAULT}). R_{TIM} externally connected from TIM to GND sets the duration of t_{FAULT}.

Table 1. Power Requirement for PCIe Connectors

POWER FAIL	X1 CONNECTOR	X4/8 CONNECTOR	X16 CONNECTOR
3.3V			
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)
Supply Current	3.0A (max)	3.0A (max)	3.0A (max)
Capacitive Load	1000µF (max)	1000µF (max)	1000µF (max)
12V			
Voltage Tolerance	±8% (max)	±8% (max)	±8% (max)
Supply Current	0.5A (max)	2.1A (max)	5.5A (max)
Capacitive Load	300µF (max)	1000µF (max)	2000µF (max)
3.3V AUXILIARY			
Voltage Tolerance	±9% (max)	±9% (max)	±9% (max)
Supply Current, Wake Enabled	375mA (max)	375mA (max)	375mA (max)
Supply Current, Nonwake Enabled	20mA (max)	20mA (max)	20mA (max)
Capacitive Load	150µF (max)	150µF (max)	150µF (max)

Table 2. Control Logic Truth Table

ON_	AUXON_	$\overline{FON\_}$	$\overline{PRES\text{-}DET}$	12V_ AND 3.3V_ OUTPUTS	3.3VAUXO_AUXILIARY OUTPUTS
X	X	Low	X	On	On
X	X	High	High	Off	Off
Low	Low	High	Low*	Off	Off
High	Low	High	Low*	On	Off
Low	High	High	Low*	Off	On
High	High	High	Low*	On	On

**PRES-DET_ high-to-low transition has a 4ms delay (t_{DEG}).*

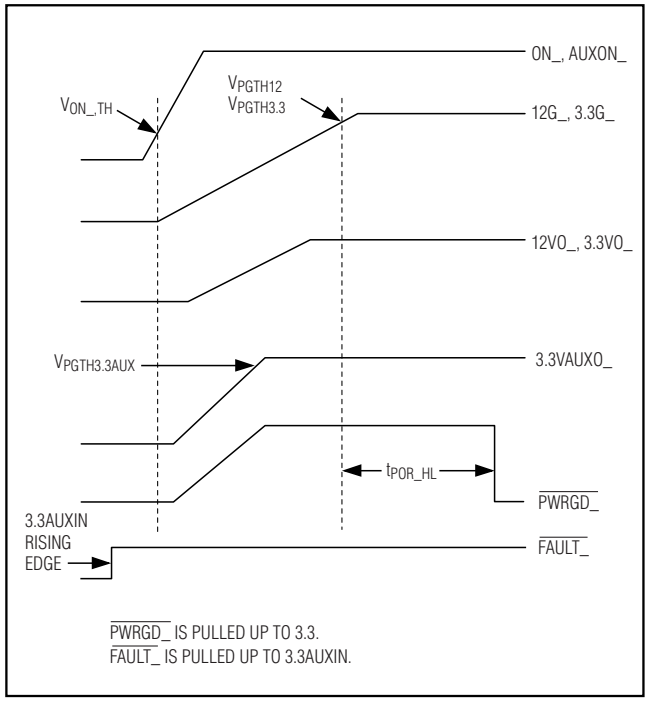


Figure 2. Power-Up Timing, No Fault

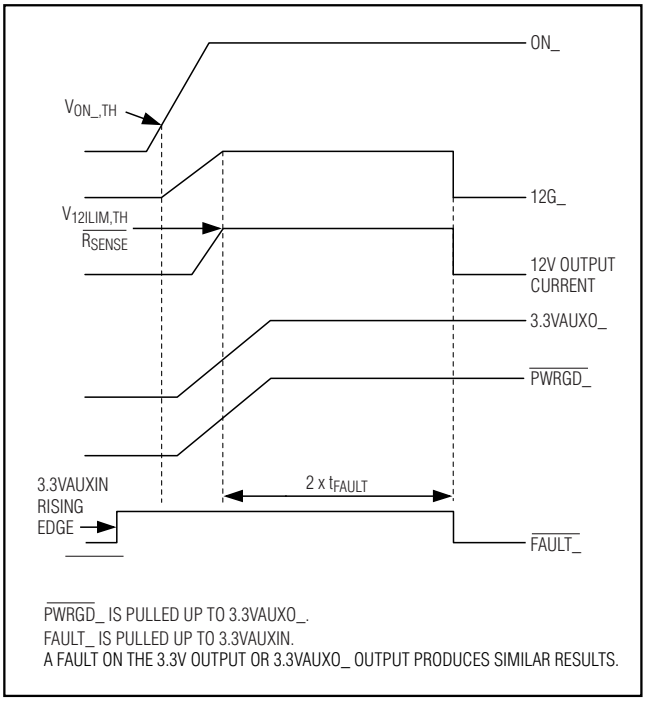


Figure 3. 12V Power-Up Timing (Turn-On into Output Overcurrent/Short Circuit)

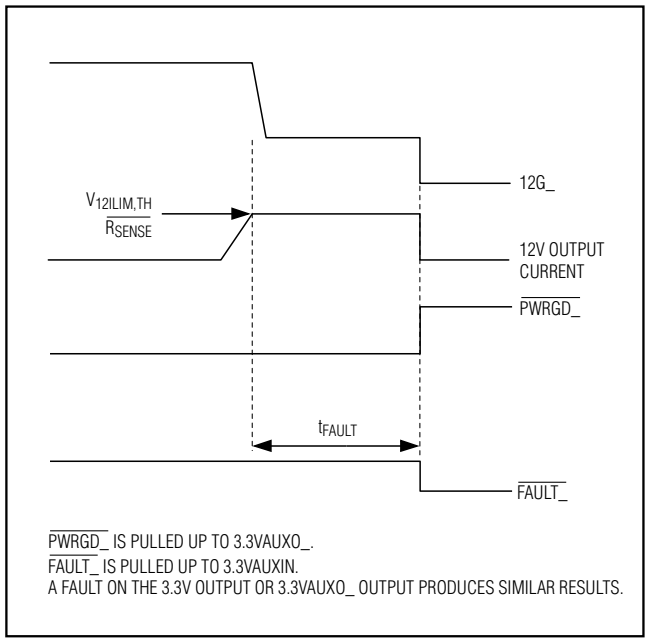


Figure 4. 12 Output Overcurrent/Short Circuit During Normal Operation

12V and 3.3V Outputs Normal Operation

The MAX5959/MAX5960 monitor and actively limit the current of the 12V and 3.3V outputs after the startup period. Each output has its own overcurrent threshold. If any of the monitored output currents rise above the overcurrent threshold for a period t_{FAULT}, $\overline{FAULT\_}$ asserts and the controller disengages both the 12V and 3.3V outputs for the particular slot (see the *Fault Management* section).

3.3V Auxiliary Output Normal Operation

The auxiliary output current is internally monitored and actively limited to the maximum current-limit value. An overcurrent fault condition occurs when the output current exceeds the overcurrent threshold for longer than t_{FAULT}. A fault on an auxiliary channel causes all supplies of the affected channel to be disabled after a programmable time period t_{FAULT}.

A fault condition on a main channel (V_{12VIN} or $V_{3.3VIN}$) causes all the channel's main outputs to shut down after the t_{FAULT} period and then either latch off or automatically restart after the $t_{RESTART}$ ($t_{RESTART}$ = 64 x t_{FAUALT}) period, depending on the device version. A fault on any of the channel's main output does not affect the auxiliary channel ($V_{3.3AUXIN}$).

Power-Good (PWRGD_)

Power-good ($\overline{PWRGD\_}$) is an open-drain output that pulls low a time (t_{POR_HL}) after all the outputs of the respective slot are fully on. All outputs are considered fully on when 3.3G_ has risen to $V_{PGTH3.3}$, 12G_ has risen to V_{PGTH12}, and $V_{3.3AUXO\_}$ is less than $V_{PGTH3.3AUX}$. t_{POR_HL} is adjustable from 2.4ms to 1.5s by connecting a resistor from PORADJ to GND. See the *Setting the Power-On Reset* and *Timeout Period (t_{POR_HL})* sections. Connect PORADJ to GND to completely skip the POR time delay for $\overline{PWRGD\_}$ assertion.

Thermal Shutdown

When the die temperature goes above (T_{SD}) +150°C, an overtemperature fault occurs and the MAX5959/MAX5960 shut down all outputs. The device waits for the junction temperature to decrease below T_{SD} - hysteresis before entering fault management (see the *Fault Management* section):

Fault Management

A fault occurs when an overcurrent or 12G_ or 3.3G_ below their power-good threshold lasts longer than $t_{\overline{FAULT}}$ or when the device experiences an overtemperature condition:

- A fault on a main output (12V or 3.3V) shuts down both main outputs of the respective slot. The 3.3V auxiliary is not affected.
- A fault on the 3.3V auxiliary output shuts down all three outputs of the respective slot.

The MAX5959A/MAX5960A automatically restart from a fault shutdown after the $t_{RESTART}$ period while the MAX5959L/MAX5960L latch off. If an overcurrent fault occurred on a main output, bring ON_ low for at least t_{RESET} (100µs) and high again to reset the fault and restart the outputs. If the overcurrent fault occurred on an auxiliary output or an overtemperature fault occurred, bring both ON_ and AUXON_ low for a minimum of t_{RESET} to reset the fault. Toggle ON_ or only AUXON_ to reset the fault condition. If ON_ and AUXON are toggled before $t_{RESTART}$ time counting has elapsed, the MAX5959L/MAX5960L store the information and restart when the delay is finished. The MAX5959A/MAX5960A (autoretry versions) restart all channels automatically after $t_{RESTART}$.

Debounced Logic Gate (INPUT_ and OUTPUT_)

INPUT1, INPUT2, and INPUT3 accept inputs from mechanical switches. The corresponding outputs are OUTPUT1, OUTPUT2, OUTPUT3, and OUTPUT4. OUTPUT_ is debounced for 4ms. When INPUT_ goes from high to low, OUTPUT_ goes low immediately and stays low for at least 4ms. After the debounce time, OUTPUT_ follows INPUT_. If INPUT_ goes from low to high, OUTPUT_ goes high immediately and stays high for at least 4ms. After the debounce time, OUTPUT_ follows INPUT_. Figure 5 shows the timing diagram describing the INPUT_/OUTPUT_ debounced feature.

Present-Detect and Forced-On Inputs (PRES-DET_, FON_)

$\overline{\text{PRES-DET\_}}$ input detects the PRSNT_# pin on a PCIe connector. When the card is plugged in, $\overline{\text{PRES-DET\_}}$ goes low and allows the turn-on of the outputs of the respective slot after a 4ms debounced time. When the card is removed, an internal 50kΩ pullup resistor forces $\overline{\text{PRES-DET\_}}$ high and the respective slot is shut down with no delay. $\overline{\text{PRES-DET\_}}$ works in conjunction with ON_ and AUXON_ and only enables the device when ON_ and AUXON_ are high.

A logic-low on $\overline{\text{FON\_}}$ forces the respective slot (main supplies and auxiliary) to turn on regardless of the status of the other logic inputs, provided the UVLO thresholds are exceeded on all the inputs.

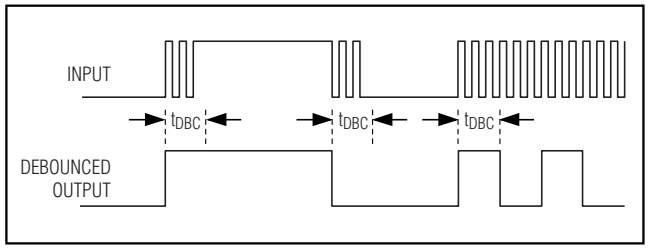


Figure 5. INPUT_ AND OUTPUT_ Debounced Feature

Active Current Limits

Active current limits are provided for all three outputs of the four slots (slot A, slot B, slot C, and slot D). Connect a current-sense resistor between 12S_+ and 12S_- to set the current limit for the 12V outputs. The current limit is set to 54mV / $R_{SENSE12}$. Connect a current-sense resistor between 3.3S_+ and 3.3S_- to set the current limit for the 3.3V main outputs to 20mV / $R_{SENSE3.3}$. For the auxiliary output (3.3VAUXO_) the current limit is fixed at 450mA in the MAX5959 and 700mA in the case of the MAX5960.

When the voltage across $R_{SENSE12}$ or $R_{SENSE3.3}$ reaches the current-limit threshold voltage, the MAX5959/MAX5960 regulate the gate voltage to maintain the current-limit threshold voltage across the sense resistor. If the current limit lasts for t_{FAULT}, then an overcurrent fault occurs. The MAX5959/MAX5960 shut down both the 12V and 3.3V outputs and assert the $\overline{\text{FAULT\_}}$ output of the respective slot.

When the auxiliary output reaches the current limit 450mA (MAX5959) or 700mA (MAX5960) for longer than t_{FAULT}, a fault occurs and the device shuts down all outputs and asserts FAULT of the respective slot.

UVLO Threshold

The UVLO thresholds prevent the internal auxiliary MOSFETs and the external main channel MOSFETs from turning on if V_{12VIN}, $V_{3.3VIN}$, and $V_{3.3VAUXIN}$ are not present. Internal comparators monitor the main supplies and the auxiliary supply and keep the gate-drive outputs (12GA, 12GB, 12GC, 12GD, 3.3GA, 3.3GB, 3.3GC, and 3.3GD) low until the supplies rise above their UVLO threshold. The 12V main supply is monitored at 12VIN and has a UVLO threshold of 10V. The 3.3V main supply is monitored at 3.3SA+ and has a UVLO threshold of 2.65V. The auxiliary supply is monitored at 3.3AUXIN and has a 2.65V UVLO threshold. For either main channels to operate, V3.3AUXIN must be above its UVLO threshold.

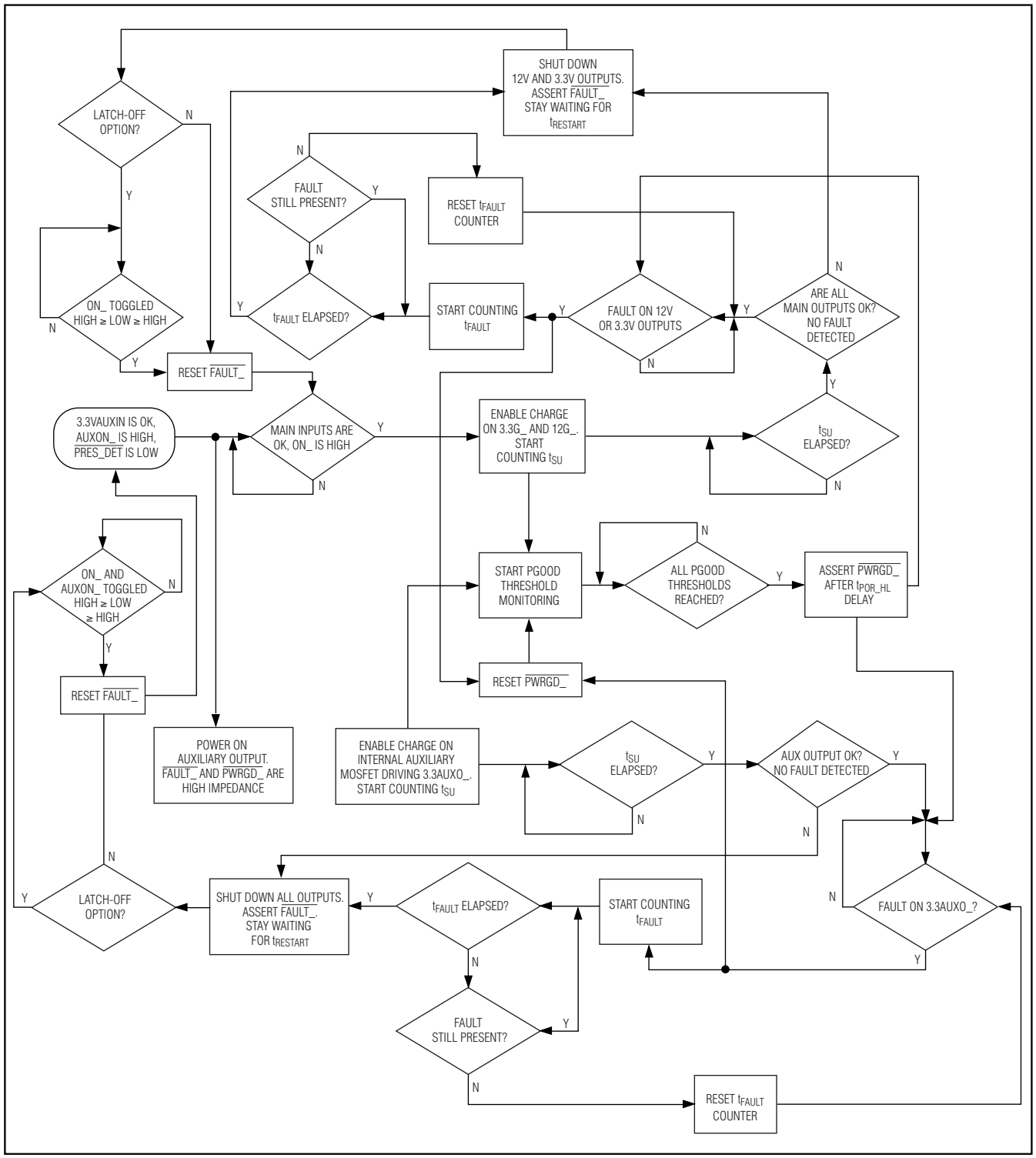


Figure 6. Fault Management Flowchart

External MOSFET Gate Drivers (12G_ and 3.3G_)

The gate drive for the external MOSFETs is provided at 12GA, 12GB, 12GC, 12GD, 3.3GA, 3.3GB, 3.3GC, and 3.3GD. 12G_ is the gate drive for the 12V main supply and is boosted to 5.3V above V_{12VIN} by its internal charge pump. During turn-on, 12G_ sources 5µA into the external gate capacitance to control the turn-on time of the external MOSFET. During turn-off, 12G_ sinks 150µA from the external gate capacitance to quickly turn off the external MOSFET. During short-circuit events, an internal 120mA current sink activates to rapidly bring the load current into the regulation limits.

3.3G_ is the gate drive for the 3.3V main supply's MOSFET and is driven to 5.5V above the 3.3V main supply. The power for 3.3G_ is supplied from 12VIN and has no internal charge pump. During turn-on, 3.3G_ sources 5µA into the external gate capacitance to control the turn-on time of the external MOSFET. During turn-off, 3.3G_ sinks 150µA to quickly turn off the external MOSFET. During short-circuit events, an internal 120mA current sink activates to rapidly turn off the appropriate external MOSFET.

Auxiliary Supply (3.3VAUXIN)

3.3VAUXIN provides power to the auxiliary outputs as well as the internal logic and references. The drains of the internal auxiliary MOSFETs connect to 3.3AUXIN through internal sense resistors and the sources connect to the auxiliary outputs (3.3VAUXO_). Both MOSFETs have typical on-resistance of 0.2Ω. Each channel's internal charge pump boosts the gate-drive voltage to fully turn on the internal n-channel MOSFETs. The auxiliary supplies have an internal current limit set to 450mA (MAX5959) or 700mA (MAX5960).

Applications Information

Setting the Power-On Reset

t_{FAULT} is the time an overcurrent or overtemperature fault must remain for the MAX5959/MAX5960 to disable the main or auxiliary channels of a particular slot. Program the fault timeout period (t_{FAULT}) by connecting a resistor (R_{TIM}) from TIM to GND. t_{FAULT} can be calculated by the following equation:

$$t_{FAULT} = (166ns / \Omega) \times R_{TIM}$$

The t_{FAULT} programmed time duration must be chosen according to the total capacitance load connected to the 12G_ and 3.3G_ pins. To properly power up the main supply outputs, the following constraints need to be taken:

$$t_{SU} \geq (V_{GATE} \times C_{LOAD}) / I_{CHG}$$

where $t_{SU} = 2 \times t_{FAULT}$ and where:

- I_{CHG} = 5µA.
- V_{GATE} = 4.8V + V_{12VIN} for 12G_ and V_{GATE} = 6.8V + $V_{3.3VIN}$ for 3.3G_.
- C_{LOAD} is the total capacitance load at the gate.

Maximum and minimum values for R_{TIM} are 500Ω and 500kΩ, respectively. Leave TIM floating for a default t_{FAULT} of 10ms.

Timeout Period (t_{POR_HL})

t_{POR_HL} is the time from when the gate voltages of all outputs of a slot reach their power-good threshold to when $\overline{PWRGD\_}$ pulls low. Program the POR timeout period (t_{POR}) by connecting a resistor (R_{PORADJ}) from PORADJ to GND. t_{POR_HL} can be calculated by the following equation:

$$t_{POR\_HL} = (2.5\mu s / \Omega) \times R_{PORADJ}$$

Maximum and minimum values for R_{PORADJ} are 500Ω and 500kΩ, respectively. Leave PORADJ floating for a default t_{POR} of 150ms. Connect PORADJ to GND in order to completely skip the power-on delay time prior to the $\overline{PWRGD\_}$ assertion.

Component Selection

Select the external n-channel MOSFET according to the applications current requirement. Limit the switch power dissipation by choosing a MOSFET with an R_{DS_ON} low enough to have a minimum voltage drop at full load. High R_{DS_ON} causes larger output ripple if there are pulsed loads. High R_{DS_ON} can also trigger an external undervoltage fault at full load. Determine the MOSFET's power-rating requirement to accommodate a short-circuit condition on the board during start-up. Table 3 lists the MOSFETs and sense resistor manufacturers.

Table 3. Component Manufacturers

COMPONENT	MANUFACTURER	PHONE	WEBSITE
Sense Resistor	Vishay-Date	402-564-3131	www.vishay.com
	IRC	704-264-8861	www.irctt.com
MOSFETs	Fairchild	888-522-5372	www.fairchildsemi.com
	International Rectifier	310-322-3331	www.irf.com
	Motorola	602-244-3576	www.mot-sps.com/ppd
	Vishay-Siliconix	—	www.vishay.com

Additional External Gate Capacitance

External capacitance can be added from the gate of the external MOSFETs to GND to slow down the dV/dt of the 12V and 3.3V outputs. The maximum gate capacitance load at 12G_ and 3.3G_ must be consistent with the conditions described in the *Setting the Power-On Reset* section.

Maximum Load Capacitance

Large capacitive loads at the 12V output, the 3.3V output, and the 3.3V auxiliary output can cause a problem when inserting discharged PCI cards into live backplanes. A fault occurs if the time needed to charge the capacitance of the board is greater than the typical startup time (2 x t_{FAULT}). The MAX5959/MAX5960 withstand large capacitive loads due to their adjustable startup times and adjustable current-limit thresholds. Calculate the maximum load capacitance as follows:

$$C_{LOAD} < (t_{SU} \times I_{LIM}) / V_{OUT}$$

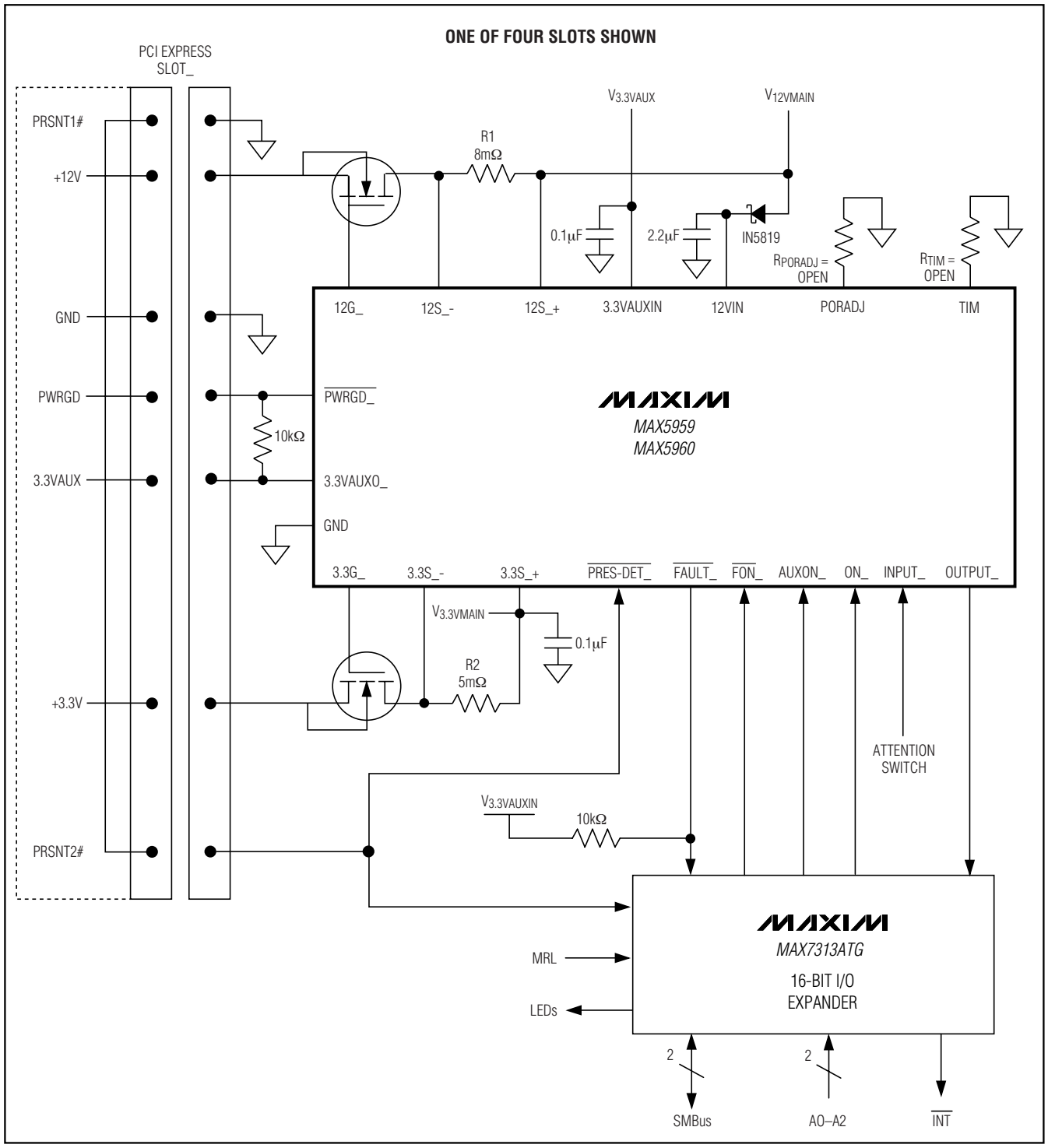
V_{OUT} is either the 3.3V output, the 12V output, or the 3.3V auxiliary output for slot A, slot B, slot C, or slot D.

Input Transients

The 12V input (12VIN), the 3.3V input (3.3SA+), and the 3.3V auxiliary (3.3AUXIN) must be above their UVLO thresholds before startup can occur. Input transients can cause the input voltage to sag below the UVLO threshold. The MAX5959/MAX5960 reject transients on the input supplies that are shorter than 4µs (typ).

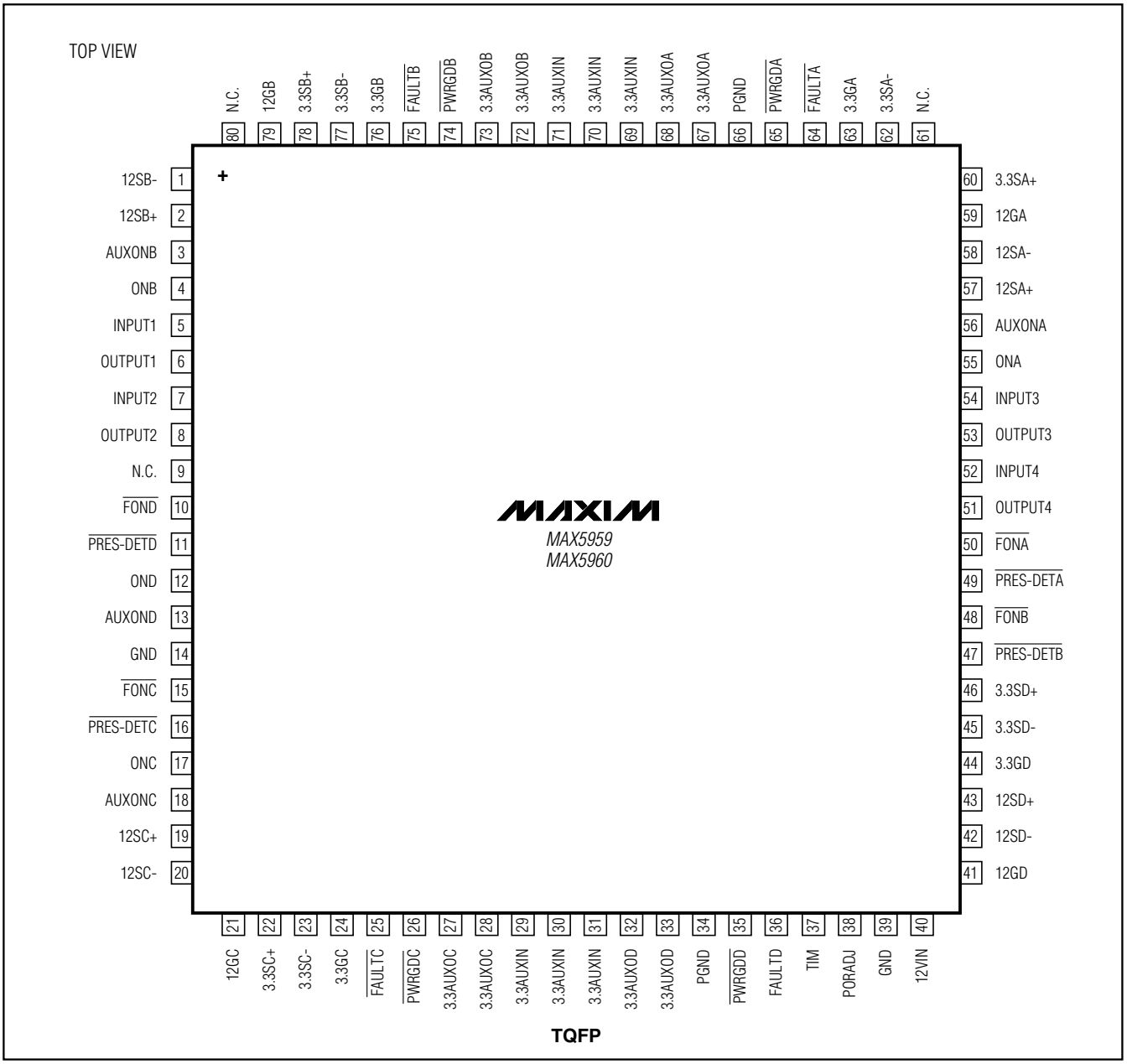
Because some load fault conditions can cause voltage transients to propagate to the supply inputs with duration of greater than 4µs, it is recommended that a small Schottky diode be placed in series with the 12VIN pin connection, upstream of the 1µF bypass capacitor. This provides a hold-up supply that will prevent the 12VIN input from dropping below V_{12UVLO} during severe transients. See the *Typical Application Circuit*.

Typical Application Circuit



Quad PCI Express, Hot-Plug Controllers

Pin Configuration



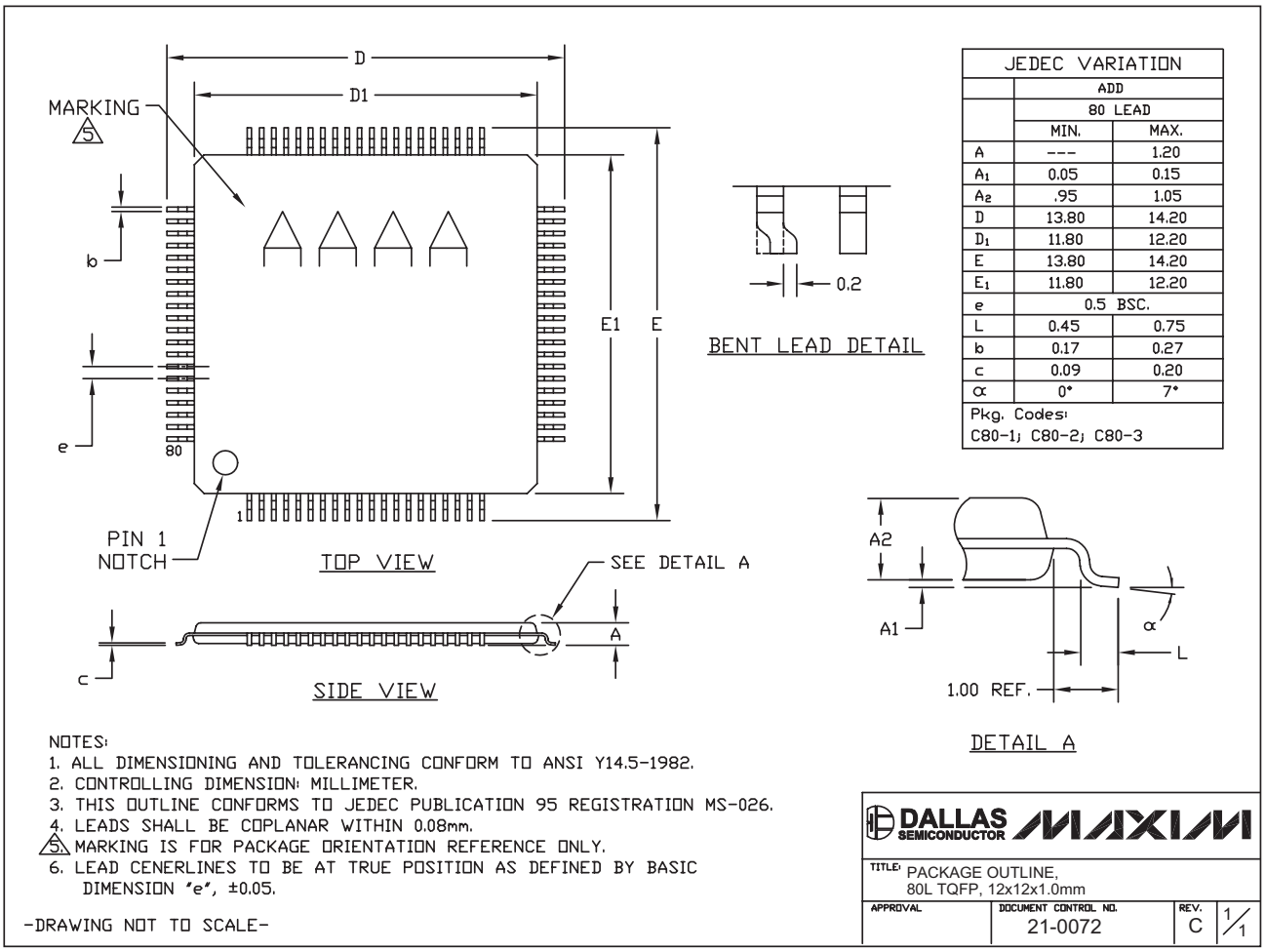
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TQFP12x12mm.EPS



JEDEC VARIATION		
	ADD	
	80 LEAD	
	MIN.	MAX.
A	---	1.20
A_1	0.05	0.15
A_2	.95	1.05
D	13.80	14.20
D_1	11.80	12.20
E	13.80	14.20
E_1	11.80	12.20
e	0.5 BSC.	
L	0.45	0.75
b	0.17	0.27
c	0.09	0.20
α	0°	7°
Pkg. Codes: C80-1; C80-2; C80-3		

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm.
5. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
6. LEAD CENERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 80L TQFP, 12x12x1.0mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0072	REV. C	1/1