

## 7.6A, 12ns, SOT23/TDFN, MOSFET Driver

### General Description

The MAX5048A/MAX5048B are high-speed MOSFET drivers capable of sinking/sourcing 7.6A/1.3A peak currents. These devices take logic input signals and drive a large external MOSFET. The MAX5048A/MAX5048B have inverting and noninverting inputs that give the user greater flexibility in controlling the MOSFET. They feature two separate outputs working in complementary mode, offering flexibility in controlling both turn-on and turn-off switching speeds.

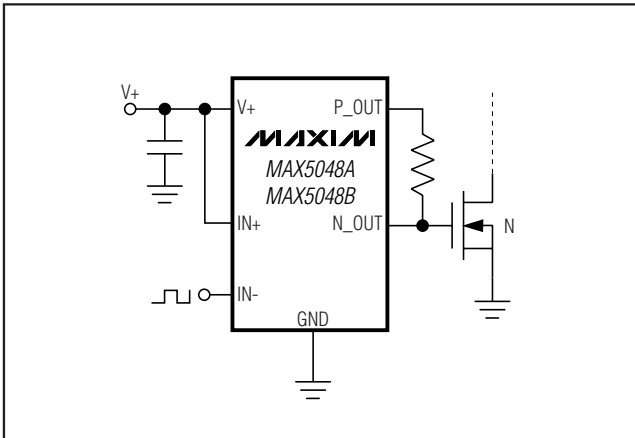
The MAX5048A/MAX5048B have internal logic circuitry, which prevents shoot-through during output state changes. The logic inputs are protected against voltage spikes up to +14V, regardless of V+ voltage. Propagation delay time is minimized and matched between the inverting and noninverting inputs. The MAX5048A/MAX5048B have very fast switching times combined with very short propagation delays (12ns typ), making them ideal for high-frequency circuits.

The MAX5048A/MAX5048B operate from a +4V to +12.6V single power supply and typically consume 0.95mA of supply current. The MAX5048A has CMOS input logic levels, while the MAX5048B has standard TTL input logic levels. These devices are available in space-saving 6-pin SOT23 and TDFN packages.

### Applications

Power MOSFET Switching  
Switch-Mode Power Supplies  
DC-DC Converters  
Motor Control  
Power-Supply Modules

### Typical Operating Circuit



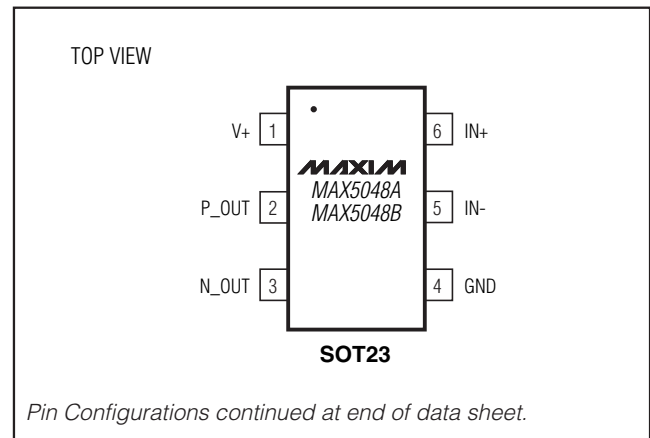
### Features

- ◆ Independent Source-and-Sink Outputs for Controllable Rise and Fall Times
- ◆ +4V to +12.6V Single Power Supply
- ◆ 7.6A/1.3A Peak Sink/Source Drive Current
- ◆ 0.23Ω Open-Drain n-Channel Sink Output
- ◆ 2Ω Open-Drain p-Channel Source Output
- ◆ 12ns (typ) Propagation Delay
- ◆ Matching Delay Time Between Inverting and Noninverting Inputs
- ◆ V<sub>CC</sub>/2 CMOS (MAX5048A)/TTL (MAX5048B) Logic Inputs
- ◆ 1.6V Input Hysteresis
- ◆ Up to +14V Logic Inputs (Regardless of V+ Voltage)
- ◆ Low Input Capacitance: 2.5pF (typ)
- ◆ -40°C to +125°C Operating Temperature Range
- ◆ 6-Pin SOT23 and TDFN Packages

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	LOGIC INPUT	TOP MARK
MAX5048AAUT-T	-40°C to +125°C	6 SOT23-6	V <sub>CC</sub> /2 CMOS	ABEC
MAX5048BAUT-T	-40°C to +125°C	6 SOT23-6	TTL	ABED
MAX5048AATT-T	-40°C to +125°C	6 TDFN-6	V <sub>CC</sub> /2 CMOS	AKV
MAX5048BATT-T	-40°C to +125°C	6 TDFN-6	TTL	AKW

### Pin Configurations



Pin Configurations continued at end of data sheet.

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### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V+	-0.3V to +13V
IN+, IN-	-0.3V to +14V
N_OUT, P_OUT	-0.3V to (V+ + 0.3V)
N_OUT Continuous Output Current (Note 1)	390mA
P_OUT Continuous Output Current (Note 1)	100mA
Continuous Power Dissipation* (T <sub>A</sub> = +70°C)	
6-Pin SOT23 (derate 9.1mW/°C above +70°C)	727mW

Junction to Case Thermal Resistance, $\theta_{JC}$ (SOT23)	75°C/W
6-Pin TDFN (derate 18.2mW/°C above +70°C)	1454mW
Junction to Case Thermal Resistance, $\theta_{JC}$ (TDFN)	8.5°C/W
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

**Note 1:** Continuous output current is limited by the power dissipation of the package.

\*As per JEDEC51 standard.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V+ = +12V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
V+ Operating Range	V+		4.0		12.6	V
V+ Undervoltage Lockout	UVLO	V+ rising	3.25	3.6	4.00	V
V+ Undervoltage Lockout Hysteresis				400		mV
V+ Undervoltage Lockout to Output Delay Time		V+ rising		300		ns
V+ Supply Current	I+	IN+ = IN- = V+		0.95	1.5	mA
<b>n-CHANNEL OUTPUT</b>						
Driver Output Resistance— Pulling Down (MAX5048AAUT/ MAX5048BAUT)	R <sub>ON-N</sub>	V+ = +10V, IN-OUT = -100mA	T <sub>A</sub> = +25°C	0.23	0.26	Ω
			T <sub>A</sub> = +125°C	0.38	0.43	
		V+ = +4.5V, IN-OUT = -100mA	T <sub>A</sub> = +25°C	0.24	0.28	
			T <sub>A</sub> = +125°C	0.40	0.47	
Driver Output Resistance— Pulling Down (MAX5048AATT/ MAX5048BATT)	R <sub>ON-N</sub>	V+ = +10V, IN-OUT = -100mA	T <sub>A</sub> = +25°C	0.31	0.34	Ω
			T <sub>A</sub> = +125°C	0.46	0.51	
		V+ = +4.5V, IN-OUT = -100mA	T <sub>A</sub> = +25°C	0.32	0.36	
			T <sub>A</sub> = +125°C	0.48	0.55	
Power-Off Pulldown Resistance		V+ = 0 or floating, IN-OUT = -10mA, T <sub>A</sub> = +25°C		3.3	10	Ω
Power-Off Pulldown Clamp Voltage		V+ = 0 or floating, IN-OUT = -10mA, T <sub>A</sub> = +25°C		0.85	1.0	V
Output Leakage Current	I <sub>LK-N</sub>	N_OUT = V+		6.85	20	μA
Peak Output Current (Sinking)	I <sub>PK-N</sub>	C <sub>L</sub> = 10,000pF		7.6		A
<b>p-CHANNEL OUTPUT</b>						
Driver Output Resistance— Pulling Up (MAX5048AAUT/ MAX5048BAUT)	R <sub>ON-P</sub>	V+ = +10V, IP-OUT = 50mA	T <sub>A</sub> = +25°C	2.00	3.00	Ω
			T <sub>A</sub> = +125°C	2.85	4.30	
		V+ = +4.5V, IP-OUT = 50mA	T <sub>A</sub> = +25°C	2.20	3.30	
			T <sub>A</sub> = +125°C	3.10	4.70	

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**MAX5048**

## ELECTRICAL CHARACTERISTICS (continued)

(V+ = +12V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Output Resistance— Pulling Up (MAX5048AATT/ MAX5048BATT)	R <sub>ON-P</sub>	V+ = +10V, I <sub>P-OUT</sub> = 50mA	T <sub>A</sub> = +25°C	2.08	3.08	Ω
			T <sub>A</sub> = +125°C	2.93	4.38	
		V+ = +4.5V, I <sub>P-OUT</sub> = 50mA	T <sub>A</sub> = +25°C	2.28	3.38	
			T <sub>A</sub> = +125°C	3.18	4.78	
Output Leakage Current	I <sub>LK-P</sub>	P <sub>OUT</sub> = 0		0.001	10	μA
Peak Output Current (Sourcing)	I <sub>PK-P</sub>	C <sub>L</sub> = 10,000pF		1.3		A
<b>LOGIC INPUT</b>						
Logic 1 Input Voltage	V <sub>IH</sub>	MAX5048A	0.67 × V+			V
		MAX5048B	2.4			
Logic 0 Input Voltage	V <sub>IL</sub>	MAX5048A	0.33 × V+			V
		MAX5048B	0.8			
Logic-Input Hysteresis	V <sub>HYS</sub>	MAX5048A	1.6			V
		MAX5048B	0.68			
Logic-Input Current		V <sub>IN_</sub> = V+ or 0		0.001	10	μA
Input Capacitance	C <sub>IN</sub>			2.5		pF
<b>SWITCHING CHARACTERISTICS FOR V+ = +10V</b>						
Rise Time	t <sub>R</sub>	C <sub>L</sub> = 1000pF	8			ns
		C <sub>L</sub> = 5000pF	45			
		C <sub>L</sub> = 10,000pF	82			
Fall Time	t <sub>F</sub>	C <sub>L</sub> = 1000pF	3.2			ns
		C <sub>L</sub> = 5000pF	7.5			
		C <sub>L</sub> = 10,000pF	12.5			
Turn-On Propagation Delay Time	t <sub>D-ON</sub>	Figure 1, C <sub>L</sub> = 1000pF (Note 3)	7	12	25	ns
Turn-Off Propagation Delay Time	t <sub>D-OFF</sub>	Figure 1, C <sub>L</sub> = 1000pF (Note 3)	7	12	25	ns
Break-Before-Make Time				2.5		ns
<b>SWITCHING CHARACTERISTICS FOR V+ = +4.5V</b>						
Rise Time	t <sub>R</sub>	C <sub>L</sub> = 1000pF	12			ns
		C <sub>L</sub> = 5000pF	41			
		C <sub>L</sub> = 10,000pF	74			
Fall Time	t <sub>F</sub>	C <sub>L</sub> = 1000pF	3.0			ns
		C <sub>L</sub> = 5000pF	7.0			
		C <sub>L</sub> = 10,000pF	11.3			
Turn-On Propagation Delay Time	t <sub>D-ON</sub>	Figure 1, C <sub>L</sub> = 1000pF (Note 3)	8	14	27	ns
Turn-Off Propagation Delay Time	t <sub>D-OFF</sub>	Figure 1, C <sub>L</sub> = 1000pF (Note 3)	8	14	27	ns
Break-Before-Make Time				4.2		ns

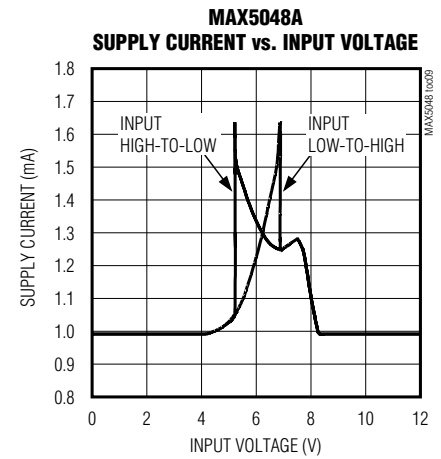
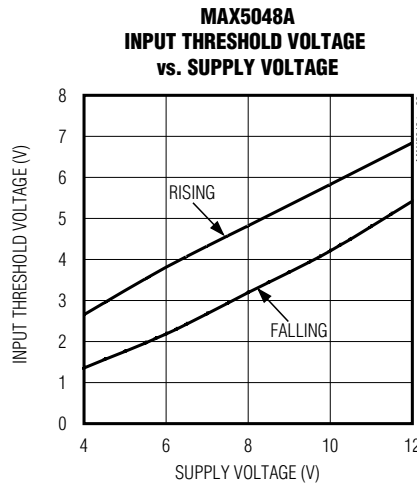
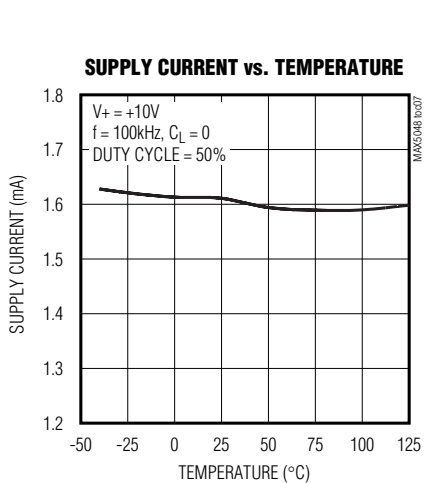
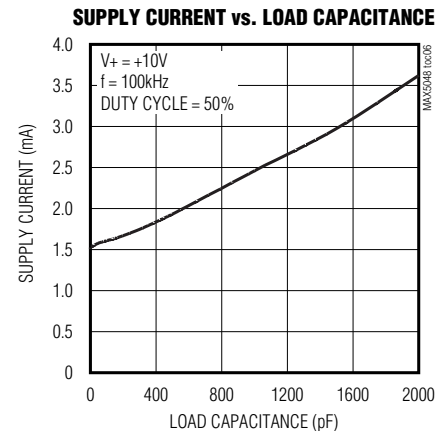
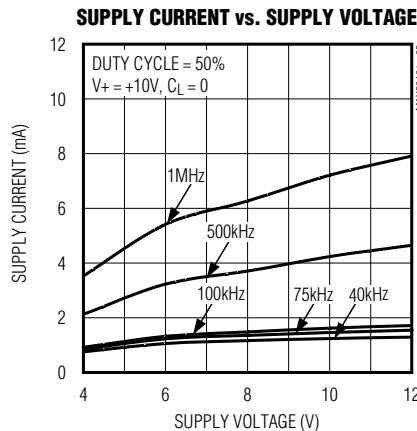
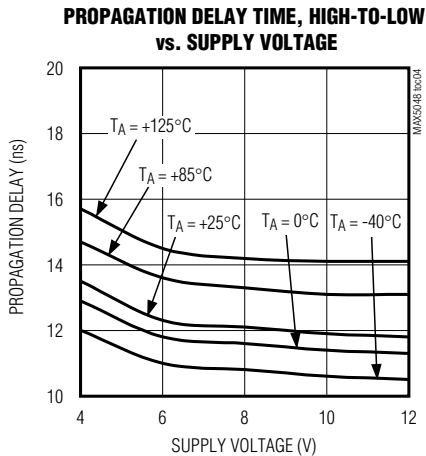
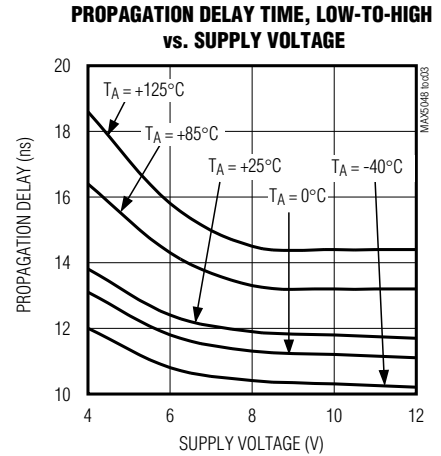
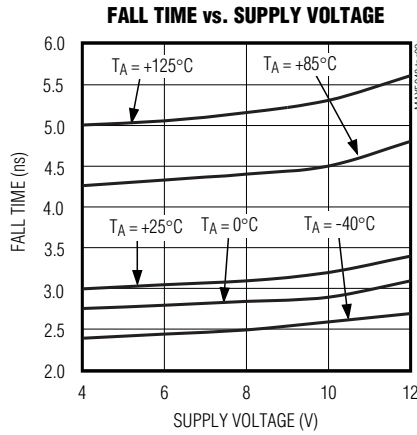
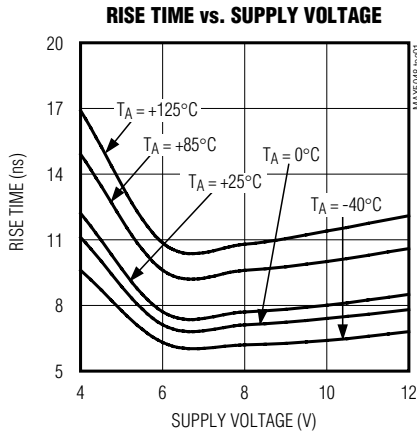
**Note 2:** All DC specifications are 100% tested at T<sub>A</sub> = +25°C. Specifications over -40°C to +125°C are guaranteed by design.

**Note 3:** Guaranteed by design, not production tested.

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## Typical Operating Characteristics

( $C_L = 1000\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



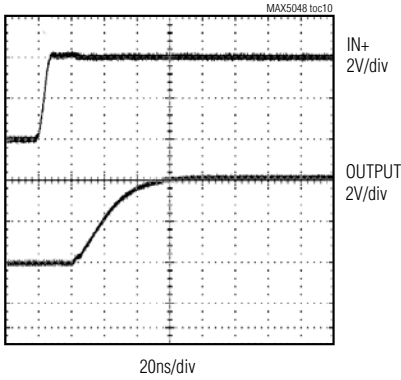
# 7.6A, 12ns, SOT23/TDFN, MOSFET Driver

## Typical Operating Characteristics (continued)

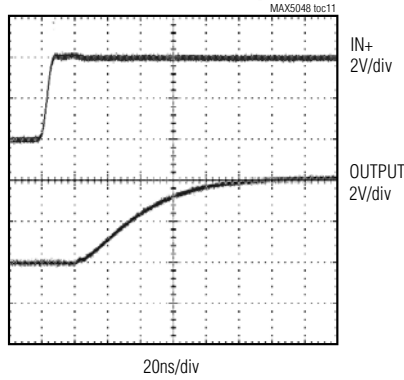
( $C_L = 1000\text{pF}$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

MAX5048

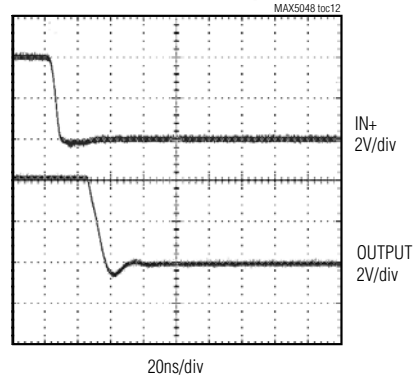
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +4\text{V}$ ,  $C_L = 5000\text{pF}$ )



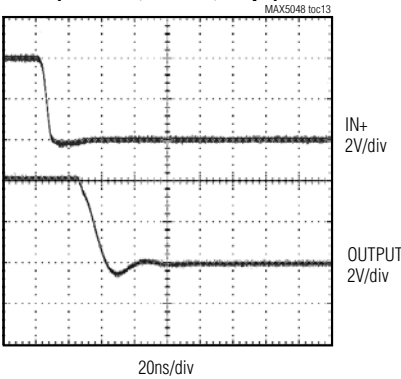
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +4\text{V}$ ,  $C_L = 10,000\text{pF}$ )



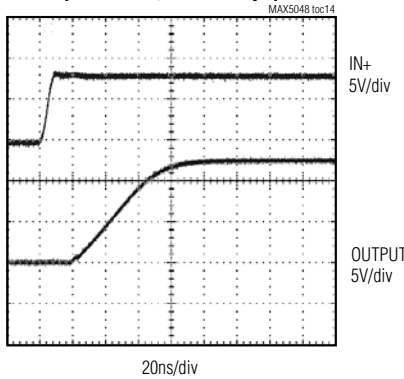
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +4\text{V}$ ,  $C_L = 5000\text{pF}$ )



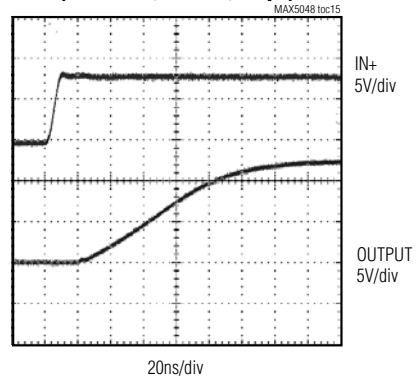
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +4\text{V}$ ,  $C_L = 10,000\text{pF}$ )



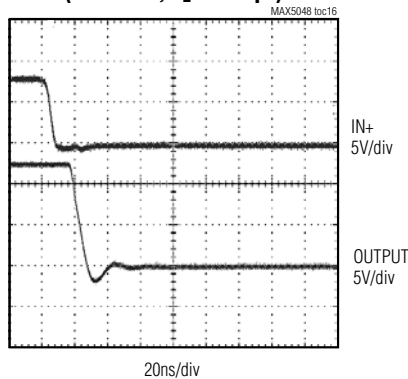
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +12\text{V}$ ,  $C_L = 5000\text{pF}$ )



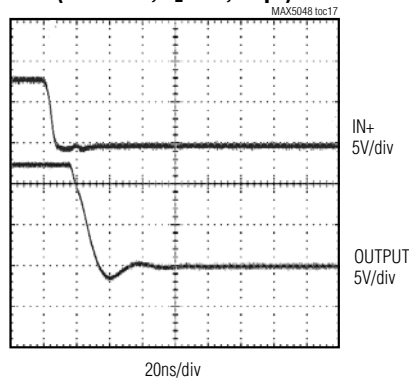
**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +12\text{V}$ ,  $C_L = 10,000\text{pF}$ )



**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +12\text{V}$ ,  $C_L = 5000\text{pF}$ )



**INPUT VOLTAGE vs. OUTPUT VOLTAGE**  
( $V_+ = +12\text{V}$ ,  $C_L = 10,000\text{pF}$ )



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### Pin Description

PIN	NAME	FUNCTION
1	V+	Power Supply. Bypass to GND with a 0.1µF ceramic capacitor.
2	P_OUT	p-Channel Open-Drain Output. Sources current for MOSFET turn-on.
3	N_OUT	n-Channel Open-Drain Output. Sinks current for MOSFET turn-off.
4	GND	Ground
5	IN-	Inverting Logic Input Terminal. Connect to GND when not used.
6	IN+	Noninverting Logic Input Terminal. Connect to V+ when not used.
—	EP	Exposed paddle. Connect to GND. Solder EP to the GND plane for improved thermal performance.

### Detailed Description

#### Logic Inputs

The MAX5048A/MAX5048Bs' logic inputs are protected against voltage spikes up to +14V, regardless of the V+ voltage. The low 2.5pF input capacitance of the inputs reduces loading and increases switching speed. These devices have two inputs that give the user greater flexibility in controlling the MOSFET. Table 1 shows all possible input combinations.

The difference between the MAX5048A and the MAX5048B is the input threshold voltage. The MAX5048A has  $V_{CC}/2$  CMOS logic-level thresholds, while the MAX5048B has TTL logic-level thresholds (see the *Electrical Characteristics*). For V+ above 5.5V,  $V_{IH}$  (typ) =  $0.5 \times (V+) + 0.8V$  and  $V_{IL}$  (typ) =  $0.5 \times (V+) - 0.8V$ . As V+ is reduced from 5.5V to 4V,  $V_{IH}$  and  $V_{IL}$  gradually approach  $V_{IH}$  (typ) =  $0.5 \times (V+) + 0.65V$  and  $V_{IL}$  (typ) =  $0.5 \times (V+) - 0.65V$ . Connect IN+ to V+ or IN- to GND when not used. Alternatively, the unused input can be used as an ON/OFF pin (see Table 1).

**Table 1. Truth Table**

IN+	IN-	p-CHANNEL	n-CHANNEL
L	L	OFF	ON
L	H	OFF	ON
H	L	ON	OFF
H	H	OFF	ON

L = Logic low

H = Logic high

### Undervoltage Lockout (UVLO)

When V+ is below the UVLO threshold, the N-channel is ON and the P-channel is OFF, independent of the state of the inputs. The UVLO is typically 3.6V with 400mV typical hysteresis to avoid chattering.

### Driver Outputs

The MAX5048A/MAX5048B provide two separate outputs. One is an open-drain P-channel, the other an open-drain N-channel. They have distinct current sourcing/sinking capabilities to independently control the rise and fall times of the MOSFET gate. Add a resistor in series with P\_OUT/N\_OUT to slow the corresponding rise/fall time of the MOSFET gate.

### Applications Information

#### Supply Bypassing, Device Grounding, and Placement

Ample supply bypassing and device grounding are extremely important because when large external capacitive loads are driven, the peak current at the V+ pin can approach 1.3A, while at the GND pin the peak current can approach 7.6A. VCC drops and ground shifts are forms of negative feedback for inverters and, if excessive, can cause multiple switching when the IN- input is used and the input slew rate is low. The device driving the input should be referenced to the MAX5048A/MAX5048B GND pin especially when the IN- input is used. Ground shifts due to insufficient device grounding may disturb other circuits sharing the same AC ground return path. Any series inductance in the V+, P\_OUT, N\_OUT and/or GND paths can cause oscillations due to the very high di/dt that results when the MAX5048A/MAX5048B are switched with any capacitive load. A 0.1µF or larger value ceramic capacitor is recommended bypassing V+ to GND and placed as close to the pins as possible. When driving very large loads (e.g., 10nF) at minimum rise time, 10µF or more of parallel storage capacitance is recommended. A ground plane is highly recommended to minimize ground return resistance and series inductance. Care should be taken to place the MAX5048A/MAX5048B as close as possible to the external MOSFET being driven to further minimize board inductance and AC path resistance.

### Power Dissipation

Power dissipation of the MAX5048A/MAX5048B consists of three components, caused by the quiescent current, capacitive charge and discharge of internal nodes, and the output current (either capacitive or resistive load). The sum of these components must be kept below the maximum power-dissipation limit.

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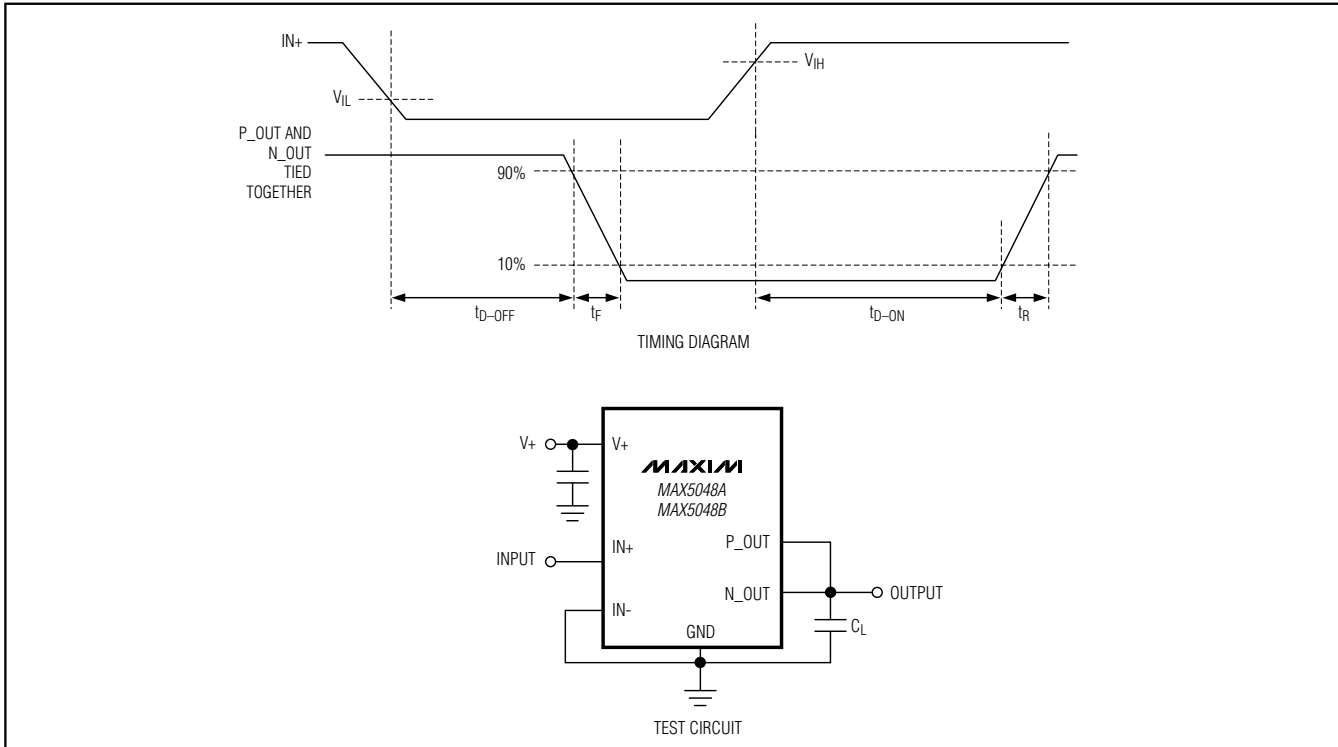


Figure 1. Timing Diagram and Test Circuit

The quiescent current is 0.95mA typical. The current required to charge and discharge the internal nodes is frequency dependent (see the *Typical Operating Characteristics*). The MAX5048A/MAX5048B power dissipation when driving a ground referenced resistive load is:

$$P = D \times R_{ON(MAX)} \times I_{LOAD}^2$$

where D is the fraction of the period the MAX5048A/MAX5048Bs' output pulls high, R<sub>ON (MAX)</sub> is the maximum on-resistance of the device with the output high (P-channel), and I<sub>LOAD</sub> is the output load current of the MAX5048A/MAX5048B.

For capacitive loads, the power dissipation is:

$$P = C_{LOAD} \times (V+)^2 \times FREQ$$

where C<sub>LOAD</sub> is the capacitive load, V+ is the supply voltage, and FREQ is the switching frequency.

### Layout Information

The MOSFET drivers MAX5048A/MAX5048B source-and-sink large currents to create very fast rise and fall edges at the gate of the switching MOSFET. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The

following PC board layout guidelines are recommended when designing with the MAX5048A/MAX5048B:

- Place one or more 0.1µF decoupling ceramic capacitor(s) from V+ to GND as close to the device as possible. At least one storage capacitor of 10µF (min) should be located on the PC board with a low resistance path to the V+ pin of the MAX5048A/MAX5048B.
- There are two AC current loops formed between the device and the gate of the MOSFET being driven. The MOSFET looks like a large capacitance from gate to source when the gate is being pulled low. The active current loop is from N\_OUT of the MAX5048A/MAX5048B to the MOSFET gate to the MOSFET source and to GND of the MAX5048A/MAX5048B. When the gate of the MOSFET is being pulled high, the active current loop is from P\_OUT of the MAX5048A/MAX5048B to the MOSFET gate to the MOSFET source to the GND terminal of the decoupling capacitor to the V+ terminal of the decoupling capacitor and to the V+ terminal of the MAX5048A/MAX5048B. While the charging current loop is important, the discharging current loop is critical. It is important to minimize the physical distance and the impedance in these AC current paths.

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- In a multilayer PC board, the component surface layer surrounding the MAX5048A/MAX5048B should consist of a GND plane containing the discharging and charging current loops.

### Chip Information

TRANSISTOR COUNT: 676  
PROCESS: BiCMOS

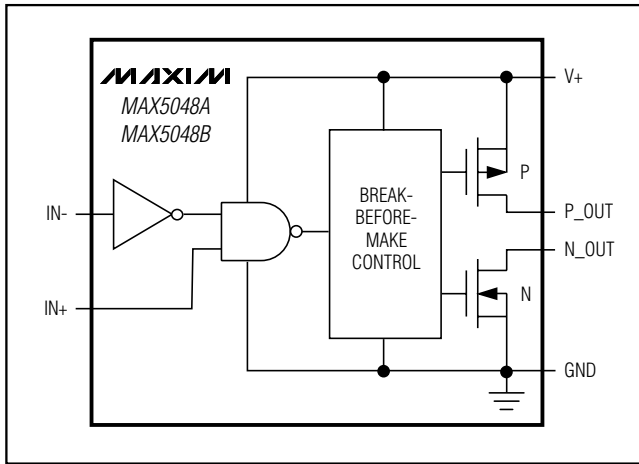


Figure 2. MAX5048A/MAX5048B Functional Diagram

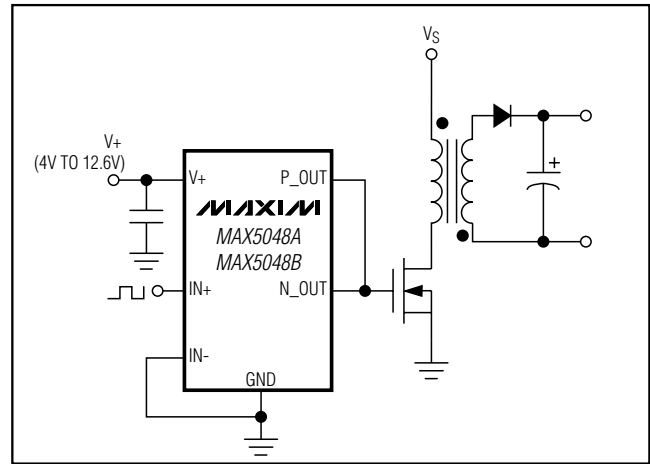


Figure 3. Noninverting Application

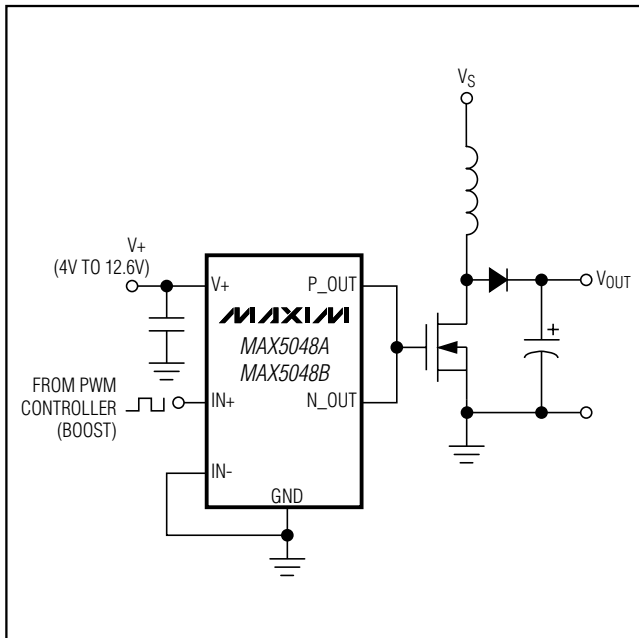


Figure 4. Boost Converter

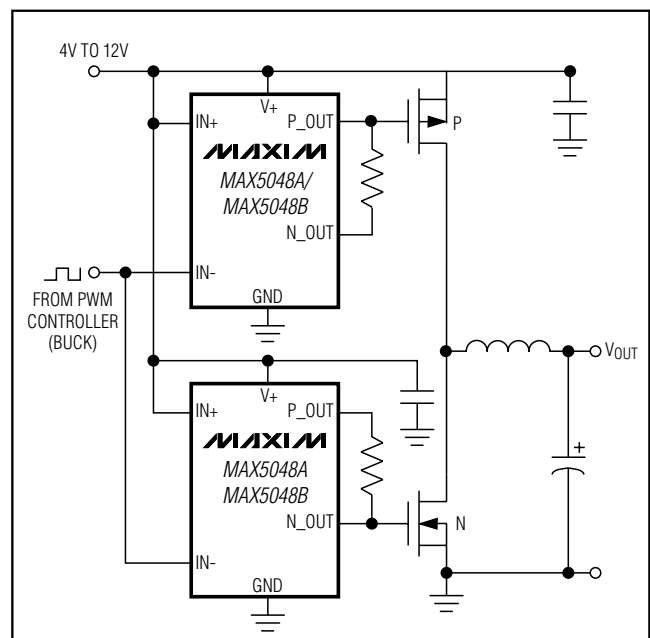


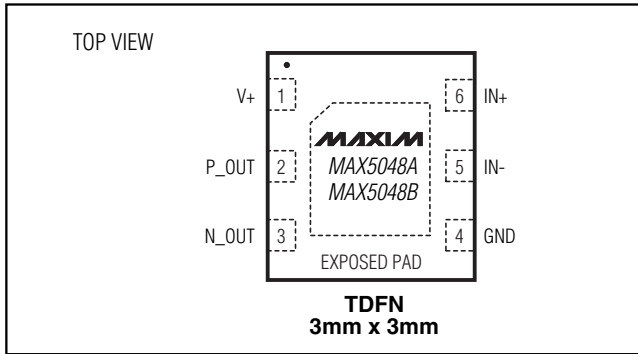
Figure 5. MAX5048A/MAX5048B in High-Power Synchronous Buck Converter



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**MAX5048**

## Pin Configurations (continued)



## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

SEE NOTE 5  
EXAMPLE  
TOP MARK

PIN 1  
I.D. DOT  
(SEE NOTE 6)

PIN #1

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60	REF.
e1	1.90	BSC.
e	0.95	BSC.
a	0°	10°

NOTES:

- ALL DIMENSIONS ARE IN MILLIMETERS.
- FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
- PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
- PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
- PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
- PIN 1 I.D. DOT IS 0.3 MM  $\phi$  MIN. LOCATED ABOVE PIN 1.
- MEETS JEDEC MO17B, VARIATION AB.
- SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
- LEAD TO BE COPLANAR WITHIN 0.1 MM.

TITLE PACKAGE OUTLINE, SOT 6L BODY		
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-DRAWING NOT TO SCALE-

6LSOTLEPS



# 7.6A, 12ns, SOT23/TDFN, MOSFET Driver

MAX5048

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS								
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	NO

**NOTES:**

- ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
- COPLANARITY SHALL NOT EXCEED 0.08 mm.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
- DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
- "N" IS THE TOTAL NUMBER OF LEADS.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

		
TITLE: PACKAGE OUTLINE, 6, 8, 10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm		
APPROVAL	DOCUMENT CONTROL NO.	REV.
	21-0137	G 2/2

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