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SAK-CIC310-OSMX2HT

FlexRay Communication Controller

IFLEX

Step A11

Microcontrollers

Never stop thinking

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1 Summary of Features

The major functions supported by the SAK-CIC310-OSMX2HT are summarized in this section.

- A powerful FlexRay v2.1 Protocol Controller
  - Certified to be conform with FlexRay protocol specification v2.1
  - Data rates of up to 10 MBit/s on each channel
  - Up to 128 message buffers configurable
  - 8 Kbyte of Message RAM for storage of e.g. 128 message buffers with maximum 48 Byte data field or up to 30 messages with 254 Byte data field
  - Configuration of message buffers with different payload lengths
  - One configurable receive FIFO
  - Each message buffer can be configured as Receive Buffer, as Transmit Buffer, or as part of the receive FIFO
  - Host access to message buffers via Input and Output Buffer.
    Input Buffer: holds message to be transferred to the Message RAM
    Output Buffer: holds message read from the Message RAM
  - Filtering for frame ID, channel ID, and cycle counter
  - Network Management supported
  - Two Channels enabling one redundant FlexRay Bus
  - All data formats are little-endian
- Independent 8-Channel DMA Controller
  - 8 selectable request inputs per DMA channel
  - Programmable priority of DMA channels within the DMA sub-block (2 levels)
  - Software and hardware DMA request generation
  - Hardware requests by selected peripherals
  - Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated.
  - Programmable address modification
  - Support of circular buffer addressing mode
  - Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
  - Individual register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register

  - Flexible interrupt generation
- 16-bit External Memory Interface Unit (XMU)
  - 16-bit wide data bus (D[15:0])
  - Automatic data assembly/disassembly operation
  - Data width of external bus master can be 8-bit or 16-bit
  - 13-bit wide address bus (A[12:0])
  - Address extension mechanism to 32-bit
  - Read (RD) and write (WR) Bus control signal
  - External synchronous/asynchronous wait state bus control signal (WAIT)
  - External master chip select (CSFPI) to access on-chip devices connected to the crossbar switch
- High performing on-chip crossbar bus structure
  - 32-bit crossbar slave interface for FlexRay
  - 32-bit crossbar slave interface for Ports and System Control
  - 32-bit crossbar slave interface for MLI communication
  - 32-bit crossbar slave interface for MLI and DMA peripheral
  - 32-bit crossbar master interface for Host Communication Interfaces
  - 32-bit crossbar master interface for DMA
- Versatile High-Speed Synchronous Serial Channels (SSC) for Host Communication
  - Full-duplex or half-duplex operation
  - Automatic half-duplex pad control
  - SSC supports proprietary protocol to drive an integrated move engine
  - Maximum Master Mode baud rate: f_{SSC} / 2
    Maximum baud rate (master mode) of 40 MBit/s (@ 80 MHz module clock)
  - Maximum Slave Mode baud rate: f_{SSC} / 4
    Maximum baud rate (slave mode) of 20 MBit/s (@ 80 MHz module clock)
- Versatile High-Speed Micro Link interfaces (MLI) for serial inter-processor communication and Host Communication
  - Fully transparent read/write access supported (including remote programming)
  - Complete address range of target controller available
  - Special protocol to transfer data, address offset, or address offset and data
  - Error control using a parity bit
  - 32-bit, 16-bit, and 8-bit data transfers
  - Address offset width: from 1 to 16 bit
  - Baud rate: f_{MLI} / 2 (symmetric shift clock approach),
    baud rate definition by the corresponding fractional divider
    Maximum baud rate of 40 MBit/s (@ 80 MHz module clock)
- Full automotive temperature range: -40°C to +125°C
- 26 digital general purpose I/O lines, 20 digital general purpose input lines
- Digital I/O ports with 3.3 V capability
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V

- One Package Option only (PG-TQFP-64)

As the FlexRay Protocol Controller is on a separate chip, the so called standalone Communication Controller, the access is handled via serial or parallel communication links. These three types of link options are discussed in the following chapter.

2 Functional Description

The SAK-CIC310-OSMX2HT IC is supposed to be connected to devices of the Infineon AUDO-NG 32bit microcontroller device family. The connection has to be done in a way that today's AUDO-NG 32-bit microcontroller MLI, ASC, or SSC interfaces remain untouched. On the other hand the FlexRay Communication controller requires communication bandwidth of 10 MBit/s and more to download the full message bandwidth of the two FlexRay links. Beside this requirement additionally the SAK-CIC310-OSMX2HT needs to be operative with a minimum pin account and area. Therefore two small serial interfaces (MLI, SSC) and an additional parallel interface are implemented.

For the SAK-CIC310-OSMX2HT concept three options are implemented in parallel to minimize the risk and to increase the options for a system composed out of the SAK-CIC310-OSMX2HT and an AUDO-NG 32-bit microcontroller device and still to handle the application requirements. These three interfaces are the SSC Interface (usable as SPI and synchronous ASC Interface), a parallel Interface, and the Micro Link Interface (MLI). All AUDO-NG 32-bit microcontroller family member are equipped with serial interfaces (ASC and SSC).

Three options are presented for the system solution based on these three communication interfaces.

2.1 MLI Host Link (Option One)

The first and preferred option is to connect the SAK-CIC310-OSMX2HT via the MLI interface to the AUDO-NG 32bit microcontroller family. The MLI has the advantage realizing a fast and smart communication interface with a low pin count and SPI like SW protocol handling. The transmission rate is high enough to handle the data traffic that is generated from the SAK-CIC310-OSMX2HT FlexRay Protocol engine to the AUDO-NG 32-bit microcontroller device and vice versa.

MLI Feature Set

- Serial communication from the MLI transmitter to MLI receiver of another controller
- Fully transparent read/write access supported (including remote programming)
- Complete address range of target controller available
- Special protocol to transfer data, address offset, or address offset and data
- Error control using a parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Address offset width: from 1 to 16 bit
- Baud rate: f_{MLI} / 2 (symmetric shift clock approach),
  baud rate definition by the corresponding fractional divider
  Maximum baud rate of 40 MBit/s (@ 80 MHz module clock)

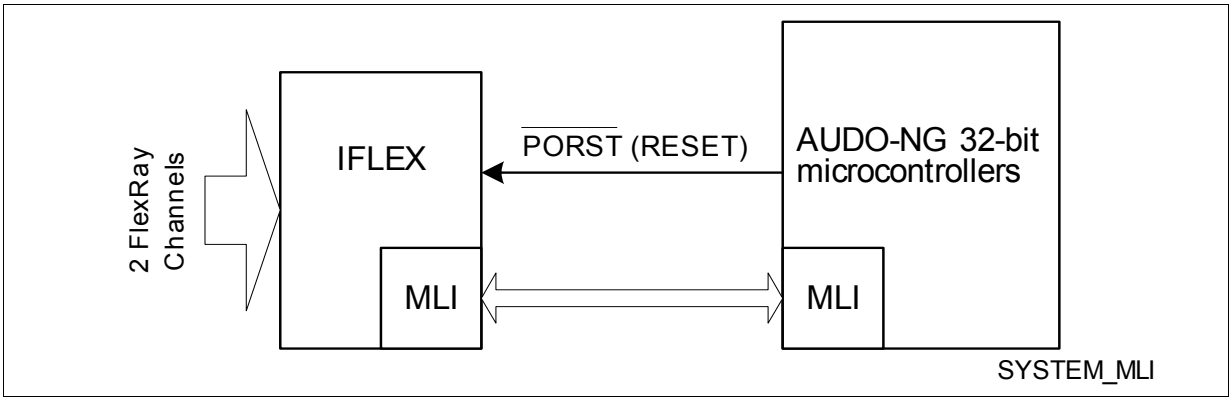

Figure 1 SAK-CIC310-OSMX2HT and AUDO-NG 32bit Microcontroller Device Connected via MLI

The connectivity features of the MLI enables also connecting two different SAK-CIC310-OSMX2HT devices with the host This requires two sets of MLI interface signals bonded out of the host MLI.

2.2 SSC Host Link (Option Two)

The second option is to connect the SAK-CIC310-OSMX2HT via a SSC (SPI) interface to e.g. the AUDO-NG 32-bit microcontroller family or the (X)C166 16-bit microcontroller family. Pin count are in a similar range compared with the MLI interface. The SW handling cost more host performance than the MLI interface requires. The single SPI link does not provide enough bandwidth to handle the maximum bandwidth FlexRay may require, but fulfil the needs of applications with lower bandwidth requirements.

SSC Feature Set

- Master and slave mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16-bit
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Baud rate (master): f_{SSC} / 2;
  Maximum master mode baud rate of 40 MBit/s (@ 80 MHz module clock)
- Baud rate (slave): f_{SSC} / 4;
  Maximum slave mode baud rate of 20 MBit/s (@ 80 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition

  – On a receiver full condition
  – On an error condition (receive, phase, baud rate, transmit error)
- SSC supports proprietary protocol to drive an integrated move engine.

Note: Even so the SSC can be flexible configured, the SSC move engine can only handle 16 bit, Slave Mode, Full-duplex mode and Half-duplex mode, leading edge is high to low, shift on leading edge.

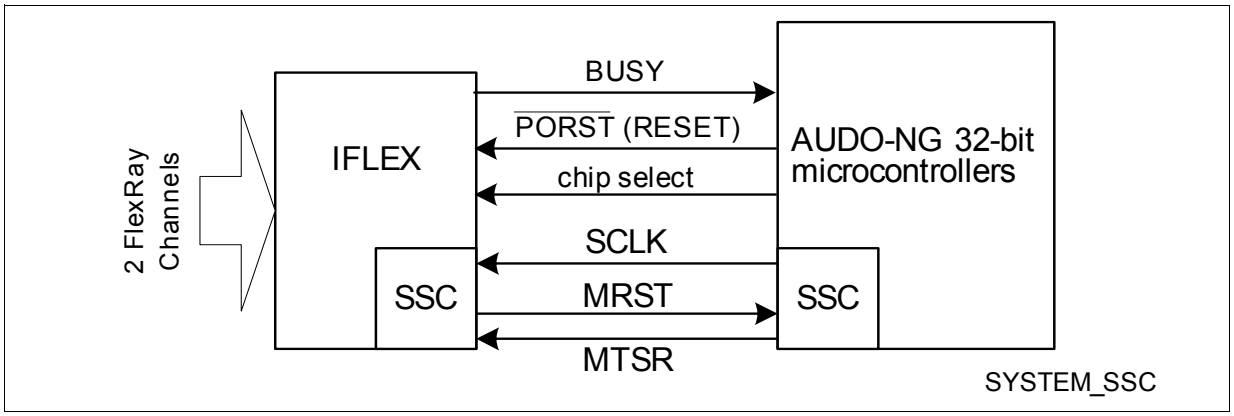

Figure 2 SAK-CIC310-OSMX2HT and AUDO-NG 32bit Microcontroller Device Connected by SPI

The SSC is configured in a manner it could communicate to the ASC of the TriCore family. The TriCore ASC is configured in a manner using both RXDxA and RXDxB of the ASC as MRST and MTSR and the TXDxA or TXDxB as Clock.

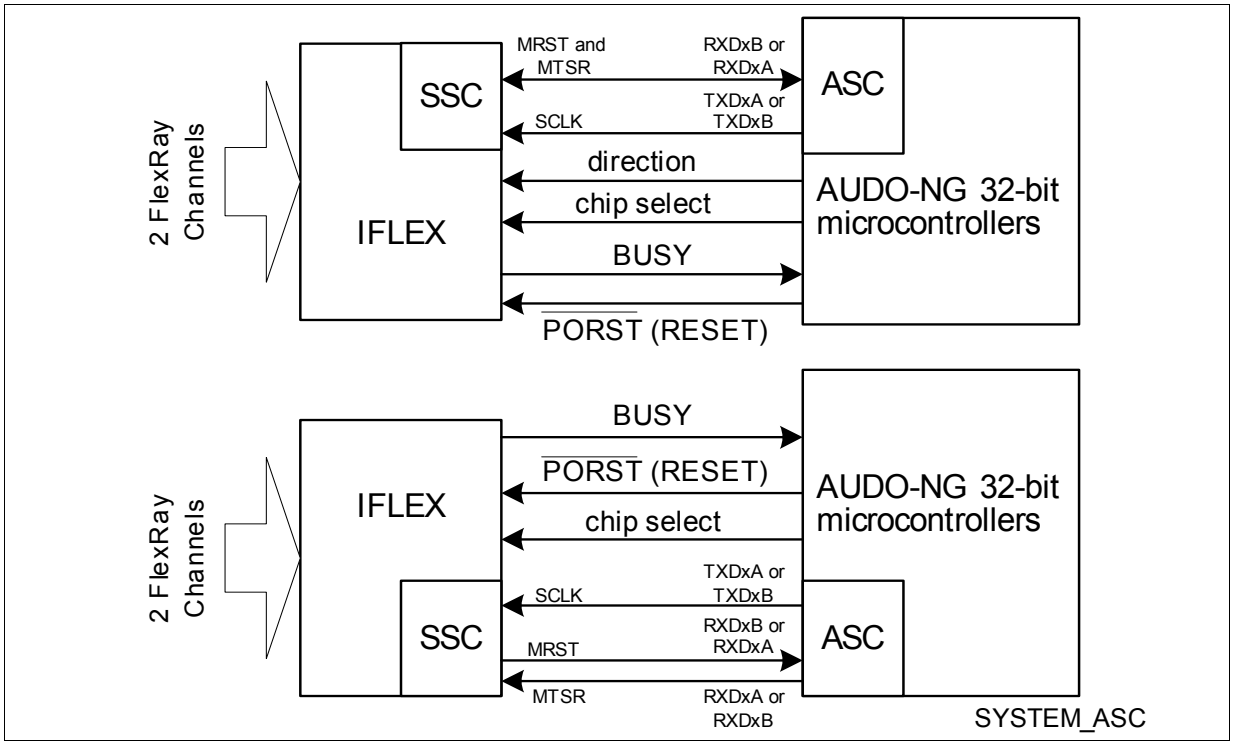

Figure 3 SAK-CIC310-OSMX2HT and AUDO-NG 32bit Microcontroller Device Connected via ASC

2.3 Parallel Host Link (Option Three)

The third option is to connect the SAK-CIC310-OSMX2HT via the parallel interface e.g. the AUDO-NG 32-bit microcontroller family or the (X)C166 16-bit microcontroller family. The parallel interface provides enough bandwidth to handle the maximum data traffic generated by the SAK-CIC310-OSMX2HT FlexRay Protocol Controller to the AUDO-NG 32-bit microcontroller device and vice versa.

XMU Features

- 16-bit wide data bus (D[15:0])
  - Data width of external bus master can be 8 or 16 bit.
  - Automatic data assembly/disassembly operation
- 13-bit wide address bus (A[12:0])
- Bus control signals
  - Read ($\overline{RD}$) and write ($\overline{WR}$)
  - Two byte control signals ($\overline{BC}$[1:0])
  - External synchronous/asynchronous wait state control ($\overline{WAIT}$)
  - External master chip select ($\overline{CSFPI}$) to access on-chip devices connected to the MIF Bus

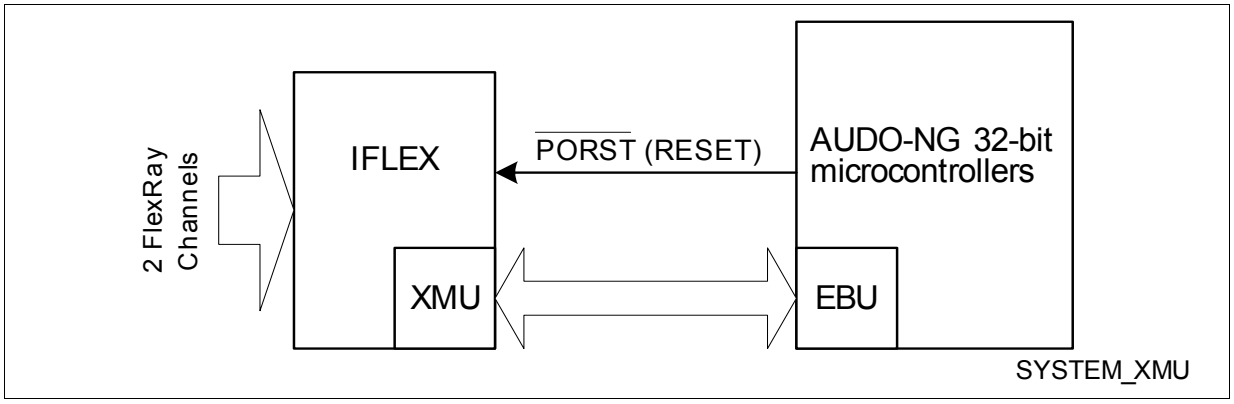

Figure 4 SAK-CIC310-OSMX2HT and AUDO-NG 32bit Microcontroller Device Connected via XMU

2.4 DMA Controller

The Direct Memory Access (DMA) Controller of the SAK-CIC310-OSMX2HT transfers data from data source locations to data destination locations without intervention of the Host Controller. One data move operation is controlled by one DMA channel. Eight DMA channels are provided. The Bus Switch provides the connection of the DMA Sub-Block to the ERAY Peripheral, Host Communication peripheral, Ports, and an MLI bus interface. **Figure 5** shows the implementation details and interconnections of the DMA module.

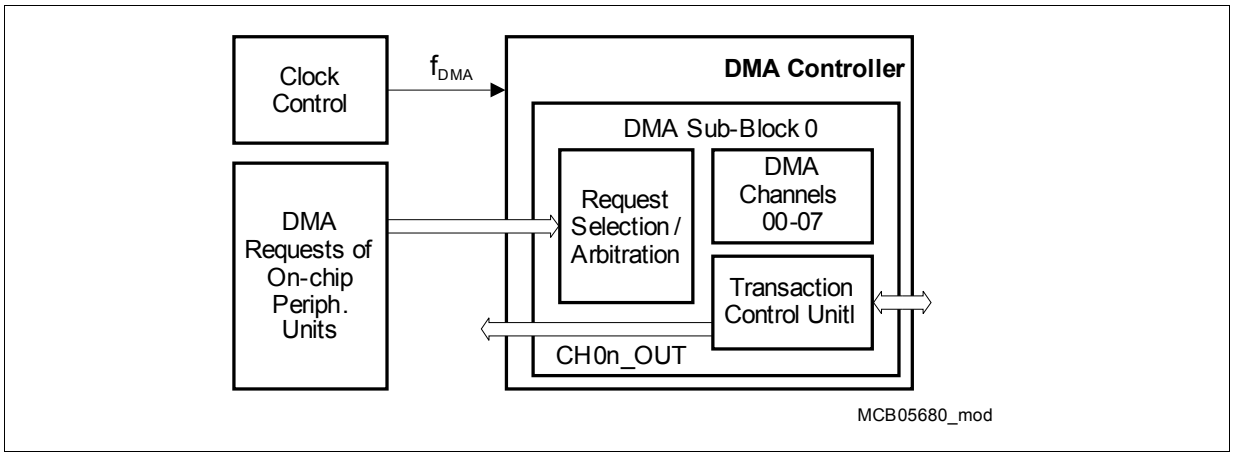

Figure 5 DMA Controller Block Diagram

Features

- 8 independent DMA channels
  - Up to 8 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within a DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- Programmable priority of the DMA Sub-Blocks on the crossbar switch
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered).
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated.
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4 GByte address range
  - Support of circular buffer addressing mode
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Micro Link bus interface support
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- Read/write requests of the System Bus Side to the Remote Peripherals are bridged to the Remote Peripheral Bus (only the DMA is master on the RPB)

3 General Device Information

This section provides an overview of the entire architecture of the SAK-CIC310-OSMX2HT companion chip.

The overall building blocks of the SAK-CIC310-OSMX2HT are:

- FlexRay v2.1 protocol controller
- Slave (SPI) SSC interface
- MLI interface
- Parallel external memory interface unit (XMU).
- 8 independent channel DMA
- Dual Voltage Power Supply
- One Package Option only (PG-TQFP-64)

3.1 Block Diagram

Figure 6 summarizes the overall architecture of the SAK-CIC310-OSMX2HT.

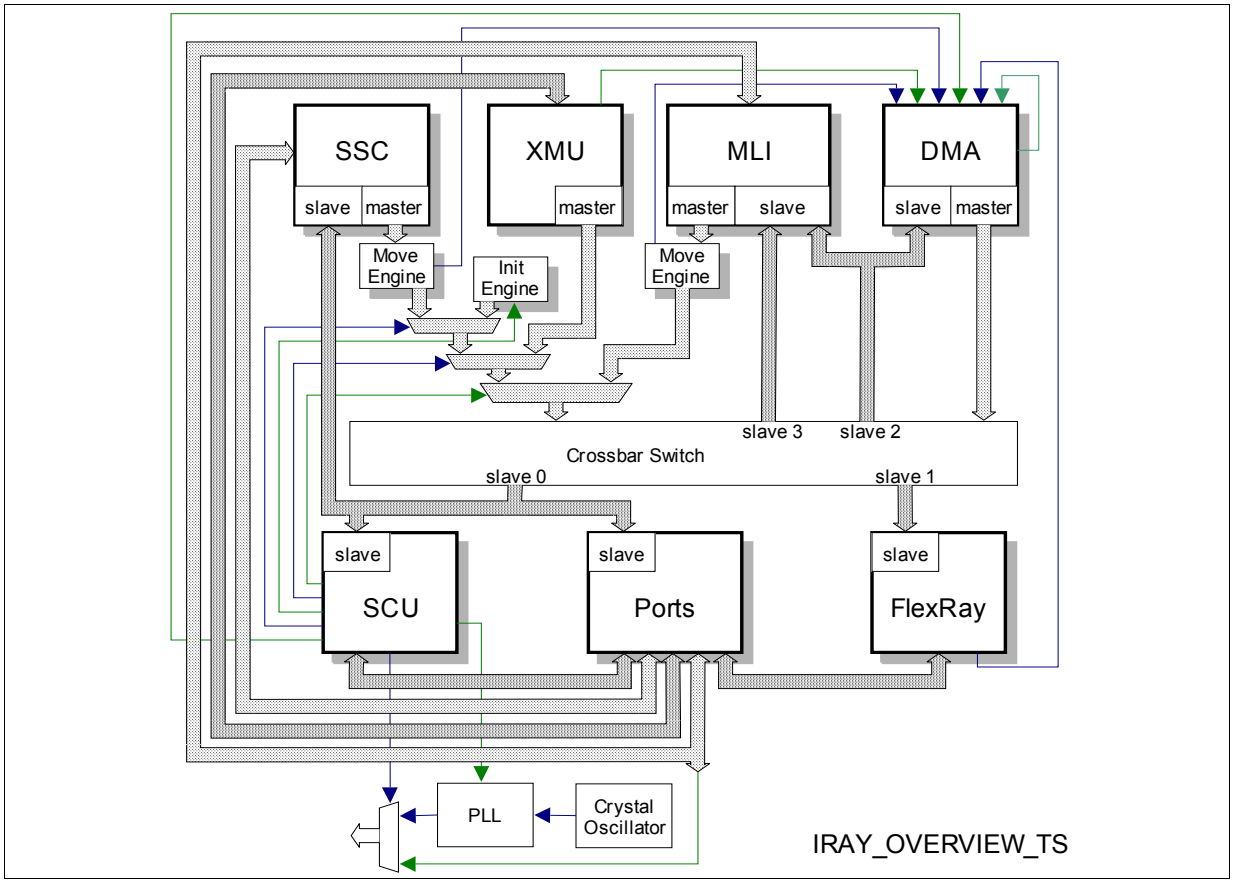

Figure 6 IFLEX Block Diagram

In **Figure 6** the block diagram of the IFLEX is shown. This concept allows the access to the FlexRay Protocol Controller for the host CPU without sacrificing any of the features

of the FlexRay Protocol Controller. This can be achieved, as all registers of the FlexRay Protocol Controller are mapped to the crossbar switch. This crossbar switch can be accessed via one of the three host interfaces, which were introduced in **Chapter 2**. The interface selection is done via the mode signals MODE[0] and MODE[1], which can be directly connected to the supply voltage or via pull-up/down resistors (of about 10-47 kΩ).

Table 1 Host Interface Select

Mode[1]	Mode[0]	Selected Host Interface
0_B	0_B	**XMU Host Interface activate**
1_B	0_B	
0_B	1_B	**MLI Host Interface activate**
1_B	1_B	**SSC Host Interface activate**

The cross bar switch allows two parallel data operations, one initiated by the DMA, the other by either the MLI, XMU, or SSC move engine and serving different ports of the crossbar switch to slave interfaces. The address ranges of the slave ports are:

1. Slave Port 0 serves the address range from 0000 0800_H to 0000 $0FFF_H$
2. Slave Port 1 serves the address range from 0000 1000_H to 0000 $1FFF_H$
3. Slave Port 2 serves the address range from 0000 0200_H to 0000 $07FF_H$
4. Slave Port 3 serves all addresses 0000 0000_H to 0000 $01FF_H$ and 0000 2000_H to FFFF $FFFF_H$

So apart from a possible loss of speed due to the serial interfaces the complete functionality of the FlexRay Protocol Controller is maintained.

The crossbar switch domain is completely separated from the address domain on the CPU chip. The addresses of all modules on the FlexRay Communication Controller are 32-bit addresses. Transactions between the CPU and the SSC are executed with the SSC transmission protocol and a high level protocol to drive the move engine, transactions between the MLI and the CPU use the MLI transmission protocol and transactions between the XMU and the CPU are based on the XMU transmission protocol.

Each transaction via any of the three host interfaces is defined by address, data, data width and type of frame. The address, where data is read from or written to, is related to the crossbar switch address domain. The data width may be 8, 16, or 32 bit for the MLI, 8 or 16 bit for the XMU, and 16 bit for the SSC. The type of frame may be a read or write access or an answer frame to a read access. The Move Engines request access to the bus via the Bus Master. The Flex Protocol Controller and the MLI may send an interrupt to the DMA.

There are several cases:

- The MLI, XMU, or the SSC interfaces requests to write.
- The MLI, XMU, or the SSC interfaces requests to read.
- The FlexRay Communication Controller requests to write.
- A general peripheral beside the FlexRay Communication Controller requests to read.

Half-word (16-bit) accesses, read and write, are only allowed for half-word aligned addresses (even addresses). Therefore if doing a half-word (16-bit) access, the least significant address bit (A0) is ignored (assumed to be to 0) by the modules of the SAK-CIC310-OSMX2HT. Therefore if addressing a half-word with an odd address n, a half-word is read instead from address n-1 (ignoring least significant address bit: n AND FFFF $FFFE_H$).

Word accesses (32-bit), read and write, are only allowed for word aligned addresses (addresses modulo 4 = 0). Therefore if doing a word (32-bit) access, the two least significant address bits (A0 and A1) are ignored (assumed to be to 0) by the modules of the SAK-CIC310-OSMX2HT. Therefore if addressing a word with an address n (n modulo 4 = {1,2,3}), a word is read instead from address (n AND FFFF $FFFC_H$) (ignoring the two least significant address bits).

3.2 Pin Definition and Functions

To enable a clean power-up, the majority of pins have a “enable pad supply” (ENPS) function. This ENPS is pad supply (V_{DDP}) driven. So only if the pad supply and the core supply is stable, the output pads may be activated. Four pins do no support ENPS: JTAGEN, PORST, XTAL1, and XTAL2. In case of a low voltage signal at the input port ENPS (PORST) the output port PAD activates the weak pull-up and disables the output driver independent of the port direction. In case of a high voltage signal at the input port ENPS (PORST) the bidirectional platform pads operate in normal mode.

3.2.1 Package Outline

The package outline and the signals of the pins are summarized in **Figure 7**.

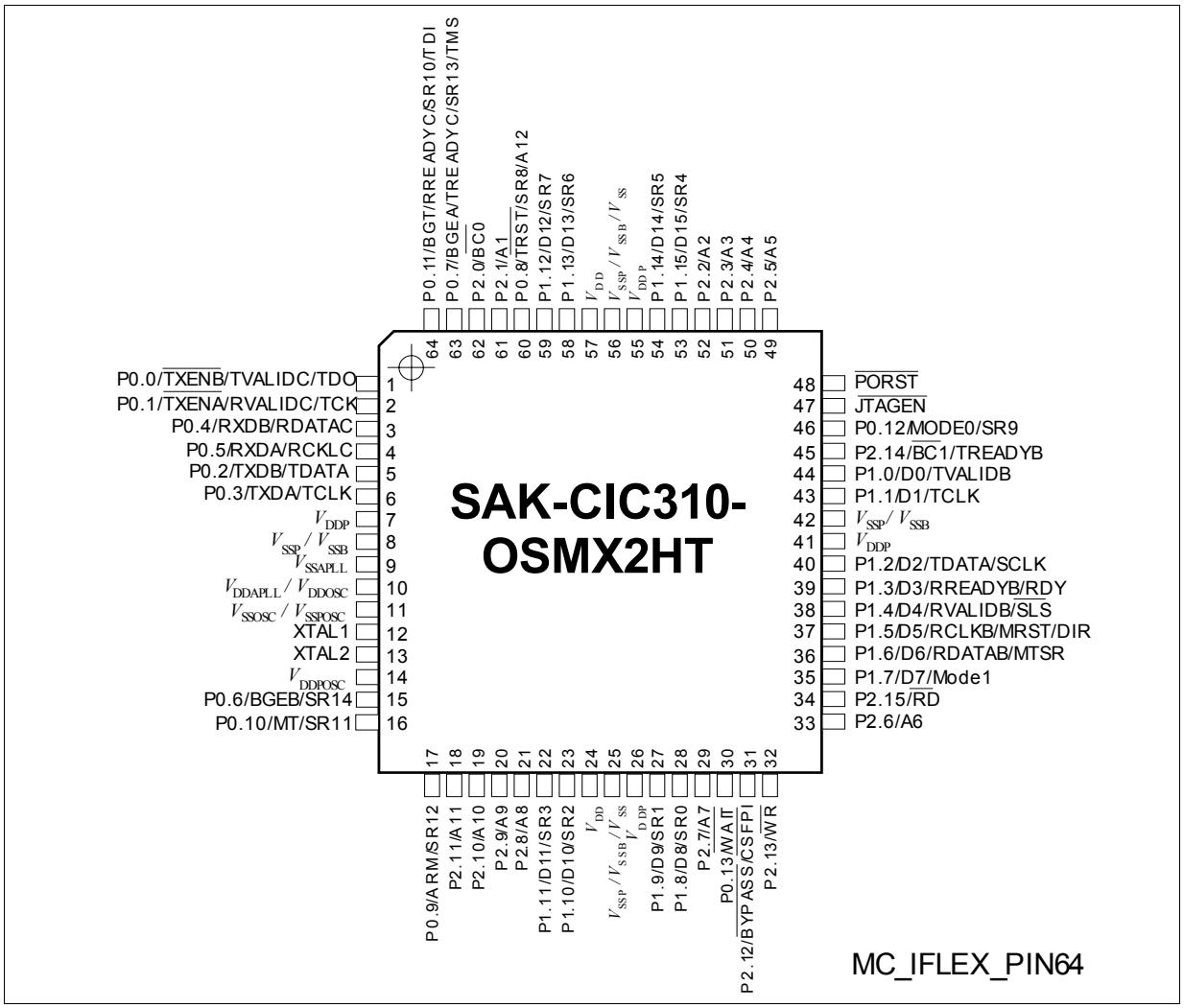

Figure 7 SAK-CIC310-OSMX2HT Pinning: PG-TQFP-64 Package (top view)

3.2.2 Pin Description

Table 2 Pin Definitions and Functions

Symbol	Pin	I/O	Function
	PG-TQFP-64		
FlexRay Bus Interface			
$\overline{\text{TXENB}}$/ TVALIDC/ TDO	1	I/O	**Port 0 line 0** **FlexRay Transmit Enable** (Channel B) **JTAG Module Serial Data Output** JTAG Enable Mode only **MLI Transmit Channel Valid Output**
$\overline{\text{TXENA}}$/ RVALIDC/ TCK	2	I/O	**Port 0 line 1** **FlexRay Transmit Enable** (Channel A) **JTAG Module Clock Input (TCK)** JTAG Enable Mode only **MLI Receive Channel Valid Input C**
RXDB/ RCLKC	3	I	**Port 0 line 4** **FlexRay Data Receiver Input** (Channel B) **MLI Receive Channel Clock Input C**
RXDA/ RDATAC	4	I	**Port 0 line 5** **FlexRay Data Receiver Input** (Channel A) **MLI Receive Channel Data Input C**
TXDB/ TCLK	5	I/O	**Port 0 line 2** **FlexRay Data Transmitter Output** (Channel B) **MLI Transmit Channel Clock Output**
TXDA/ TDATA	6	I/O	**Port 0 line 3** **FlexRay Data Transmitter Output** (Channel A) **MLI Transmit Channel Data Output**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
BGEB/ SR14	15	I	**Port 0 line 6** **FlexRay Bus Guardian Enable** (Channel B) **Interrupt Request input line 14** The logic 0 level at this pin indicates an interrupt request from the external host device.
MT/ SR11	16	I/O	**Port 0 line 10** **FlexRay Bus Guardian Macro Tick** FlexRay corrected Macro Tick Clock **Interrupt Request Input/Output line 11** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
ARM/ SR12	17	I/O	**Port 0 line 9** **FlexRay Bus Guardian Arm Signal** Indicates the begin of a communication cycle to the bus guardian. **Interrupt Request Input/Output line 12** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
BGEA/ TMS/ SR13/ TREADYC	63	I	**Port 0 line 7** **FlexRay Bus Guardian Enable** (Channel A) **JTAG Module State Machine Control Input** JTAG Enable Mode only **Interrupt Request input line 13** The logic 0 level at this pin indicates an interrupt request from the external host device. **MLI Transmit Channel Ready Input C**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
BGT/ TDI/ SR10/ RREADYC	64	I/O	**Port 0 line 11** **FlexRay Bus Guardian Tick** Used by the Macro Tick Watchdog of the Bus Guardian as Time Base **JTAG Module Serial Data Input** JTAG Enable Mode only. **Interrupt Request Input/Output line 10** The logic 0 level at this pin indicates an interrupt request from/to the external host device. **MLI Receive Channel Ready Output C**
Host Interfaces			
BC[1]/ TREADYB	45	I	**Port 2 line 14** MODE = 00_B: **XMU Byte control line 1** Controls the byte access to corresponding byte location D[15:8] MODE = 01_B**:** **MLI Transmit Channel Ready Input B** MODE = 10_B: **XMU Byte control line 1** Controls the byte access to corresponding byte location D[15:8] MODE = 11_B: **Port 2 line 14** (input only)
D0/ TVALIDB	44	I/O	**Port 1 line 0** MODE = 00_B: **XMU** Data bus Line 0 MODE = 01_B**:** **MLI Transmit Channel Valid Output** MODE = 10_B: **XMU** Data Bus line 0 MODE = 11_B: **Port 1 line 0** (Input/Output)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D1/ TCLK	43	I/O	**Port 1 line 1** MODE = 00_B: **XMU** Data Bus Line 1 MODE = 01B: **MLI Transmit Channel Clock Output** MODE = 10_B: **XMU** Data Bus Line 1 MODE = 11_B: **Port 1 line 1** (Input/Output)
D2/ TDATA/ SCLK	40	I/O	**Port 1 line 2** MODE = 00_B: **XMU** Data Bus Line 2 MODE = 01_B**:** **MLI Transmit Channel Data Output** MODE = 10_B: **XMU** Data Bus Line 2 MODE = 11_B: **SSC Serial Channel Clock** (Input/Output)
D3/ RREADYB / RDY	39	I/O	**Port 1 line 3** MODE = 00_B: **XMU** Data Bus Line 3 MODE = 01_B**:** **MLI Receive Channel Ready Output B** MODE = 10_B: **XMU** Data Bus Line 3 MODE = 11_B: **SSC Ready Signal** (Output) Output signal indicating that the standalone device is ready for data transfer**.**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D4/ RVALIDB/ SLS	38	I/O	**Port 1 line 4** MODE = 00_B: **XMU** Data Bus Line 4 MODE = 01_B**:** **MLI Receive Channel Valid Input B** MODE = 10_B: **XMU** Data Bus Line 4 MODE = 11_B: **SSC Select Slave** Input used to enable SSC action when active.
D5/ RCLKB/ MRST/ DIR	37	I/O	**Port 1 line 5** MODE = 00_B: **XMU** Data Bus Line 5 MODE = 01_B**:** **MLI Receive Channel Clock Input B** MODE = 10_B: **XMU** Data Bus Line 5 MODE = 11_B: **SPI Master Receive Slave Transmit** Serial data output Alternative: Direction of SPI Half-Duplex communication.
D6/ RDATAB/ MTSR/ MRST	36	I/O	**Port 1 line 6** MODE = 00_B: **XMU** Data Bus Line 6 MODE = 01_B**:** **MLI Receive Channel Data Input B** MODE = 10_B: **XMU** Data Bus Line 6 MODE = 11_B: **SPI Master Transmit Slave Receive** Serial data input **SPI Slave Transmit Master Receive** Serial data input (half duplex mode)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
Parallel Host Interface			
$\overline{BC}$[0]	62	I	**Port 2 line 0** MODE = 00_B: **XMU Byte control line 0** Controls the byte access to corresponding byte location D[7:0] MODE = 01_B: **Port 2 line 0** MODE = 10_B: **XMU Byte control line 0** Controls the byte access to corresponding byte location D[7:0] MODE = 11_B: **Port 2 line 0**
A[1]	61	I	**Port 2 line 1** MODE = 00_B: **XMU Address bus line 1** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 1** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 1**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
A[2]	52	I	**Port 2 line 2** MODE = 00_B: **XMU Address bus line 2** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 2** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 2**
A[3]	51	I	**Port 2 line 3** MODE = 00_B: **XMU Address bus line 3** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 3** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 3**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
A[4]	50	I	**Port 2 line 4** MODE = 00_B: **XMU Address bus line 4** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 4** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 4**
A[5]	49	I	**Port 2 line 5** MODE = 00_B: **XMU Address bus line 5** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 5** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 5**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
A[6]	33	I	**Port 2 line 6** MODE = 00_B: **XMU Address bus line 6** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 6** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 6**
A[7]	29	I	**Port 2 line 7** MODE = 00_B: **XMU Address bus line 7** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 7** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 7**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
A[8]	21	I	**Port 2 line 8** MODE = 00_B: **XMU Address bus line 8** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 8** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 8**
A[9]	20	I	**Port 2 line 9** MODE = 00_B: **XMU Address bus line 9** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 9** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 9**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
A[10]	19	I	**Port 2 line 10** MODE = 00_B: **XMU Address bus line 9** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 1** MODE = 10_B: **XMU Address bus line 10** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 9**
A[11]	18	I	**Port 2 line 11** MODE = 00_B: **XMU Address bus line 11** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 2 line 11** MODE = 10_B: **XMU Address bus line 11** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 2 line 11**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D8/ SR0	28	I/0	**Port 1 line 8** MODE = 00_B: **XMU** Data bus Line 8 MODE = 01_B**:** **Port 1 line 8** (Input/Output) MODE = 10_B: **XMU** Data Bus line 8 MODE = 11_B: **Port 1 line 8** (Input/Output) Alternative: **Interrupt Request Input/Output line 0** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
D9/ SR1	27	I/0	**Port 1 line 9** MODE = 00_B: **XMU** Data bus Line 9 MODE = 01_B**:** **Port 1 line 9** (Input/Output) MODE = 10_B: **XMU** Data Bus line 9 MODE = 11_B: **Port 1 line 9** (Input/Output) Alternative: **Interrupt Request Input/Output line 1** The logic 0 level at this pin indicates an interrupt request from/to the external host device.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D10/ SR2	23	I/0	**Port 1 line 10** MODE = 00_B: **XMU** Data bus Line 10 MODE = 01_B**:** **Port 1 line 10** (Input/Output) MODE = 10_B: **XMU** Data Bus line 10 MODE = 11_B: **Port 1 line 10** (Input/Output) Alternative: **Interrupt Request Input/Output line 2** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
D11/ SR3	22	I/0	**Port 1 line 11** MODE = 00_B: **XMU** Data bus Line 11 MODE = 01_B**:** **Port 1 line 11** (Input/Output) MODE = 10_B: **XMU** Data Bus line 11 MODE = 11_B: **Port 1 line 11** (Input/Output) Alternative: **Interrupt Request Input/Output line 3** The logic 0 level at this pin indicates an interrupt request from/to the external host device.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D12/ SR7	59	I/0	**Port 1 line 12** MODE = 00_B: **XMU** Data bus Line 12 MODE = 01_B**:** **12** (Input/Output) MODE = 10_B: **XMU** Data Bus line 12 MODE = 11_B: **Port 1 line 12** (Input/Output) Alternative: **Interrupt Request Input/Output line 7** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
D13/ SR6	58	I/0	**Port 1 line 13** MODE = 00_B: **XMU** Data bus Line 13 MODE = 01_B**:** **Port 1 line 13** (Input/Output) MODE = 10_B: **XMU** Data Bus line 13 MODE = 11_B: **Port 1 line 13** (Input/Output) Alternative: **Interrupt Request Input/Output line 6** The logic 0 level at this pin indicates an interrupt request from/to the external host device.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D14/ SR5	54	I/0	**Port 1 line 14** MODE = 00_B: **XMU** Data bus Line 14 MODE = 01_B**:** **Port 1 line 14** (Input/Output) MODE = 10_B: **XMU** Data Bus line 14 MODE = 11_B: **Port 1 line 14** (Input/Output) Alternative: **Interrupt Request Input/Output line 5** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
D15/ SR4	53	I/0	**Port 1 line 15** MODE = 00_B: **XMU** Data bus Line 15 MODE = 01_B**:** **Port 1 line 15** (Input/Output) MODE = 10_B: **XMU** Data Bus line 15 MODE = 11_B: **Port 1 line 15** (Input/Output) Alternative: **Interrupt Request Input/Output line 4** The logic 0 level at this pin indicates an interrupt request from/to the external host device.
$\overline{RD}$	34	I	**Port 2 line 15** MODE = 00_B: **XMU Read control line** Active during read operation MODE = 01_B: **Port 2 line 15** MODE = 10_B: **XMU Read control line** Active during read operation MODE = 11_B: **Port 2 line 15**

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
$\overline{WR}$	32	I	**Port 2 line 13** MODE = 00_B: **XMU Write control line** Active during write operation input line MODE = 01_B: **Port 2 line 13** MODE = 10_B: **XMU Write control line** Active during write operation input line MODE = 11_B: **Port 2 line 13**
$\overline{WAIT}$	30	I/O	**Port 0 line 13** MODE = 00_B: **XMU Wait output** MODE = 01_B: **Port 0 line 13** MODE = 10_B: **XMU Wait output** MODE = 11_B: **Port 0 line 13**
Control Signals			
$\overline{PORST}$	48	I	**Power-on Reset**
$\overline{JTAGEN}$	47	I	**JTAG Enabled Mode Selection/** Pin JTAGEN selects whether JTAG Enabled Mode is used to access the SAK-CIC310-OSMX2HT device. $\overline{JTAGEN}$ = 0_B: JTAG Enabled Mode $\overline{JTAGEN}$ = 1_B: Normal Mode

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
$\overline{\text{TRST}}$/ SR8/ A[12]	60	I/O	**Port 0 line 8** **Interrupt Request Input/Output Line 8** The logic 0 level at this pin indicates an interrupt request to/from the external host device. MODE = 00_B: **XMU Address bus line 12** The XMU Address Bus Lines serve as external address bus MODE = 01_B: **Port 0 line 8** or **Interrupt Request Input/Output Line 8** The logic 0 level at this pin indicates an interrupt request to/from the external host device. MODE = 10_B: **XMU Address bus line 12** The XMU Address Bus Lines serve as external address bus MODE = 11_B: **Port 0 line 8** or **Interrupt Request Input/Output Line 8** The logic 0 level at this pin indicates an interrupt request to/from the external host device. **Test Reset** (JTAG Enable Mode)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
MODE[0]/ SR9[1]	46[2]	I/O	**Port 0 line 12** **Interface Selection 0** Pin MODE 0 selects if the on-chip serial Host Communication Links (MLI or SSC) or the parallel XMU Host Communication Link is enabled for communicating to the SAK-CIC310-OSMX2HT device. MODE 0 = 0_B: On-chip XMU MODE 0 = 1_B: On-chip SSC or MLI After latching the initial state with the rising edge of the PORST signal (e.g. external pull-up or pull-down resistors), this MODE 0 pin can be used as: **Interrupt Request Input/Output Line 9** The logic 0 level at this pin indicates an interrupt request to/from the external host device.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
D7/ Mode[1][3)]	35	I/O	**Port 1 line 7** MODE = 00_B: **XMU Data Bus Line 7** MODE = 01_B: **Interface Selection 1** Pin MODE 1 selects if the on-chip serial MLI Communication Link or the serial SPI Host Communication Link is enabled for communicating to the SAK-CIC310-OSMX2HT device if Mode[0] = 1. MODE[0]= 1 AND MODE[1] = 0_B: On-chip MLI MODE[0]= 1 AND MODE[1]= 1_B: On-chip SSC After latching the initial state with the rising edge of the $\overline{\text{PORST}}$ signal (e.g. external pull-up or pull-down resistors), this MODE 1 pin can be used as standard IO pin. MODE = 10_B: **XMU Data Bus Line 7** Active during write operation input line MODE = 11_B: **Interface Selection 1** Pin MODE 1 selects if the on-chip serial MLI Communication Link or the serial SPI Host Communication Link is enabled for communicating to the SAK-CIC310-OSMX2HT device if Mode[0] = 1. MODE[0]= 1 AND MODE[1] = 0_B: On-chip MLI MODE[0]= 1 AND MODE[1]= 1_B: On-chip SSC After latching the initial state with the rising edge of the $\overline{\text{PORST}}$ signal (e.g. external pull-up or pull-down resistors), this MODE 1 pin can be used as standard IO pin.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
$\overline{\text{BYPASS}}$ CSFPI[4]	31	I	**Port 2 line 12** With the rising edge of the $\overline{\text{PORST}}$ the $\overline{\text{BYPASS}}$ signal is sampled: 0 The oscillator circuitry is bypassed and f_{osc} is directly derived from XTAL1 (OSCCON.OSCBY is set to 1). 1 In normal operating mode the oscillator is running and f_{osc} is derived from the crystal or from an external clock signal (OSCCON.OSCBY is set to 0). After latching the initial state with the rising edge of the $\overline{\text{PORST}}$ signal (e.g. external pull-up or pull-down resistors), this $\overline{\text{BYPASS}}$ pin can be used as standard Input pin as described following: MODE = 00_B: **XMU Chip Select** MODE = 01_B**:** **Port 2 Line 12** (Input) MODE = 10_B: **XMU** Chip Select MODE = 11_B: **Port 2 Line 12** (Input)
V_{DDP}	7, 26, 41, 55	+3.3 V	**Power Supply**, supply for IO pads
V_{SSP}[5]	8,25,4256	0V	**Ground**, for IO pads
V_{SSB}[5]	8,25,4256	0V	**Ground**, for Bulk Contact
V_{DDAPLL}[5]	10	+1.5 V	**Power Supply**, supply for analogue PLL circuitries
V_{SSAPLL}	9	0V	**Ground**, for analogue PLL circuitries
V_{DDOSC}[5]	10	+1.5 V	**Power Supply**, supply for oscillator
V_{SSOSC}[5]	11	0V	**Ground**, for oscillator
V_{SSPOSC}[5]	11	0V	**Ground**, for oscillator pad

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin	I/O	Function
	PG-TQFP-64		
V_{DDPOSC}	14	+3.3 V	**Power Supply**, supply for oscillator pad
V_{DD}	24, 57	+1.5 V	**Power Supply**, supply for digital module cores
V_{SS} 5)	25, 56	0V	**Digital Ground**, for digital module cores
XTAL1	12	I	**XTAL1** Input of the inverting oscillator amplifier and input to the internal clock generation circuit. When the SAK-CIC310-OSMX2HT device is provided with an external clock, XTAL1 should be driven while XTAL2 is left unconnected. Minimum and maximum high and low pulse width as well as rise/fall times specified in the AC characteristics must be respected.
XTAL2	13	O	**XTAL2** Output of the inverting oscillator amplifier.

1) The initial logic state on pins $\overline{\text{MODE}}$ is latched while the $\overline{\text{PORST}}$ input is active.
2) During Reset an internal pull-up device is connected.
3) The initial logic state on pins $\overline{\text{MODE}}$ is latched while the $\overline{\text{PORST}}$ input is active.
4) The initial logic state on pin $\overline{\text{BYPASS}}$ is latched while the $\overline{\text{PORST}}$ input is active.
5) Some power supplies are multiple bonded to a common pin.

In **Table 2** the signals and power lines going outside the standalone chip are summarized. These signals are partially routed via the pad logic to the pins. The analog signals go directly to the pins.

Figure 7 shows the pinning for a PG-TQFP-64 pin package.

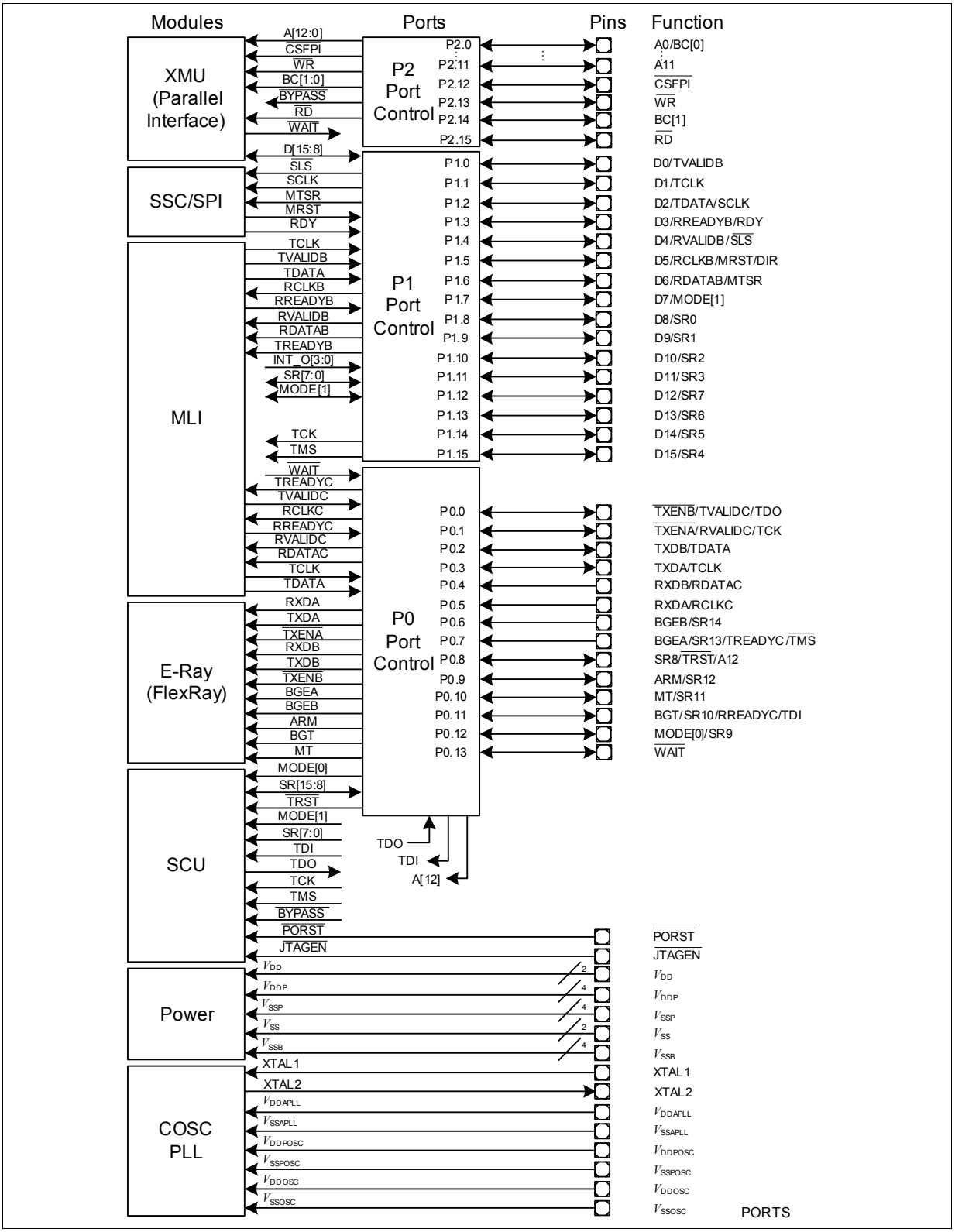

Figure 8 Pins for a PG-TQFP-64 Pin Package

3.2.3 Ordering Information

The ordering code for Infineon companion chip provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the SAK-CIC310-OSMX2HT please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 3** enumerates these derivatives and summarizes the differences.

Table 3 SAK-CIC310-OSMX2HT Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-CIC310-OSMX2HT	T_A = -40°C to +125°C

4 Electrical Parameters

The operating range for the SAK-CIC310-OSMX2HT is defined by its electrical parameters. For proper operation the indicated limitations must be respected when designing a system.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

4.1.1 Parameter Interpretation

The parameters listed on the following pages partly represent the characteristics of the SAK-CIC310-OSMX2HT and partly its demands on the system. To aid in interpreting the parameters easily, when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

Such parameters indicate **C**ontroller **C**haracteristics which are distinctive features of the SAK-CIC310-OSMX2HT and must be regarded for system design.

SR (**S**ystem **R**equirements):

Such parameter indicate **S**ystem **R**equirements which must be provided by the system in which the SAK-CIC310-OSMX2HT is designed in.

4.1.2 Pad Driver and Input Classes Definitions

Table 4 Pad Driver and Input Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage [1)]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A2**	40 MHz	50 pF	6 µA	Series termination recommended

1) Values are for T_{Jmax}=150°C

4.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN} > related V_{DD} or V_{IN} < V_{SS}) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 5 Absolute Maximum Ratings

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Ambient temperature	T_A	SR	-40	–	125	°C	Under Bias
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	Under Bias
Voltage at 1.5 V power supply pins with respect to V_{SS} [1]	V_{DD}	SR	–	–	2.25	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS} [2]	V_{DDP}	SR	–	–	3.75	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}		-0.5	–	V_{DDP} + 0.5 or max. 3.7	V	Whatever is lower
Crossbar Switch Frequency	f_{SYS}		–	–	80 [3]	MHz	–
E-Ray Sampling Frequency	f_{SAMPLE}		–	–	80 [3]	MHz	–

1) Applicable for V_{DD}, V_{DDOSC}, and V_{DDAPLL}.
2) Applicable for V_{DDP}.
3) The PLL jitter characteristics add to this value according to the application to the application settings. See PLL jitter parameters.

4.1.4 Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the SAK-CIC310-OSMX2HT. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 6 Operating Conditions

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Digital supply voltage[1]	V_{DD}	SR	1.42	–	1.58[2]	V	–
	V_{DDAPLL}	SR	1.42	–	1.58[2]	V	–
	V_{DDPOSC}	SR	3.13	–	3.47[3]	V	–
	V_{DDP}	SR	3.13	–	3.47[3]	V	For Class A pins (3.3V±5%)
Digital ground voltage	V_{SS}	SR	0	–	–	V	–
Ambient temperature under bias	T_A	SR	-40	–	+125	°C	–
Crossbar Frequency	f_{SYS}	SR	–[4]	–	80	MHz	–
Short circuit current	I_{SC}	SR	-5	–	+5	mA	[5]
Absolute sum of short circuit currents of a pin group[6]	$\Sigma\|I_{IN}\|$	SR	–	–	20	mA	See Note[7]
Inactive device pin current (V_{DD} = 0)	I_{ID}	SR	-1		1	mA	–
Absolute sum of short circuit currents of a the device	$\Sigma\|I_{SC}\|$	SR	–	–	50	mA	See Note[7]

1) Digital supply voltages applied to the SAK-CIC310-OSMX2HT must be static regulated voltages which allow a typical voltage swing of ±5%.

2) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ pin low, provided the pulse duration is less than 100µs and the accumulated summary of these pulses does not exceed 1 hour.

3) Voltage overshoot up to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ pin low, provided the pulse duration is less than 100µs and the accumulated summary of these pulses does not exceed 1 hour.

4) The SAK-CIC310-OSMX2HT uses a static design, so the minimum operation frequency is 0 MHz. Due to test time restriction no lower frequency boundary is tested, however.

5) The absolute sum of all currents (output current, overload current, short circuit current) on all digital IO pins of a port must not exceed 20 mA. The supply voltage must remain within the specified limits.

6) pin group 0: P0.0; P0.1; P0.4; P0.5; P0.2; P0.3; P0.6; P0.10
pin group 1: P0.9; P2.11; P2.10; P2.9; P2.8; P1.11; P1.10
pin group 2: P1.9; P1.8; P2.7; P0.13; P2.12; P2.13
pin group 3: P2.6; P2.15; P1.7; P1.6; P1.5; P1.4; P1.3; P1.2
pin group 4: P1.1; P1.0; P2.14; P0.12; $\overline{\text{JTAGEN}}$; $\overline{\text{PORST}}$
pin group 5: P2.5; P2.4; P2.3; P2.2; P1.15; P1.14
pin group 6: P1.13; P1.12; P0.8; P2.1; P2.0; P0.7; P0.11

7) See additional document “TC1796 Pin Reliability in Overload” for overload current definitions.

4.2 DC Parameters

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

The leakage currents strongly depend on the operating temperature and the actual voltage level at the respective pin. The maximum values given in the following tables apply under worst case conditions.
The actual value for the leakage current can be determined by evaluating the respective leakage derating formula using values from the actual application.

The pads of the SAK-CIC310-OSMX2HT are designed to operate in various driver modes. The DC parameter specifications refer to the current limits given in **Table 7**.

4.2.1 Input/Output Characteristics

These parameters apply to the lower IO voltage area of 3.13 V ≤ V_{DDP} ≤ 3,47 V.

Table 7 Input/Output DC-Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
General Parameters							
Pull-up current[1)]	$\|I_{PUH}\|$	CC	10	–	100	µA	$V_{IN} < V_{IHAmin}$
Pull-down current[1)]	$\|I_{PDL}\|$	CC	10	–	150	µA	$V_{IN} > V_{ILAmax}$
Pin capacitance[1)] (Digital I/O)	C_{IO}	CC	–	–	10	pF	f = 1 MHz T_A = 25 °C
Input only Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)							
Input low voltage class A2 pins (all except XTAL1, XTAL2)	V_{ILA}	SR	-0.3	–	0.34 × V_{DDP}	V	–
Input high voltage class A2 pins (all except XTAL1, XTAL2)	V_{IHA2}	SR	0.64 × V_{DDP}	–	V_{DDP} + 0.3 or max. 3.6	V	Whatever is lower
V_{IL}Ratio /V_{IH}[1)]		CC	0.53	–	–	–	–
Input hysteresis[2)]	HYSA	CC	0.1 × V_{DDP}	–	–	V	

Table 7 Input/Output DC-Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
General Parameters							
Input leakage current	I_{OZI}	CC	–	–	±3000 ±6000	nA	$V_{DDP}((/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3]
Class A Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ±5%)							
Output low voltage[4]	V_{OLA}	CC	–	–	0.4	V	I_{OL} = 2 mA for strong driver mode,
Output high voltage[3]	V_{OHA}	CC	2.4	–	–	V	I_{OH} = 2 mA for strong driver mode,
		CC	V_{DDP} - 0.4		–	V	I_{OH} = 1.4 mA for strong driver mode,
Input low voltage class A2 pins	V_{ILA}	SR	-0.3		0.34 × V_{DDP}	V	–
Input high voltage class A2 pins	V_{IHA}	SR	0.64 × V_{DDP}	–	V_{DDP} + 0.3 or max 3.6V	V	Whatever is lower
Ratio V_{IL}/V_{IH}[1]		CC	0.53	–	–		–
Input hysteresis[1]	HYSA	CC	0.1 × V_{DDP}	–	–	mV	[5]
Input leakage current Class A2 pins	I_{OZA24}	CC	–	–	±3000 ±6000	nA	$((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ otherwise[3]

1) Not subject to production test, verified by design/characterization.

2) Not subject to production test, verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

3) Only one of these parameters is tested, the other is verified by design / characterization

4) Max. resistance between pin and next power supply pin 25 Ω for strong driver mode, (verified by design / characterization)

5) Function verified by design, value verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot guaranteed that it suppresses switching due to external system noise.

4.2.2 External Clock Drive

These parameters define the external clock supply for the SAK-CIC310-OSMX2HT. The clock signal can be supplied either to pin XTAL1.

Table 8 Oscillator Pins Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Frequency Range	f_{OSC}	CC	20	–	40	MHz	–
Input low voltage at XTAL1[1)]	V_{ILX}	SR	-0.2	–	0.3 × V_{DDPOSC}	V	–
Input high voltage at XTAL1[1)]	V_{IHX}	SR	0.7 × V_{DDPOSC}	–	V_{DDPOS} + 0.2	V	–
Input current at XTAL1	I_{IX1}	CC	–	–	±25	µA	0 V < V_{IN} < V_{DDPOSC} 2)

1) If the XTAL1 pin is driven by a crystal, reaching an amplitude (peak-to-peak) of 0.3 × V_{DDPOSC} is sufficient.

2) Not subject to production test, verified by design / characterization.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.

4.2.3 Power Supply Current

Table 9 Power Supply Currents (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note Conditions
			Min.	Typ.	Max.		
$\overline{\text{PORST}}$ low current at V_{DD}	I_{DD_PORST}	CC	–	–	20	mA	The PLL running at the base frequency
$\overline{\text{PORST}}$ low current at V_{DDP}, and $\overline{\text{PORST}}$ high current without any port activity	I_{DDP_PORST}	CC	–	–	4.5	mA	The PLL running at the base frequency, Mode[0]=0 and Mode[1]=1
Active mode core supply current[1)2)]	I_{DD}	CC	25	–	80	mA	f_{SAMPLE}=80 MHz f_{sample}/f_{SYS} = 1:1
			25	–	50	mA	f_{SAMPLE}=80 MHz f_{sample}/f_{SYS} = 2:1
Oscillator and PLL core power supply	I_{DDAPLL}	CC	–	–	4	mA	–
Oscillator and PLL pads power supply	I_{DDPOSC}	CC	–	–	3.5	mA	–
Maximum Allowed Power Dissipation[3)]	P_D	SR	–	–	$P_D \times R_{\theta JA}$ < 25°C	–	Worst case T_A = 125°C

1) Infineon Power Loop: all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

2) The I_{DD} decreases for typically 20mA if the f_{SAMPLE} is decreased for 60 MHz, at constant T_J = 150°C, for the Infineon Max Power Loop.
The dependency in this range is, at constant junction temperature, linear.

3) For the calculation of junction to ambient thermal resistance R_{TJA}, see the chapter **"Package and Reliability" on Page 66**.

Note: The power supply currents are not subject to production test. They are verified by design / characterization.

4.3 AC Characteristic Targets

These parameters describe the dynamic behavior of the SAK-CIC310-OSMX2HT.

4.3.1 Testing Waveforms

These references are used for characterization and production testing (except for pin XTAL1).

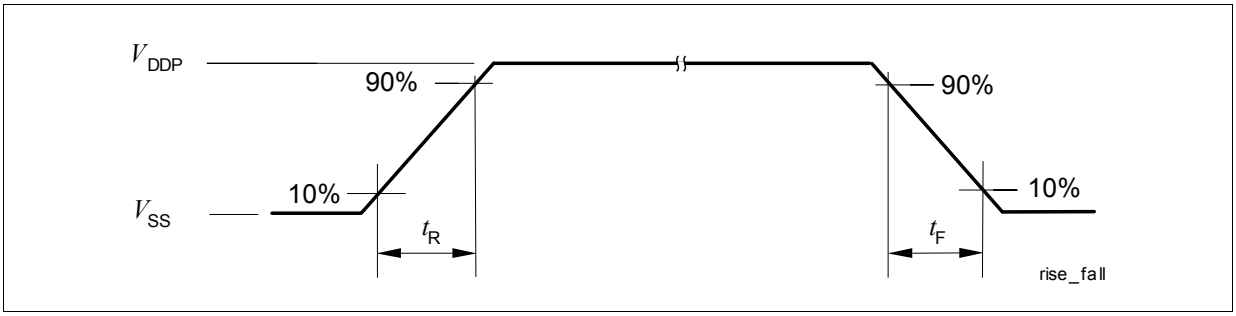

Figure 9 Test Levels for Output Rise / Fall Times

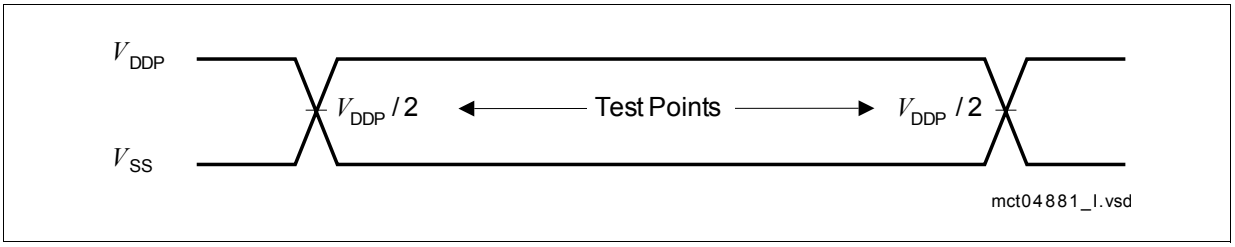

Figure 10 Test Levels for Output Delay

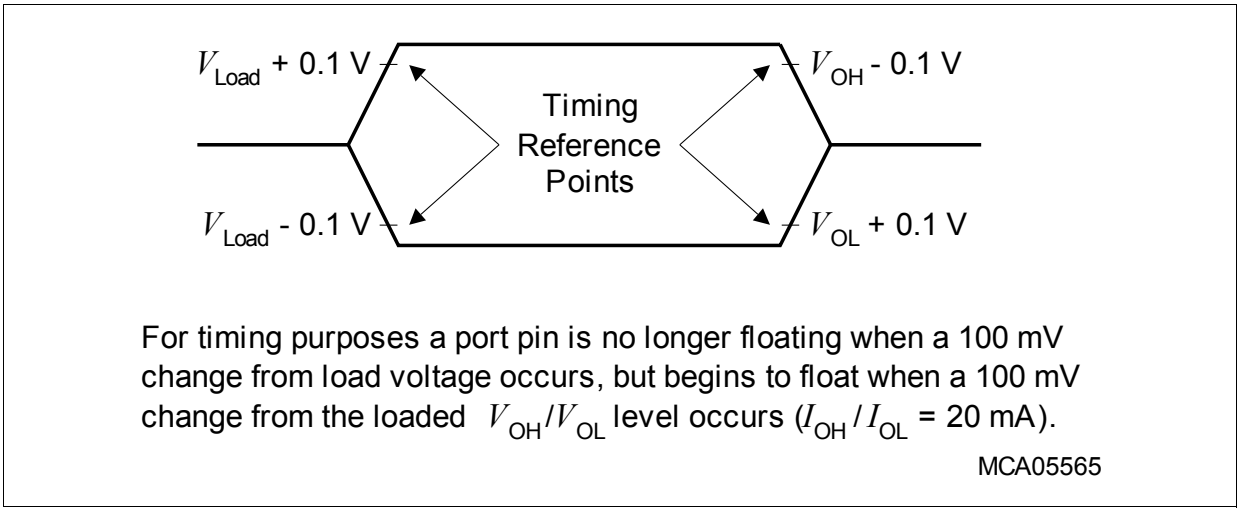

Figure 11 Test Levels for Output Floating / Driving

4.3.2 Output Rise/Fall Times

Table 10 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Class A2 Pads							
Rise/fall times	t_{RA2}, t_{FA2}	CC	–	–	3.7 7.5 7.0 18 50 140 18000	ns	strong driver, sharp edge, 50 pF strong driver, sharp edge, 100 pF strong driver, med. edge,50 pF strong driver, soft edge, 50 pF medium driver, 50 pF medium driver, 150 pF medium driver, 20 000 pF 1)
Rise/fall time matching		CC	125	–	160	%	

1) Not subject to production test, verified by design / characterization.

4.3.3 Power Sequencing

There is a restriction for the power sequencing of V_{DD} and V_{DDP} as shown in **Figure 12**: V_{DDP} must always be greater than V_{DD} - 0.5 V. The gray area shows the valid range for V_{DDP}.

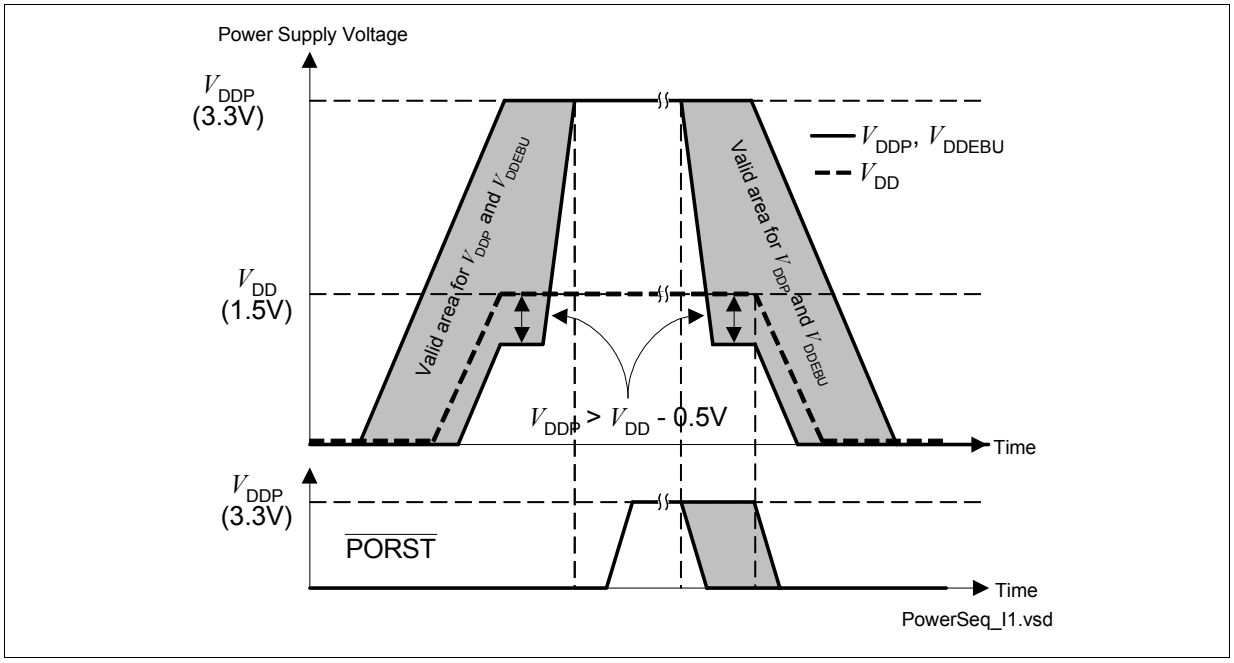

Figure 12 V_{DDP} / V_{DD} Power Sequencing

All ground pins V_{SS}, V_{SSP}, V_{SSPLL}, and V_{SSOSC} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 200 mV.

All power pins V_{DD} and V_{DDAPLL} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 100 mV.

All power pins V_{DDP} and V_{DDPOSC} must be externally connected to one single star point in the system. The difference voltage between the ground pins must not exceed 100 mV.

The $\overline{\text{PORST}}$ signal must be activated at latest before any power supply voltage falls below the levels shown on the figure below. Additionally the $\overline{\text{PORST}}$ signal should be activated as soon as possible. The sooner the $\overline{\text{PORST}}$ signal is activated, the less time the system operates outside of the normal operating power supply range.

4.3.4 Power, Pad and Reset Timing

These parameters are not subject to production test. They are verified by design/characterization.

Table 11 Power Up/Down Parameters

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Min. V_{DDP} voltage to ensure defined pad states[1]	V_{DDPPA}	CC	0.6	–	–	V	–
Minimum V_{DD} $\overline{\text{PORST}}$ activation threshold	$V_{PORST1.5}$	SR	1.32	–	–	V	–
Minimum V_{DDP} $\overline{\text{PORST}}$ activation threshold	$V_{PORST3.3}$	SR	2.9	–	–	V	–
Oscillator start-up time[2]	t_{OSCS}	CC	–	–	10	ms	–
Minimum $\overline{\text{PORST}}$ active time after power supplies are stable at operating levels	t_{POA}	CC	10	–	–	ms	–
$\overline{\text{PORST}}$ rise time	t_{POR}	SR	–	–	50	ms	–
Setup time to $\overline{\text{PORST}}$ rising edge[3]	t_{POS}	SR	0	–	–	ns	–
Hold time from $\overline{\text{PORST}}$ rising edge[3]	t_{POH}	SR	100	–	–	ns	–
Ports inactive after any reset active[4]	t_{PIP}	CC	–	–	150	ns	–

1) This parameter is valid under assumption that $\overline{\text{PORST}}$ signal is constantly at low-level during the power-up/power-down of the V_{DDP}.

2) t_{OSCS} is defined from the moment when V_{DDPOSC} = 3.13 V until the oscillations reach an amplitude at XTAL1 of 0,3*V_{DDPOSC}. This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.

3) Applicable for input pins $\overline{\text{JTAGEN}}$, MODE0 and MODE1 with noise suppression filter of $\overline{\text{PORST}}$ switched-on.

4) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

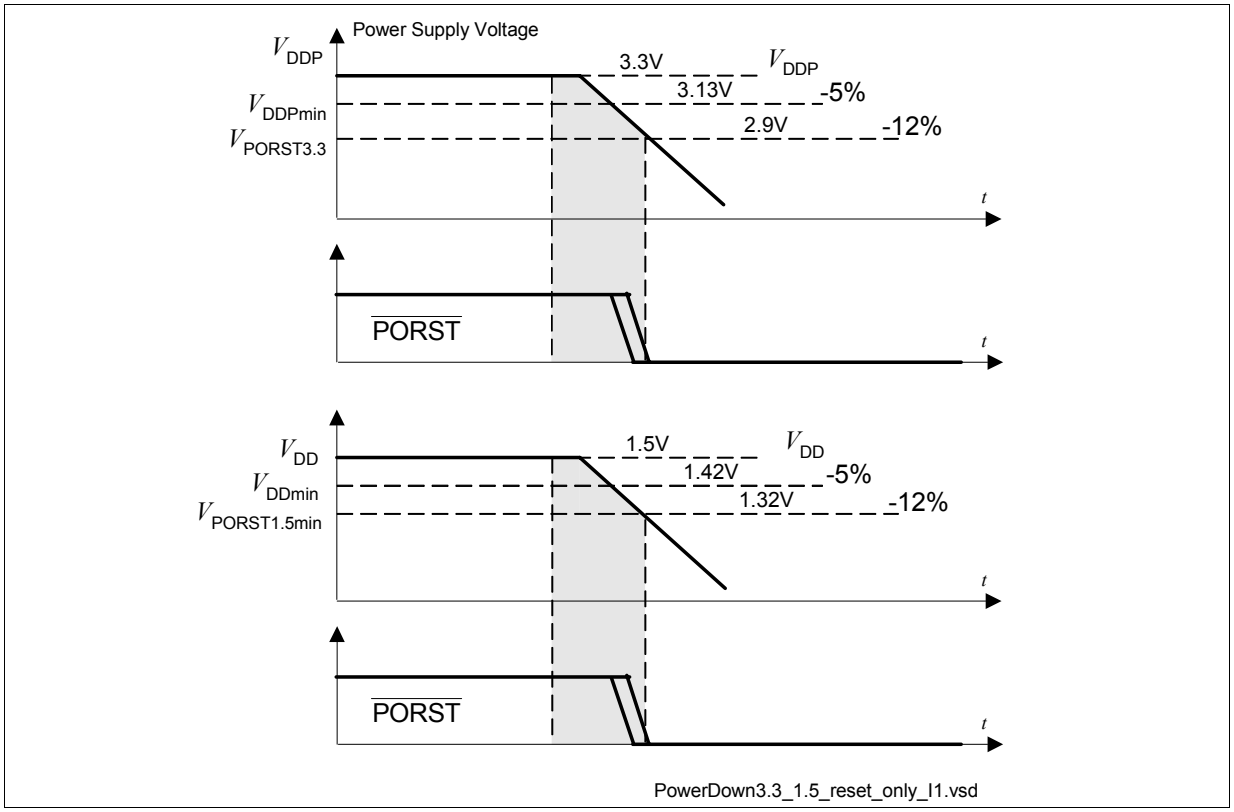

Figure 13 Power Down/Power Loss Sequences

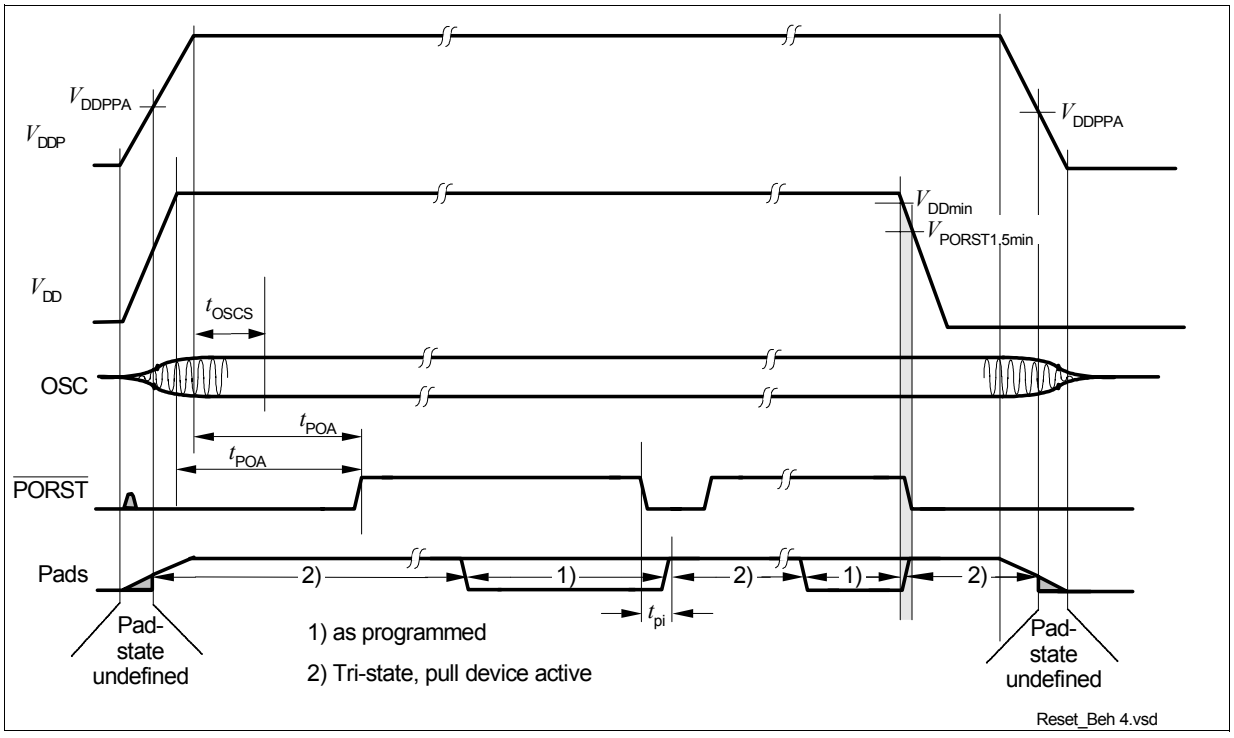

Figure 14 Power, Pad and Reset Timing

4.3.5 Input Clock Timing

Table 12 Input Clock Timing (Operating Conditions apply)

Parameter		Symbol		Limit Values			Unit	Notes
				Min.	Typ.	Max.		
Oscillator clock frequency	bypass PLL	f_{OSC}	SR	20	–	40	MHz	–
	with PLL	f_{OSC}	SR	20	–	40	MHz	–
Input clock frequency driving at XTAL1	bypass PLL	f_{OSCDD}	SR	–	–	80	MHz	–
	with PLL	f_{OSCDD}	SR	20	–	40	MHz	–
Input Clock high time		t_1	SR	$0.4 \times T_{OSCDD}$	–	–	ns	1)2)3)
Input Clock low time		t_2	SR	$0.4 \times T_{OSCDD}$	–	–	ns	1)2)3)
Input Clock rise time		t_3	SR	–	–	8	ns	1)2)3)
Input Clock fall time		t_4	SR	–	–	8	ns	1)2)3)

1) The clock input signal must reach the defined levels V_{ILX} and V_{IHX}.
2) Not subject to production test, verified by design / characterization.
3) Applies to oscillator bypass mode.

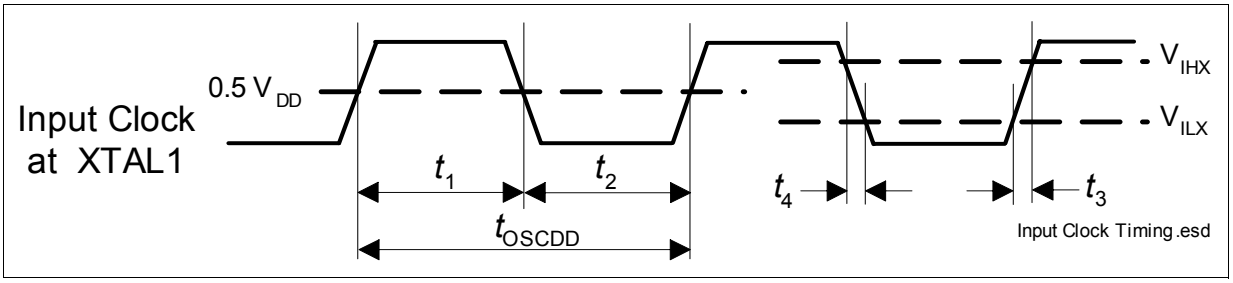

Figure 15 Input Clock Timing

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 20 MHz or 40 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

4.3.6 Phase Locked Loop (PLL)

Note: All PLL characteristics defined on this and the next page are verified by design characterization.

Table 13 PLL Parameters (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Accumulated jitter	D_P	CC	See **Figure 16**	–	–	–	–
VCO frequency range	f_{VCO}	CC	400	–	500	MHz	–
PLL base frequency[1)]	$f_{PLLBASE}$	CC	140	–	320	MHz	–
PLL lock-in time	t_L	CC	–	–	200	µs	–

1) The system base frequency which is selected after reset is calculated by dividing the limit values by 16 (this is the K factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the clock f_{SYS}) is constantly adjusted to the selected frequency. The relation between f_{VCO} and f_{SYS} is defined by: $f_{VCO} = K \times f_{SYS}$. The PLL causes a jitter of f_{SYS}.

Figure 16 gives the jitter curve.

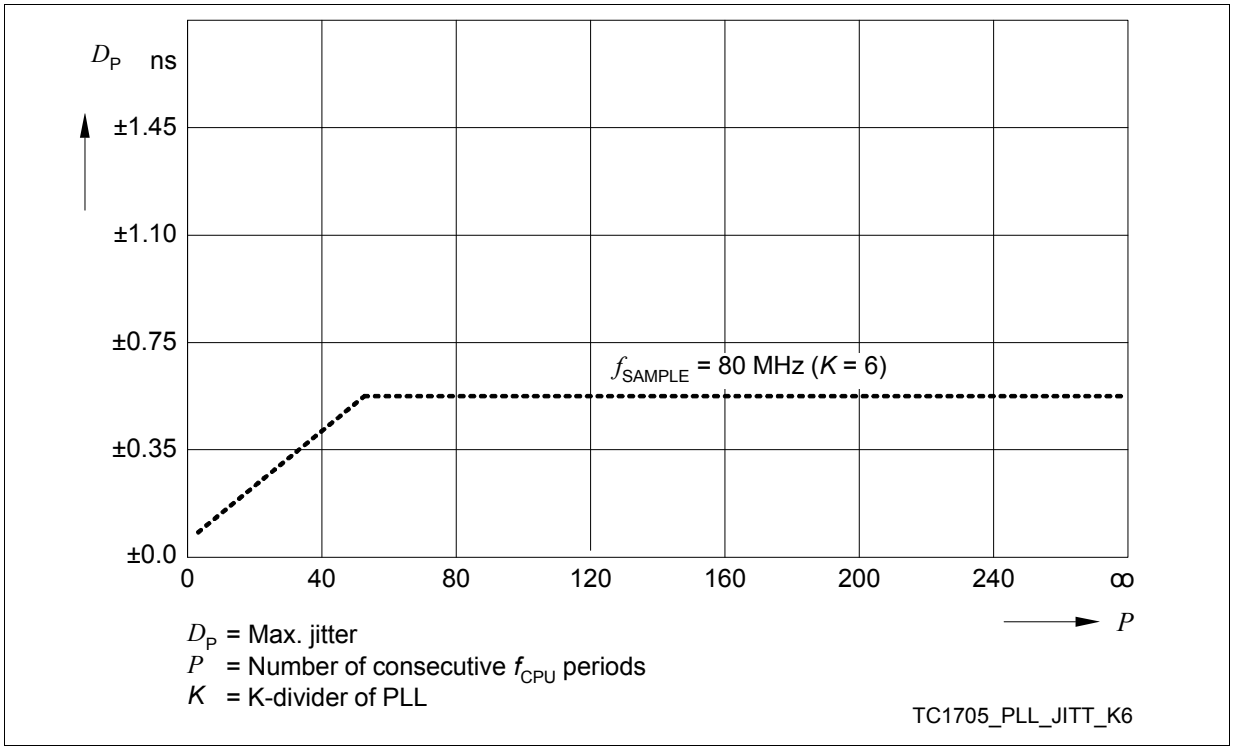

Figure 16 Approximated Maximum Accumulated PLL Jitter for Typical Clock Frequencies f_{SAMPLE} (overview)

Note: The specified PLL jitter values are valid if the capacitive load at the External Bus Unit (XMU) is limited to C_L=20 pF.

Note: The maximum peak-to-peak noise on the supply voltage pin V_{DDAPLL} is limited to a peak-to-peak voltage of V_{PP} = 10mV and frequency less than 200 KHz. This condition can be achieved by appropriate blocking of the Core Supply Voltage as near as possible to the supply pins and using PCB supply and ground planes.

4.3.7 Synchronous Serial Channel (SSC) Slave Mode Timing

The following parameters define the behavior of the SAK-CIC310-OSMX2HT's synchronous serial communication interface.

Table 14 SSC Timing (Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
Slave Mode Timing							
SCLK clock period	t_{20}	SR	50	–	–	ns	
SCLK high period	t_{30}	SR	20%	–	70%	t_{20}	
SCLK low period	t_{31}	SR	20%	–	70%	t_{20}	
MRST delay from SCLK rising edge (CON.PO, CON.PH = 00) SCLK falling edge (CON.PO,CON.PH = 10)	t_{21}	CC	3	–	12	ns	
MRST hold from SLSI1 rising edge	t_{26}	CC	–	–	14	ns	1)
MTSR setup to SCLK rising edge (CON.PO,CON.PH = 00) SCLK falling edge (CON.PO,CON.PH = 10)	t_{22}	SR	16	–	–	ns	
MTSR hold from SCLK rising edge (CON.PO,CON.PH = 00) SCLK falling edge (CON.PO,CON.PH = 10)	t_{23}	SR	13	–	–	ns	
SLSI lead delay to SCLK rising edge (CON.PO,CON.PH = 00) SCLK falling edge (CON.PO,CON.PH = 10)	t_{24}	SR	12[2)]	–	–	ns	
RDY lead delay to SLSI falling edge	t_{25}	CC	100	–	130	ns	
SLSI hold from RDY rising edge	t_{27}	SR	8	–	–	ns	
DIR lead delay to SCLK rising edge (CON.PO,CON.PH = 00) SCLK falling edge (CON.PO,CON.PH = 10)	t_{28}	SR	4	–	–	ns	
DIR hold from SCLK falling edge (CON.PO,CON.PH = 00) SCLK rising edge (CON.PO,CON.PH = 10)	t_{29}	SR	12	–	14	ns	1)
SLSI falling edge delay to SLSI rising edge	t_{20}	SR	50	–	–	ns	

1) Not subject to production test, verified by design / characterization.

2) This is only valid if SSC move engine is idle (RDY = 1).

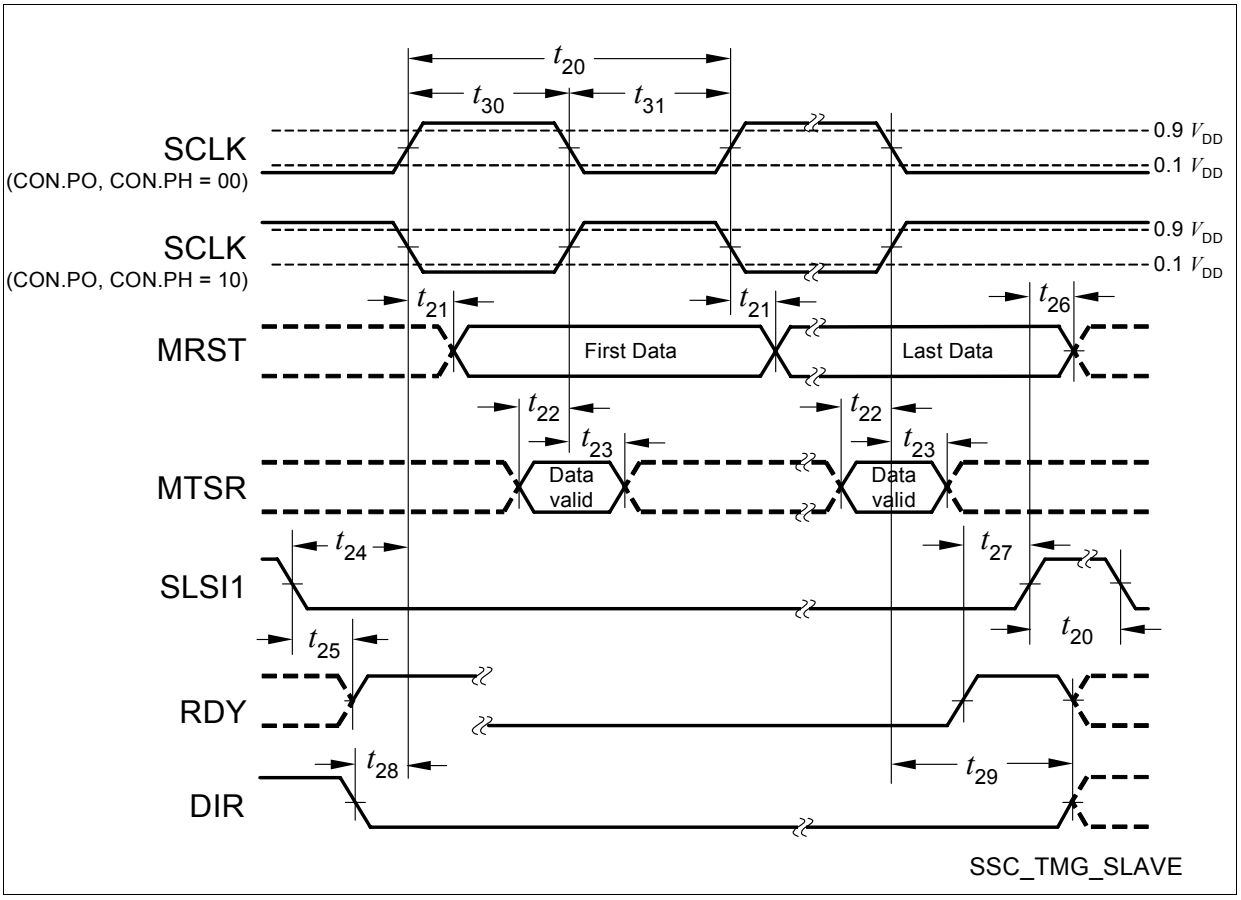

Figure 17 SSC Slave Mode Timing

4.3.8 MLI Interface Timing

The following parameters define the behavior of the SAK-CIC310-OSMX2HT's microlink interface.

Table 15 MLI Interface Timing (Operating Conditions apply); C_L = 50 pF

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
TCLK clock period[1]	t_{40}	CC/SR	$2 \times T_{MLI}$[2]	–	–	ns	–
TCLK high period	t_{41}	CC	20%	–	70%	t_{40}	–
TCLK low period	t_{42}	CC	20%	–	70%	t_{40}	–
RCLK high period	t_{41}	SR	20%	–	70%	t_{47}	–
RCLK low period	t_{42}	SR	27%	–	70%	t_{47}	–
TCLK rise time[3]	t_{43}	CC	–	–	25%	t_{40}	4)
TCLK fall time[1]	t_{44}	CC	–	–	25%	t_{40}	4)
RCLK rise time	t_{43}	SR	–	–	25%	t_{47}	4)
RCLK fall time	t_{44}	SR	–	–	25%	t_{47}	4)
TDATA and TVALID valid after TCLK rising edge	t_{45}	CC	-10%	–	35%	t_{40}	–
TREADY setup to TCLK rising edge	t_{46}	SR	35%	–	–	t_{40}	–
RVALID and RDATA setup to RCLK falling edge	t_{46}	SR	25%	–	–	t_{47}	–
RCLK clock period (typically 50% duty cycle)	t_{47}	SR	$2 \times T_{SYS}$ = 25	–	–	ns	–
RVALID and RDATA hold from RCLK falling edge	t_{48}	SR	45%	–	–	t_{47}	–
RREADY valid after RCLK falling edge	t_{49}	CC	-10%	–	50%	t_{47}	–

1) TCLK high and low times can be minimum $1 \times T_{MLI.}$

2) $T_{MLImin} = 2 \times T_{SYS} = 2 \times 1/f_{SYS}$. When f_{SYS} = 80 MHz, t_{40} = 25 ns

3) Fastest driver strength selected.

4) Not subject to production test, verified by design / characterization.

Note: The handshake timing does not include any protocol delay times (number of TCLK or RCLK clock periods), but only the respective hardware sampling time and setup time windows.

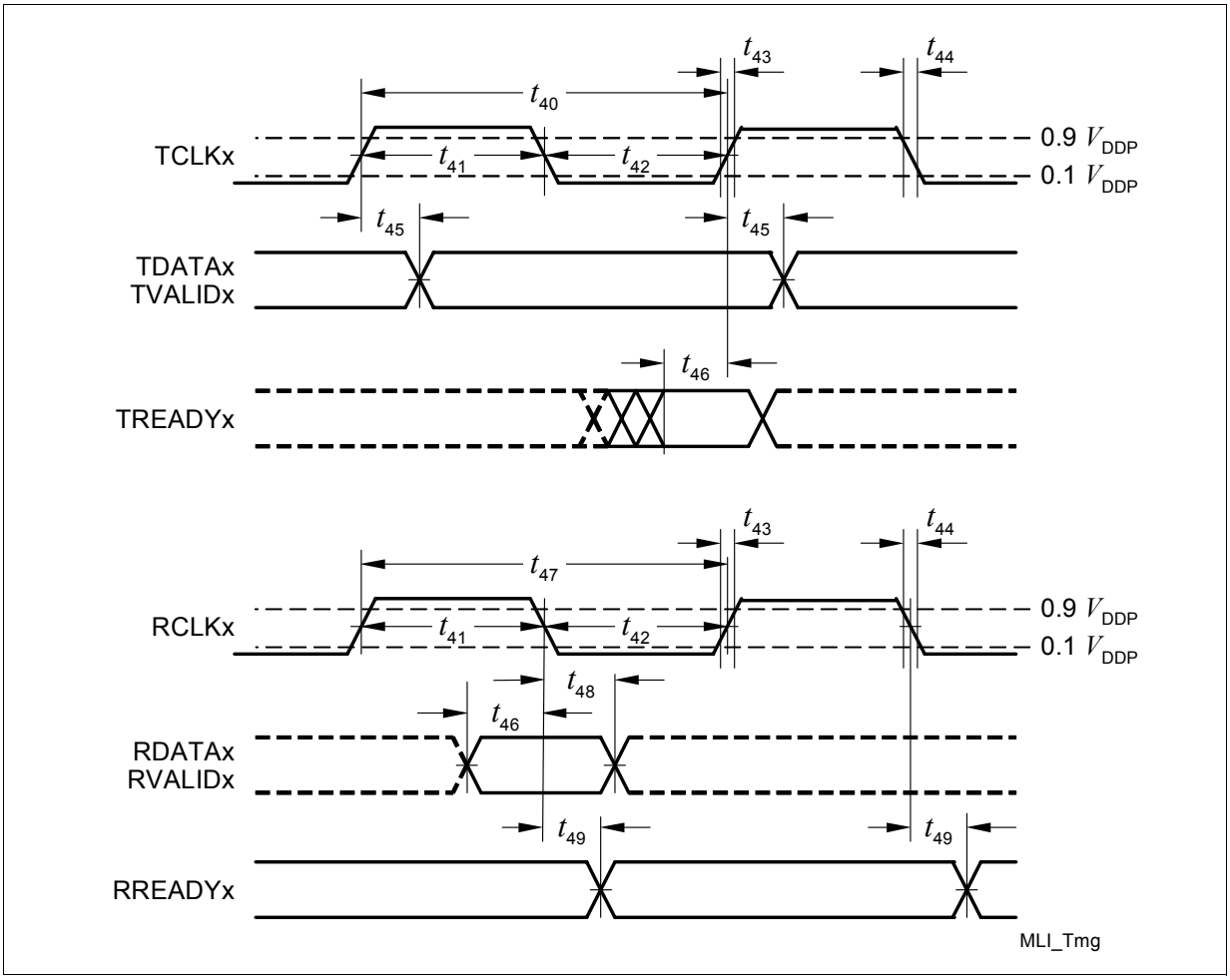

Figure 18 MLI Interface Timing

4.3.9 XMU External Access Timing

The following parameters define the behavior of the SAK-CIC310-OSMX2HT's external parallel memory interface.

Table 16 XMU External Access Timing (Operating Conditions apply), C_L = 20 pF

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
$\overline{RD}$ delay from $\overline{CSFPI}$ falling edge	t_{51}	SR	3	–	–	ns	
$\overline{WR}$ delay from $\overline{CSFPI}$ falling edge	t_{51}	SR	3	–	–	ns	
Address setup to $\overline{RD}$ falling edge	t_{52}	SR	3	–	–	ns	
Address hold from $\overline{RD}$ falling edge	t_{53}	SR	10	–	–	ns	
$\overline{WAIT}$ active after $\overline{RD}$ falling edge	t_{54}	CC	–	–	20	ns	
$\overline{WAIT}$ active after $\overline{WR}$ falling edge	t_{54}	CC	–	–	20	ns	
$\overline{WAIT}$ rising edge after $\overline{RD}$ falling edge	t_{55}	CC	11 × t_{SYS}	–	–	ns	
Data setup to $\overline{RD}$ falling edge	t_{55}	CC	12 × t_{SYS}	–	–	ns	
$\overline{WAIT}$ valid after $\overline{RD}$ rising edge	t_{56}	CC	–	–	20	ns	1)
$\overline{WAIT}$ valid after $\overline{WR}$ rising edge	t_{56}	CC	–	–	20	ns	1)
Data valid after $\overline{WR}$ rising edge	t_{56}	CC	–	–	20	ns	1)
$\overline{WAIT}$ float after $\overline{CSFPI}$ rising edge	t_{57}	CC	–	–	12	ns	1)
Data float after $\overline{CSFPI}$ rising edge	t_{57}	CC	–	–	12	ns	1)
$\overline{WR}$ rising edge delay from $\overline{WAIT}$ rising edge	t_{58}	SR	3	–	–	ns	
Data, Address, and Byte Control hold from $\overline{WR}$ rising edge	t_{59}	SR	3	–	–	ns	

1) Not subject to production test, verified by design / characterization.

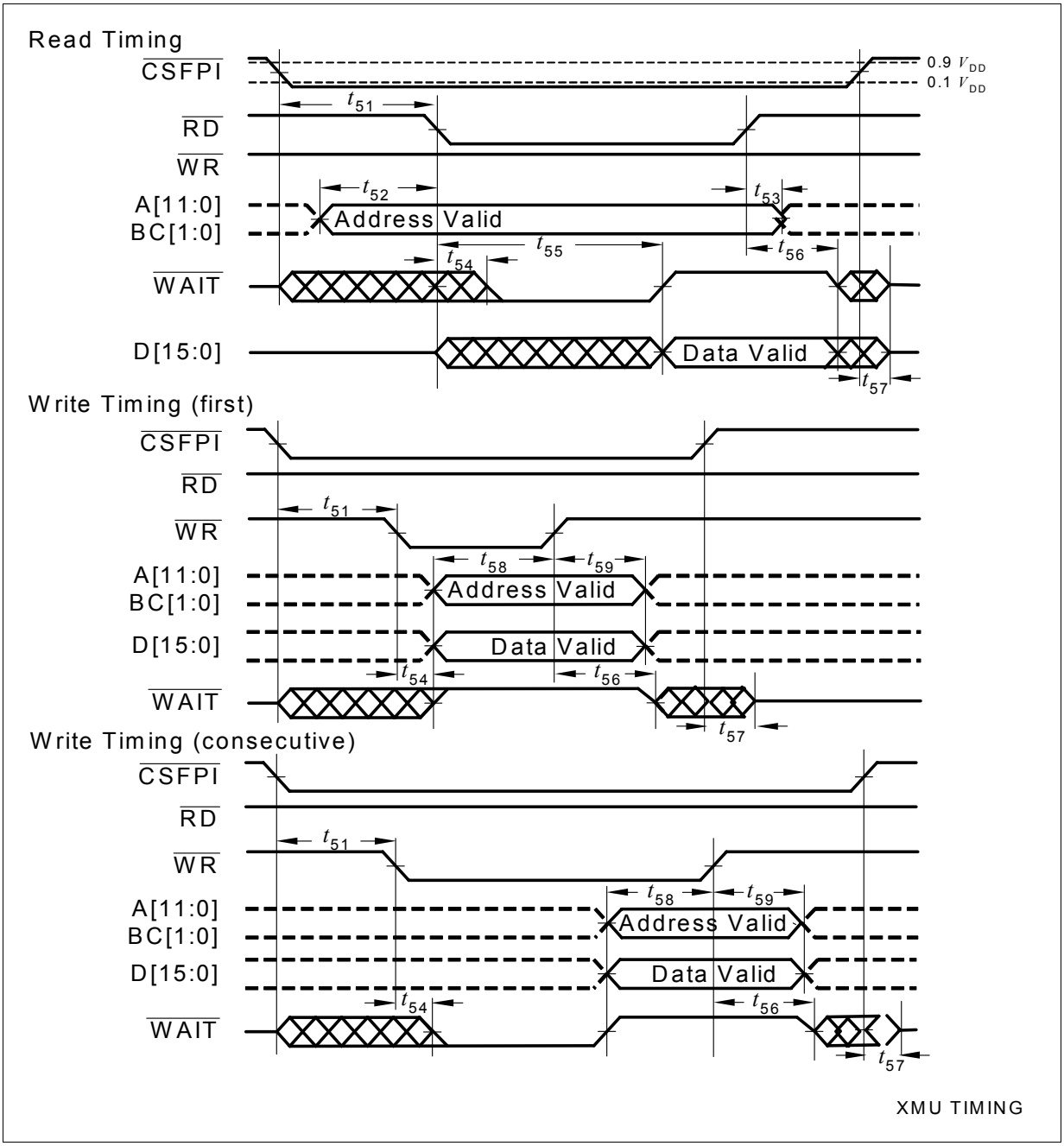

Figure 19 XMU External Access Timing

4.3.10 ERAY Interface Timing

Table 17 ERAY Interface Timing (Operating Conditions apply), C_L = 35 pF

Parameter	Symbol		Limit Values			Unit	Notes Conditions
			Min.	Typ.	Max.		
TxDA/TxDB Signal Timing at end of frame							
Time span from last BSS to FES without the influence of external quartz circuitry tolerances (d10Bit_TX))	t_{60}	CC	997.75	–	1002.25	ns	f_{OSCDD} = 20 MHz or 40 MHz; C_L = 35 pF; PRT.BRP = 0; P0_PDR.PD0 = 000_B (TxDA, TxDB) External noise on V_{DDAPLL}: Amplitude ≤ 10 mV Frequency ≤ 200 kHz
TxD data valid from f_{sample} flip-flop txd_reg ⇒ TxDA, TxDB) (dTxAsym)[1)]	$\|t_{61} - t_{62}\|$	CC	–	–	1.5	ns	Asymmetrical Delay of rising and falling edge (TxDA, TxDB) P0_PDR.PD0 = 000_B
RxDA/RxDB Signal Timing at end of frame							
Time span between last BSS and FES that can to be properly decoded without influence of external quartz circuitry tolerances (d10Bit_RX)	t_{63}	SR	966.25	–	1045.97	ns	f_{OSCDD} = 20 MHz or 40 MHz; C_L = 35 pF PRT.BRP = 0; PRT.SPP = 0 (RxDA, RxDB) External noise on V_{DDAPLL}: Amplitude ≤ 10 mV Frequency ≤ 200 kHz
RxD capture by f_{sample} (RxDA/RxDB ⇒ sampling flip-flop) (dRxAsym)[1)]	$\|t_{64} - t_{65}\|$	CC	–	–	3.5	ns	Asymmetrical Delay of rising and falling edge (RxDA, RxDB)

1) Not subject to production test, verified by design/characterization.

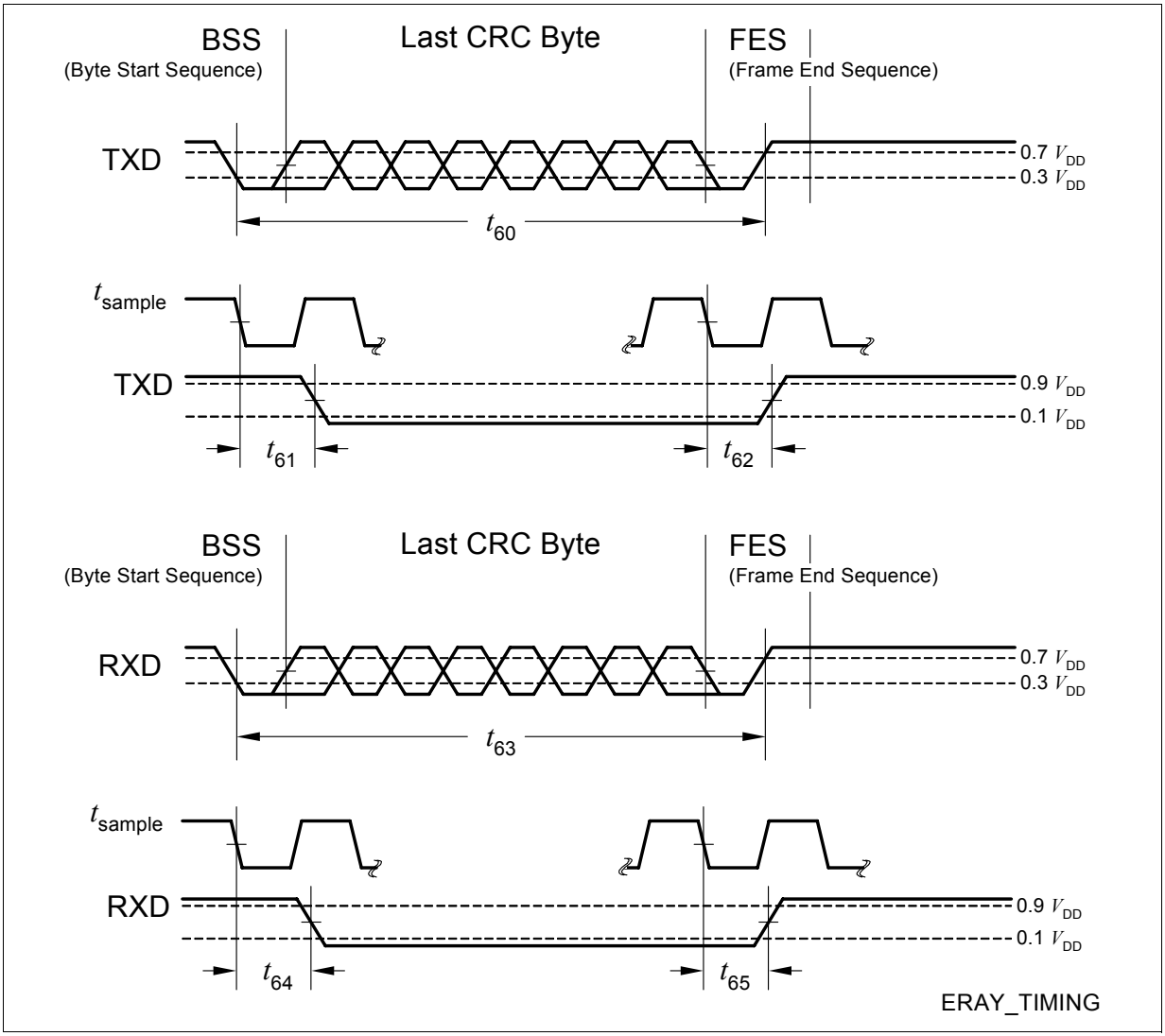

Figure 20 ERAY Timing

4.4 Package and Reliability

4.4.1 Package Parameters (PG-TQFP-64)

Table 18 Thermal Characteristics of the Package

Parameter	Symbol		Values			Unit	Note Conditions
			Min.	Typ.	Max.		
Thermal resistance junction case top[1)]	$R_{\theta JCTop}$	CC	–		17.1	K/W	–
Thermal resistance junction leads[1)]	$R_{\theta JLeads}$	CC	–		39	K/W	–

1) The thermal resistances from the case top and the lead to the ambient ($R_{\Theta CTA}$, $R_{\Theta LA}$) are to be combined with the thermal resistances between the junction and the case/leads given above ($R_{\Theta JCTop}$, $R_{\Theta JLeads}$), in order to calculate the total thermal resistance between the junction and the ambient ($R_{\Theta JA}$).
The thermal resistances between the case/leads and the ambient ($R_{\Theta CTA}$, $R_{\Theta LA}$) as well as the method of combination/calculation depend on the external system (PCB, case) characteristics, and are under user responsibility. The junction temperature can be calculated using the following equation: $T_J = T_A + R_{\Theta JA} \times P_D$, where the $R_{\Theta JA}$ is the total thermal resistance between the junction and the ambient. This total junction ambient resistance $R_{\Theta JA}$ can be obtained from the upper four partial thermal resistances.

4.4.2 Package Outline

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

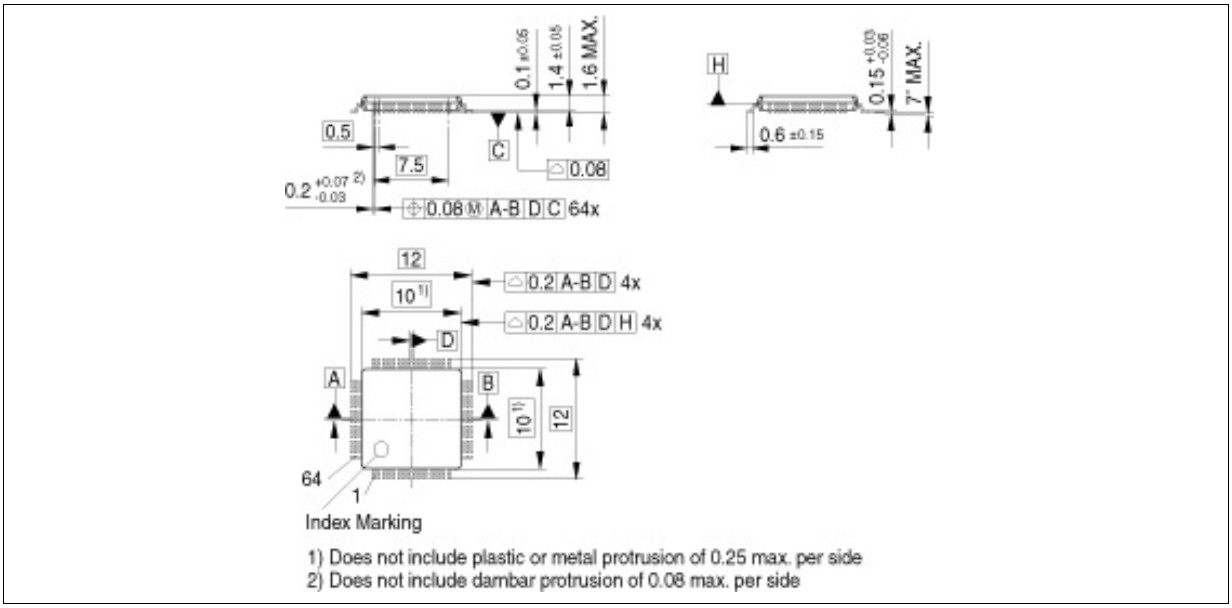

Figure 21 Package Outlines PG-TQFP-64, Plastic Green Thin profile Quad Flat Package

4.4.3 Quality Declarations

Table 19 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1)2)]	t_{OP}	–	–	24000	hours	at average weighted junction temperature T_j = 127°C
		–	–	66000	hours	at average weighted junction temperature T_j = 100°C
		–	–	20	years	at average weighted junction temperature T_j = 85°C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Soldered Device Model (SDM)	V_{SDM}	–	–	1000	V	Conforming to EOS/ESD-DS5.3-1993
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.

2)One example of a detailed temperature profile is:

2000 hours at T_j = 150°C
16000 hours at T_j = 125°C
6000 hours at T_j = 110°C

This example is equivalent to the operation lifetime and average temperatures given in the table.

4.4.4 Thermal Considerations

When operating the SAK-CIC310-OSMX2HT in a system, the total heat generated on the chip must be dissipated to the ambient environment to prevent overheating and resulting thermal damages.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” is a measure for these parameters. The power dissipation must be limited so the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = \Sigma(V_{DDP} \times I_{DDP}) + \Sigma(V_{DD} \times I_{DD}) + (V_{DDAPLL} \times I_{DDAPLL}) + (V_{DDPOSC} \times I_{DDPOSC}) + (V_{DDOSC} \times I_{DDOSC})$.

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and the switching frequencies.

If the total power dissipation determined for a given system configuration exceeds the defined limit countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, V_{DD}, V_{DDPOSC}, V_{DDOSC}, and V_{DDAPLL} if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

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