Winbond Electronics Corp.

# PCI TO ISA BRIDGE SET

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## 1. GENERAL DESCRIPTION

W83628F is a PCI-to-ISA bus conversion IC. W83629D is a condensed centralizer IC for IRQ and DMA control. W83628F and W83629D together form a complete set for the PCI-to-ISA bridge.

For the new generation Intel chipset Camino and Whitney, featuring LPC bus, there is no support for ISA bus and slots. However the demand of ISA devices still exist. For such case, W83628F plus W83629D are the best companion solution for the non-ISA chipset. Also the packages of W83628F (128-QFP) and W83629D (48-LQFP) had been chosen to be the most economic solution for save the M/B board layout size and cost.

For the new generation chipset featuring LPC interface and support no ISA bus, W83627HF/F (Winbond LPC I/O) together with the set of W83628F and W83629D is the complete solution.

## 2. FEATURES

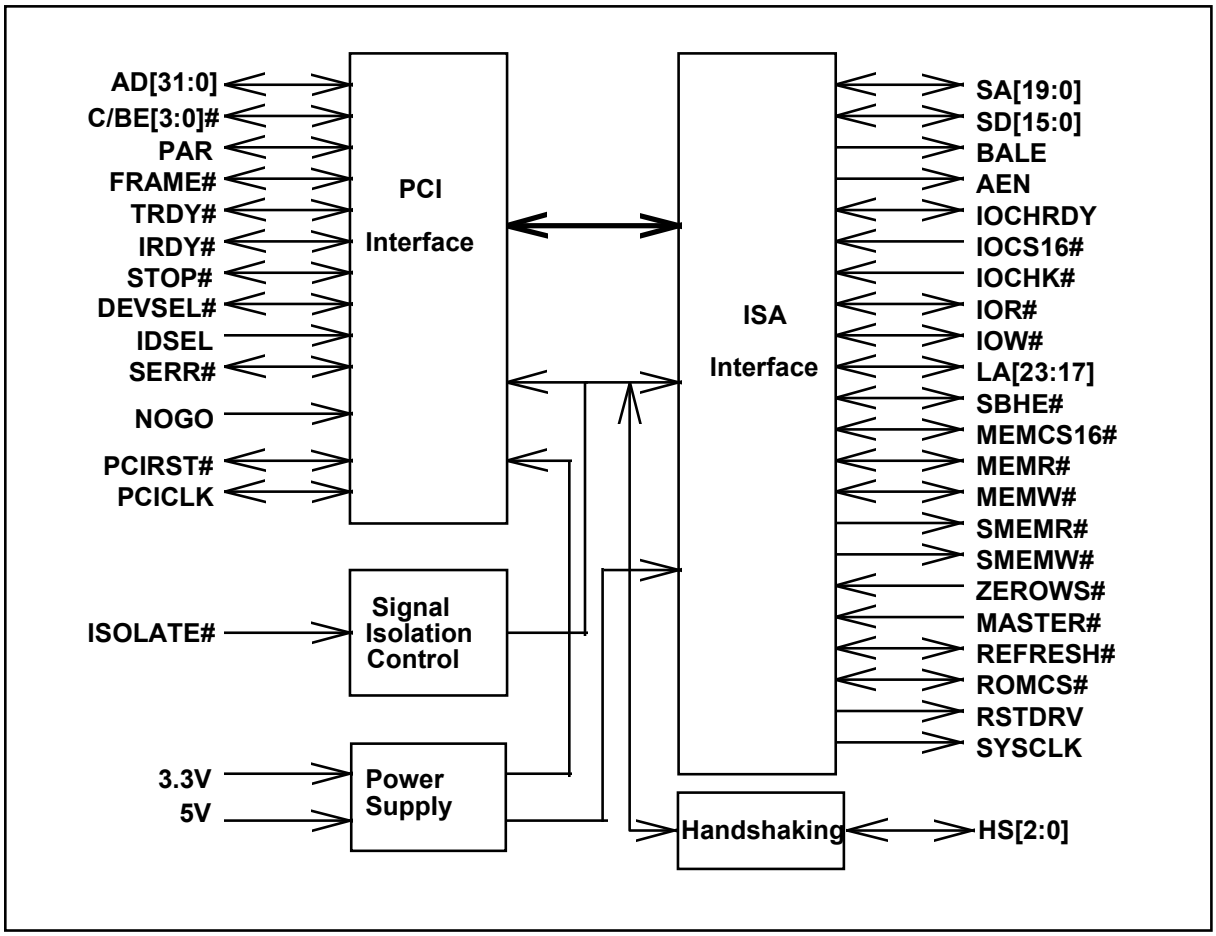
### PCI to ISA Bridge

- Full ISA Bus Support including ISA Masters
- 5V ISA and 3.3V PCI interfaces
- PC/PCI DMA protocol for Software Transparent
- IRQ Serializer for ISA Parallel IRQ transfer to Serial IRQ
- Supports 3 fully ISA Compatible Slots without Buffering
- PCI Bus at 25MHz, 33MHz and up to 40MHz
- Supports Programmable ISA Bus Divide the PCI Bus Clock into 3 or 4
- All ISA Signals can be Isolate
- Supports Configuration registers for programming performance

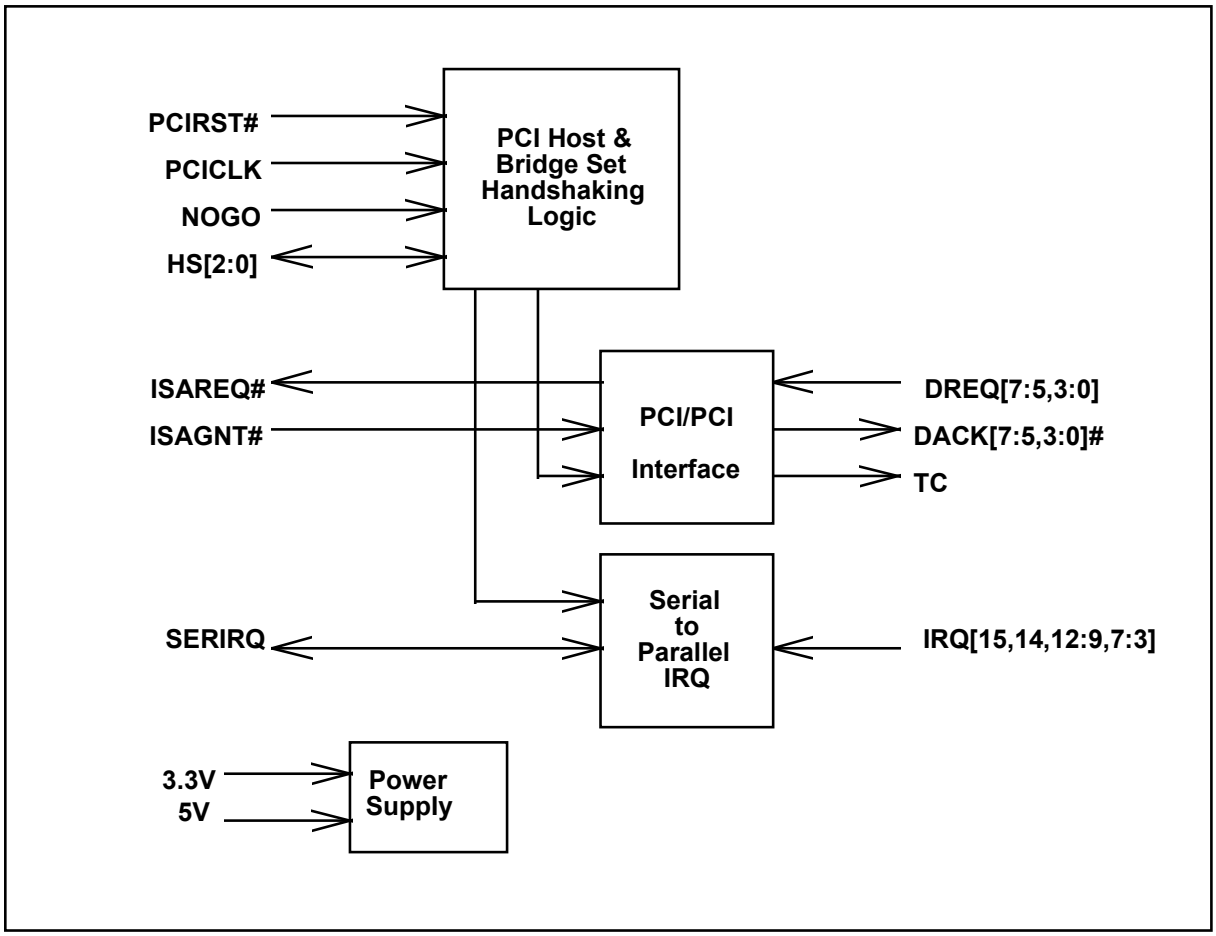
## 3. PACKAGE

- 128-pin PQFP for W83628F
- 48-pin LQFP for W83629D

## 4. BLOCK DIAGRAM OF W83628F

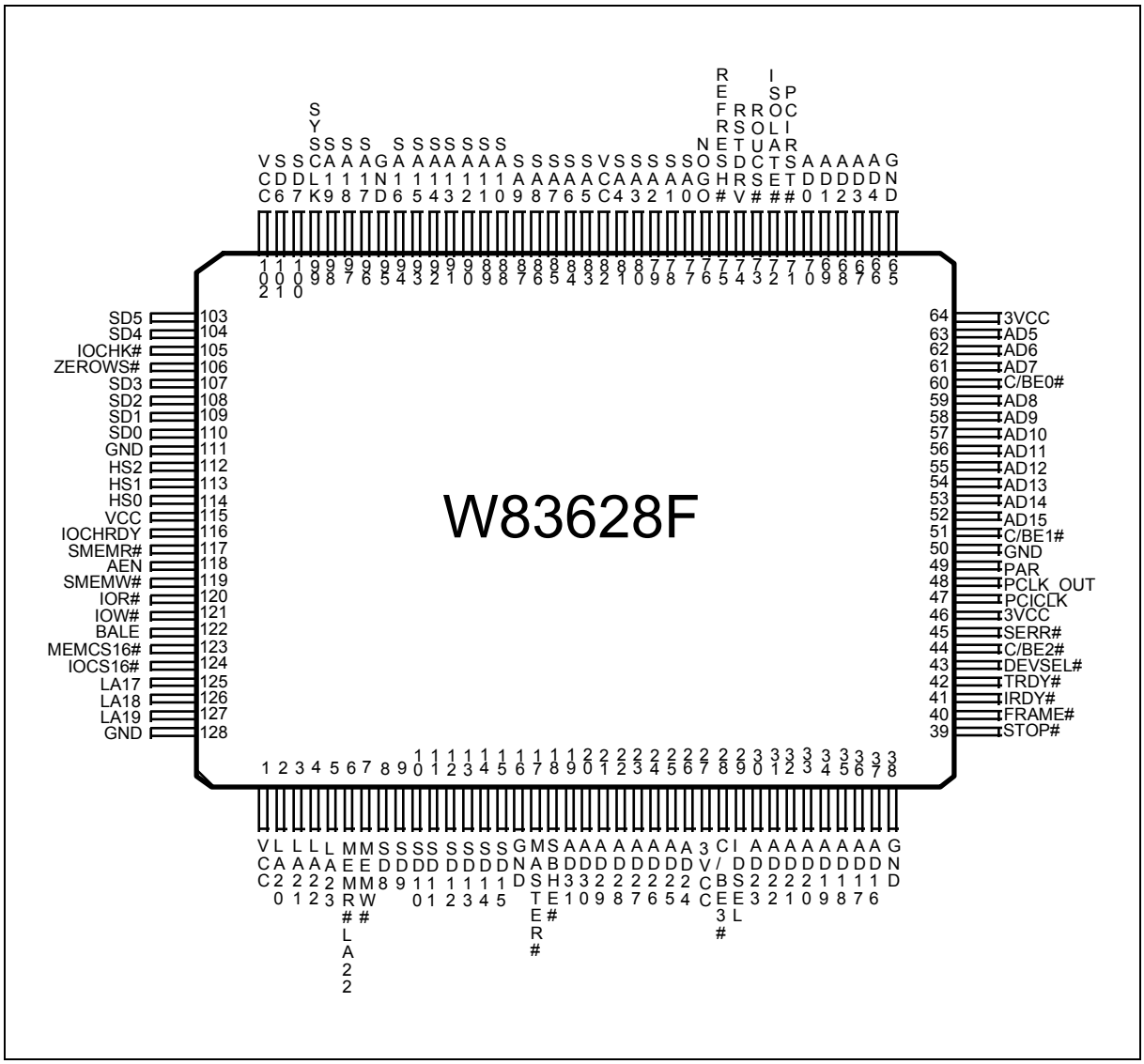


## 5. BLOCK DIAGRAM OF W83629D

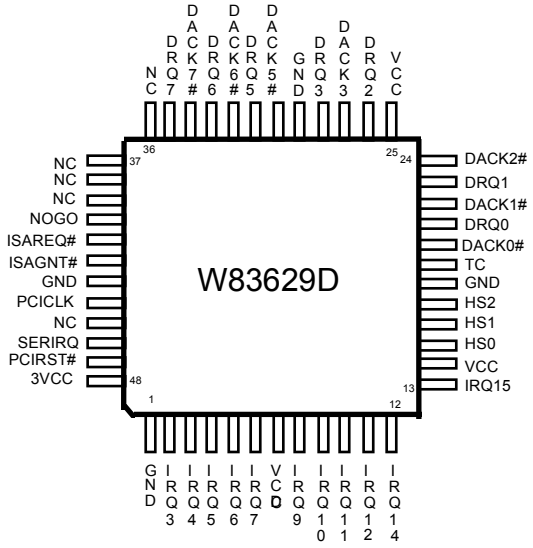


# 6. PIN CONFIGURATION

## 6.1 PIN CONFIGURATION FOR 628F



## 6.2 PIN CONFIGURATION FOR 629D



# 7. PIN DESCRIPTION

**Note:** Please refer to Section 13.2 DC CHARACTERISTICS for details.

$I/O_{12t}$ - TTL level bi-directional pin with 12 mA source-sink capability

$I/O_{24t}$ - TTL level bi-directional pin with 24 mA source-sink capability

$I/O_{12tp3}$ - 3.3V TTL level bi-directional pin with 12 mA source-sink capability

$I/O_{24tp3}$ - 3.3V TTL level bi-directional pin with 24 mA source-sink capability

$I/OD_{12t}$ - TTL level bi-directional pin open drain output with 12 mA sink capability

$I/O_{24t}$ - TTL level bi-directional pin with 24 mA source-sink capability

$OUT_{12t}$ - TTL level output pin with 12 mA source-sink capability

$OUT_{24t}$ - TTL level output pin with 24 mA source-sink capability

$OUT_{12tp3}$ - 3.3V TTL level output pin with 12 mA source-sink capability

$OUT_{24tp3}$ - 3.3V TTL level output pin with 24 mA source-sink capability

$OD_{12}$ - Open-drain output pin with 12 mA sink capability

$OD_{24}$ - Open-drain output pin with 24 mA sink capability

$IN_{cs}$ - CMOS level Schmitt-trigger input pin

$IN_{t}$ - TTL level input pin

$IN_{td}$ - TTL level input pin with internal pull down resistor

$IN_{ts}$ - TTL level Schmitt-trigger input pin

$IN_{tsp3}$ - 3.3V TTL level Schmitt-trigger input pin

## 7.1 W83628F PIN DESCRIPTION

### 7.1.1 PCI Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| AD[31:0] | 19-26<br>30-37<br>52-59<br>61-63<br>66-70 | $I/O_{24tp3}$ | **PCI Bus Address and Data Signals.** The standard PCI address and data lines. Address is driven with FRAME# assertion, data is driven or received in following clocks. |
| C/BE[3:0]# | 28,45<br>51,60 | $I/O_{24tp3}$ | **PCI Bus Command and Byte Enables.** During the address phase of a transaction C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. |
| PCICLK | 47 | $IN_{t}$ | **PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. |
| PCLK_OUT | 48 | $OUT_{12t}$ | **PCI Bus System Clock DPLL Output.** The PCLK_OUT can reduce the PCICLK Loading and it produced from internal DPLL. |

4.1.1 PCI Interface, contiuned

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| FRAME# | 40 | $I/O_{24tp3}$ | **Frame Signal**. FRAME# is driven by the current PCI bus master to indicate the beginning and duration of an access. |
| IDSEL | 29 | $IN_t$ | **Initialization Device Select.** IDSEL is used as a chip select during configuration read and write transactions. This signal should be externally tied to one of the upper 21 address signals. |
| STOP# | 39 | $I/O_{12tp3}$ | **Bus Stop#.** STOP# indicates the current target is requesting the master to stop the current PCI bus transaction. |
| IRDY# | 41 | $I/O_{12tp3}$ | **Initiator Ready.** IRDY# indicates the initiating agent ability to complete the current data phase of the PCI bus transaction. |
| TRDY# | 42 | $I/O_{12tp3}$ | **Target Ready.** TRDY# indicates the target agent's ability to complete the current data phase of the PCI bus transaction. |
| DEVSEL# | 43 | $I/O_{12tp3}$ | **Device Select.** W83628F drives DEVSEL# to indicate that it is the target of the current PCI bus transaction. W83628F uses subtractive decoding and the NOGO protocol to claim PCI transactions. |
| SERR# | 45 | $OD_{12}$ | **System Error.** SERR# can be pulsed active by any PCI agent that detects a system error condition. |
| PAR | 49 | $I/O_{12tp3}$ | **Parity Signal.** W83628F generates even parity across AD[31:0] and C/BE[3:0]#. |
| PCIRST# | 71 | $IN_t$ | **PCI Reset.** W83628F receives PCIRST# as a reset from the PCI Bus. |

### 7.1.2 Control Logic and Handshaking Signals

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| HS[2:0] | 112-114 | $I/O_{12}$ | **Handshaking Signals.** HS[2:0] connected to W83629D for PCI to ISA SET handshaking signals.<br>***HS1 is handshaking Signal 1, this pin weak pulled-down during PCIRST# is asserted, and apply a pull-up resistor(4.7Kohm) to this pin disables ISA bridge subtraction decoder.*** |
| ISOLATE# | 72 | $IN_t$ | **Isolation Control Input. Isolate#** is an active low signal by user programming to control the W83628F all output signals to Isolation and Tri-state. |
| NOGO | 76 | $IN_t$ | **NOGO,** This signal indicates which master initiated the current transaction and also indicates whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and W83628F. |

### 7.1.3 ISA Interface Signals

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SA[19:17] | 98-96 | $OUT_{24t}$ | **System Address Bus.** These are the upper address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[19:17] are at an unknown state upon PCIRST#. |
| SA[16:0] | 94-83<br>81-77 | $I/O_{24t}$ | **System Address Bus.** These are the bi-directional lower address lines that define the ISA's byte granular address space (up to 1 Mbyte). SA[16:0] are at an unknown state upon PCIRST#. |
| SD[15:0] | 110-107,<br>104,<br>103,<br>101,<br>100,<br>8-15 | $I/O_{24t}$ | **System Data.** SD[15:0] provide the 16-bit data path for devices residing on the ISA Bus. The W83628F tri-states SD[15:0] during PCIRST#. |
| AEN | 118 | $OUT_{24t}$ | **Address Enable.** AEN is asserted during DMA cycles. This signal is also driven high during W83628F initiated refresh cycles. AEN is driven low upon PCIRST#. |
| IOR# | 120 | $I/O_{24t}$ | **I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). |
| IOW# | 121 | $I/O_{24t}$ | **I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (SD[15:0]). |
| IOCHRDY | 116 | $I/O_{24t}$ | **I/O Channel Ready.** Resources on the ISA Bus negate IOCHRDY to indicate that additional time (wait states) is required to complete the cycle. |
| SYSCLK | 99 | $OUT_{24t}$ | **ISA System Clock.** SYSCLK is the reference clock for the ISA bus. The SYSCLK is generated by dividing PCICLK by 3 or 4. |
| RSTDRV | 74 | $OUT_{24t}$ | **Reset Drive.** W83628F asserts RSTDRV to reset devices that reside on the ISA Bus. The W83628F asserts this signal while the PCIRST# is asserted. |
| IOCS16# | 124 | $IN_t$ | **16-bit I/O Chip Select.** This signal is driven by I/O devices on the ISA Bus to indicate that they support 16-bit I/O bus cycles. |
| SBHE# | 18 | $I/O_{24t}$ | **System Byte High Enable.** SBHE# asserted indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is at an unknown state upon PCIRST#. |
| IOCHK# | 105 | $IN_t$ | **I/O Channel Check.** IOCHK# can be driven by any resource on the ISA bus during on detection of an error. |

4.1.3 ISA Interface Signals, contiuned

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| MEMR# | 6 | $I/O_{24t}$ | **Memory Read.** MEMR# asserted indicates the current ISA bus cycle is a memory read. |
| MEMW# | 7 | $I/O_{24t}$ | **Memory Write.** MEMW# asserted indicates the current ISA bus cycle is a memory write. |
| MASTER# | 17 | $IN_t$ | **MASTER#.** This signal is used with a DREQ line by an ISA master to gain control of the ISA Bus. |
| LA[23:17] | 5-2<br>127-125 | $I/O_{24t}$ | **Unlatched Address.** The LA[23:17] address lines are bi-directional. These address lines allow accesses to physical memory on the ISA Bus up to 16 Mbytes. LA[23:17] are outputs when the W83628F owns the ISA Bus. |
| ROMCS# | 73 | $I/O_{12}$ | ***ROMCS# ,this pin weak pulled-down during PCIRST is asserted, and apply a pull-up resistor (4.7 Kohm) to this pin enable positive decoder of BIOS address range (depend on Configure register 70 , bit 3,2). When BIOS assress range is enabled , the PIN is BIOS ROM CS# output.*** |
| REFRESH# | 75 | $I/O_{24t}$ | **Refresh.** REFRESH# asserted indicates that a refresh cycle is in progress, or that an ISA master is requesting W83628F to generate a refresh cycle. Upon PCIRST#, this signal is tri-stated. |
| ZEROWS# | 106 | $IN_t$ | **Zero Wait States.** An ISA slave asserts ZEROWS# after its address and command signals have been decoded to indicate that the current cycle can be executed as an ISA zero wait state cycle. ZEROWS# has no effect during 16-bit I/O cycles. |
| SMEMR# | 117 | $OUT_{24t}$ | **Standard Memory Read.** SMEMR# asserted indicates the current ISA bus cycle is a memory read cycle to an address below 1 Mbyte. |
| SMEMW# | 119 | $OUT_{24t}$ | **Standard Memory Write.** SMEMW# asserted indicates the current ISA bus cycle is a memory write cycle to an address below 1 Mbyte. |
| BALE | 122 | $OUT_{24t}$ | **Bus Address Latch Enable.** BALE is an active high signal asserted by the W83628F to indicate that the address (SA[19:0], LA[23:17]) and SBHE# signal lines are valid.<br>The LA[23:17] address lines are latched on the trailing edge of BALE. BALE remains asserted throughout DMA and ISA master cycles. BALE is driven low upon PCIRST#. |
| MEMCS16# | 123 | $OD_{24}$ | **Memory Chip Select 16.** MEMCS16# asserted indicates that the memory slave supports 16-bit accesses. |

### 7.1.4 Power Signals

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| VCC | 1, 82, 102, 115 | PWR | **5V Supply.** |
| 3VCC | 27, 46, 64 | PWR | **3.3V Supply.** |
| GND | 16, 38, 50, 65, 95, 111, 128 | PWR | **Ground.** |

## 7.2 W83629D PIN DESCRIPTION

### 7.2.1 Control Logic and Handshaking Signals

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| HS[2:0] | 17-15 | $I/O_{12}$ | **Handshaking Signals.** HS[2:0] connected to W83628F for PCI to ISA SET handshaking signals. |
| NOGO | 40 | $IN_t$ | **NO GO.** This signal indicates which master initiated the current transaction and also indicates whether or not the current bus cycle is targeted for the ISA bus. This signal is a point-to-point connection between PCI HOST Bridge and W83628F. |
| PCICLK | 44 | $IN_t$ | **PCI Bus System Clock**. PCICLK provides timing for all transactions on the PCI bus. All other PCI signals are sampled on the rising edge of PCICLK, and all timing parameters are defined with respect to this edge. |
| PCIRST# | 47 | $IN_t$ | **PCI Reset.** W83628F receives PCIRST# as a reset from the PCI Bus. |

### 7.2.2 PC/PCI Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| ISAREQ# | 41 | $OUT_{24t}$ | **ISA Bus Request.** This signal is a point-to-point signal between W83629D and a PCI HOST arbiter . The W83629D asserts this signal according to the PC/PCI protocol. |
| ISAGNT# | 42 | $IN_t$ | **ISA Bus Grant.** This signal is a point-to-point signal between W83629D and a PCI HOST Bridge's secondary bus PCPCIGNT# signal. W83629D asserts this signal according to the PC/PCI protocol. |
| DRQ [7:5,3:0] | 35,33 31,28 26,23 21 | $IN_t$ | **DMA Request.** The DREQ signal indicates that either a slave DMA device is requesting DMA services, or an ISA bus master is requesting use of the ISA bus. |
| DACK [7:5,3:0]# | 34,32 30,27 24,22 20 | $OUT_{24t}$ | **DMA Acknowledge.** The DACK# signal indicates that either a DMA channel or an ISA bus master has been granted the ISA bus. |
| TC | 19 | $OUT_{24t}$ | **Terminal Count.** The W83628F asserts TC to DMA slaves as a terminal count indicator. |

### 7.2.3 IRQ Serializer Interface

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| SERIRQ | 46 | I/OD12t | **Serial Interrupt Requested Signals.** This signal is for transfer IRQ mode between parallel IRQ to serial IRQ. |
| IRQ [3:7,9:12,14,15] | 2-6<br>8-13 | INt | **Parallel Interrupt Requested Input.** |

### 7.2.4 Power Signals

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| VCC | 7, 14, 25 | PWR | **5V Supply.** |
| 3VCC | 48 | PWR | **3.3V Supply.** |
| GND | 1, 18, 29, 43 | PWR | **Ground.** |

### 7.2.5 NC Pins

| SYMBOL | PIN | I/O | FUNCTION |
|---|---|---|---|
| NC | 36, 37,38, 39, 45 | | **No Connection.** |

# 8. PCI CONFIGURATION REGISTERS

## 8.1 VID-VENDOR IDENTIFICATION REGISTER

Address Offset: 00-01h

Default Value: 1050h

Attribute: Read only

This register is read-only and contains Winbond vendor identification number(1050h).

## 8.2 DID-DEVICE IDENTIFICATION REGISTER

Address Offset: 02-03h

Default Value: 0628h

Attribute: Read only

This register is read-only and contains the device identification number(0628h).

## 8.3 PCICMD-PCI COMMAND REGISTER

Address Offset: 04-05h

Default Value: 0007h

Attribute: Read/Write

This register provides control over ISA bridge to generate and response to PCI cycles properly. When a 0 is written to this register, ISA bridge is to be disconnected from PCI bus for all accesses except configuration accesses.

**Bit 15:10** **Reserved.**

**Bit 9** **Fast Back to Back.** This bit always returns a zero.

**Bit 8** **SERR# Enable.**

=1 Enable.

=0 Disable.

**Bit 7** **Wait Cycle Control(Not supported).**

Hardwired to zero.

**Bit 6** **Parity Error Response(Not supported).**

Hardwired to zero.

**Bit 5** **VGA Palette Snoop Enable(Not supported).**

Hardwired to zero.

**Bit 4** **Memory Write and Invalidate Enable(Not supported).**

Hardwired to zero.

**Bit 3** **Parity Error Response(Not supported).**

Hardwired to zero.

**Bit 2** **Bus Master Enable.**

Hardwired to one. The ISA bridge Bus Masters are always supported to generate a PCI Bus master cycle.

**Bit 1** **Memory Space Enable.**

Hardwired to one. The ISA bridge Memory space is always enabled.

**Bit 0** **I/O Space Enable.**

Hardwired to one. The ISA bridge I/O space is always enabled.

## 8.4 PCISTS-PCI STATUS REGISTER

Address Offset: 06-07h

Default Value: 0200h

Attribute: Read/Write

This register shows status information for PCI bus related events.

**Bit 15** **Detected Parity Error.**

Hardwired to zero. The ISA bridge does not check bus parity.

**Bit 14** **Signaled System Error.**

This bit is set when ISA bridge asserts SERR# on PCI bus.

**Bit 13** **Received Master Abort Status.**

This bit is set when the ISA bridge is target aborted as a master on the PCI bus. Software sets this bit to 0 by writing a 1 to it.

**Bit 12** **Received Target Abort Status.**

This bit is set when the ISA bridge target aborts a PCI transaction as a target. Software sets this bit to 0 by writing a 1 to it.

**Bit 11** **Signaled Target Abort Status.**

This bit is set when the ISA bridge signals a target abort for a PCI transaction. Software sets this bit to 0 by writing a 1 to it.

**Bit 10:9** **DEVSEL# Timing.** This 2 bits always return a 01b(medium decode).

**Bit 8** **Data Parity Detected(Not supported).**

Hardwired to zero.

**Bit 7** **Fast Back-to-Back(Not supported).**

Hardwired to zero.

**Bit 6** **66 MHz/ 33 MHz(Only support 33 MHz).**
Hardwired to zero.

**Bit 5** **User Defineable Features(Not supported).**
Hardwired to zero.

**Bit 4:0** **Reserved.**
Reserved and will returns zero when reading this register.

## 8.5 REVID-REVISION IDENTIFICATION REGISTER

Address Offset: 08h
Default Value: See lastest stepping information
Attribute: Read Only

This register shows status information for PCI bus related events.

**Bit 7:0** **Revision Identification Number.**

## 8.6 CCODE-CALSS CODE REGISTER

Address Offset: 09-0Bh
Default Value: 060100h
Attribute: Read Only

The class code register is a read-only register and used to identify the ISA bridge.

**Bit 23:16** **Base Class Code.**
06h = Bus Bridge

**Bit 15:8** **Sub-Class Code.**
01h = PCI to ISA Bridge

**Bit 7:0** **Programming Interface.**
00h

## 8.7 HEADT-HEAD TYPE REGISTER

Address Offset: 0Eh
Default Value: 00h
Attribute: Read Only

The register is a read-only register and used to indicate that the ISA bridge configuration space adheres to PCI local bus specification. It also indicates that ISA bridge is not a multifunction device.

**Bit 7** **Multifunction Indicator.**
0 = Not a multifunction device.

**Bit 6:0** **Layout Code.**
00h = PCI layout type.

## 8.8 IO_RCVR-IO RECOVERY REGISTER

Address Offset: 40h

Default Value: 4Dh

Attribute: Read/Write

**Bit 7** **SYSCLK Divider.**

0 = SYSCLK is equal to PCICLK divided by 4.

1 = SYSCLK is equal to PCICLK divided by 3.

**Bit 6** **8-bit I/O Recovery Enable**

0 = Disable bits 5:3 setting and uses 3.5 SYSCLKs for 8 bit I/O recovery time.

1 = Enable bits 5:3 setting.

**Bit 5:3** **8-bit I/O RecoveryTimes.**

When bit 6=1 ,this 3-bit field defines the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 8 bit I/O

000 =0 SYSCLK

001 =1 SYSCLK

010 =2 SYSCLKs

011 =3 SYSCLKs

100 =4 SYSCLKs

101 =5 SYSCLKs

110 =6 SYSCLKs

111 = 7 SYSCLKs

**Bit 2** **16-bit I/O Recovery Enable.**

= 0 Ignore bits 1:0 setting and uses 3.5 SYSCLKs for 16-bit I/O recovery time.

= 1 The 16-bit I/O recovery time is decided by bits 1:0.

**Bit 1:0** **16-bit I/O Recovery Times.**

When bit 2=1 ,this 2-bit field defines the additional number of SYSCLKs added to standard 3.5 SYSCLK recovery time for 16 bit I/O

= 01 1 SYSCLK

= 10 2 SYSCLKs

= 11 3 SYSCLKs

= 00 4 SYSCLKs

## 8.9 WISA_STS-ISA BRIDGE ERROR STATUS REGISTER

Address Offset: 42h

Default Value: 00h

Attribute: Read/Write

**Bit 7:3** **Reserved.**

**Bit 2** **IOCHK# Pin State.**

This bit reflects the inverse state of IOCHK# pin on the ISA bus.

**Bit 1** **Reserved.**

**Bit 0** **Byte Lane Error.**

This bit is set if the ISA bridge detects an illegal byte lane combination for a PCI I/O cycles.

## 8.10 WISA_FADC-ISA BRIDGE FAST DECODERS CONTROL REGISTER

Address Offset: 50h

Default Value: 00h

Attribute: Read/Write

**Bit 7** **Enable/Disable Fast I/O Address Decoder # 7.**

**Bit 6** **Enable/Disable Fast I/O Address Decoder # 6.**

**Bit 5** **Enable/Disable Fast I/O Address Decoder # 5.**

**Bit 4** **Enable/Disable Fast I/O Address Decoder # 4.**

**Bit 3** **Enable/Disable Fast I/O Address Decoder # 3.**

**Bit 2** **Enable/Disable Fast I/O Address Decoder # 2.**

**Bit 1** **Enable/Disable Fast I/O Address Decoder # 1.**

**Bit 0** **Enable/Disable Fast I/O Address Decoder # 0.**

## 8.11 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 0 MASK CONTROL REGISTER

Address Offset: 58h

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 0, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 0.

## 8.12 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 1 MASK CONTROL REGISTER

Address Offset: 59h

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 1, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 1.

### 8.13 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 2 MASK CONTROL REGISTER

Address Offset: 5Ah

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 2, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 2.

### 8.14 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 3 MASK CONTROL REGISTER

Address Offset: 5Bh

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 3, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 3.

### 8.15 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 4 MASK CONTROL REGISTER

Address Offset: 5Ch

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 4, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 4.

### 8.16 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 5 MASK CONTROL REGISTER

Address Offset: 5Dh

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 5, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 5.

### 8.17 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 6 MASK CONTROL REGISTER

Address Offset: 5Eh

Default Value: 00h

Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 6, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 6.

### 8.18 WISA_FAD0MC-ISA BRIDGE FAST DECODERS # 7 MASK CONTROL REGISTER

Address Offset: 5Fh
Default Value: 00h
Attribute: Read/Write

This register is used to mask address bits(A7~A0) for fast address decoder # 7, if the corresponding bit of this register is set to a 1, the corresponding address bit(A7~A0) is ignore by the faster address decoder # 7.

### 8.19 WISA_FADCB0-ISA BRIDGE FAST DECODERS # 0 BASE ADDRESS REGISTER

Address Offset: 60-61h**
Default Value: 0000h
Attribute: Read/Write

This register contains the base address for fast address decoder # 0.A

***Note: 60h is lower byte and 61h is upper byte.***

### 8.20 WISA_FADCB1-ISA BRIDGE FAST DECODERS # 1 BASE ADDRESS REGISTER

Address Offset: 62-63h
Default Value: 0000h
Attribute: Read/Write

This register contains the base address for fast address decoder # 1.

### 8.21 WISA_FADCB2-ISA BRIDGE FAST DECODERS # 2 BASE ADDRESS REGISTER

Address Offset: 64-65h
Default Value: 0000h
Attribute: Read/Write

This register contains the base address for fast address decoder # 2.

### 8.22 WISA_FADCB3-ISA BRIDGE FAST DECODERS # 3 BASE ADDRESS REGISTER

Address Offset: 66-67h
Default Value: 0000h
Attribute: Read/Write

This register contains the base address for fast address decoder # 3.

### 8.23 WISA_FADCB4-ISA BRIDGE FAST DECODERS # 4 BASE ADDRESS REGISTER

Address Offset: 68-69h
Default Value: 0000h
Attribute: Read/Write

This register contains the base address for fast address decoder # 4.

### 8.24 WISA_FADCB5-ISA BRIDGE FAST DECODERS # 5 BASE ADDRESS REGISTER

Address Offset: 6A-6Bh
Default Value: 0000h
Attribute: Read/Write
This register contains the base address for fast address decoder # 5.

### 8.25 WISA_FADCB6-ISA BRIDGE FAST DECODERS # 6 BASE ADDRESS REGISTER

Address Offset: 6C-6Dh
Default Value: 0000h
Attribute: Read/Write
This register contains the base address for fast address decoder # 6.

### 8.26 WISA_FADCB7-ISA BRIDGE FAST DECODERS # 6 BASE ADDRESS REGISTER

Address Offset: 6E-6Fh
Default Value: 0000h
Attribute: Read/Write
This register contains the base address for fast address decoder # 0.

### 8.27 WISA_CTRLREG1-ISA BRIDGE CONTROL REGISTER 1

Address Offset: 70h
Default Value: 0000*01s*sb
Attribute: Read/Write

***Power-on setting bits bit 1:0 are power-on set by ROMCS# and HS1.***

**Bit 7-6** **Reserved.**

**Bit 5-4** **= 00 Send AD Bus with no STEP**
**= 01 Send AD Bus with 2 STEP**
**= 10 Send AD Bus with 4 STEP**
**= 11 Reverse**

***Bit 3-2 = 00 1MB BIOS ROM positive decode.***
***= 01 2MB BIOS ROM positive decode.***
***= 10 4MB BIOS ROM positive decode.***
***= 11 8MB BIOS ROM positive decode.***

***Bit 1 =0 Disable High-Address BIOS ROM decoder.***
***=1 Enable High-Address BIOS ROM decoder.***
***This bit can be set/reset by ROMCS# power-on setting during PCIRST# assert.***

**Bit 0** **=0 Normal mode.**
**=1 Disable ISA Bridge subtraction decoder.**
***This bit can be set/reset by HS1 power-on setting during PCIRST# assert.***

### 8.28 WISA_CTRLREG2-ISA BRIDGE CONTROL REGISTER 2

Address Offset: 71h
Default Value: 00h
Attribute: Read/Write

**Bit7** **=0 Enable IRQ11.**
**=1 Disable IRQ11.**
**Bit 6** **=0 Enable IRQ10.**
**=1 Disable IRQ10.**
**Bit 5** **=0 Enable IRQ9.**
**=1 Disable IRQ9.**
**Bit 4** **=0 Enable IRQ7.**
**=1 Disable IRQ7.**
**Bit 3** **=0 Enable IRQ6.**
**=1 Disable IRQ6.**
**Bit 2** **=0 Enable IRQ5.**
**=1 Disable IRQ5.**
**Bit 1** **=0 Enable IRQ4.**
**=1 Disable IRQ4.**
**Bit 0** **=0 Enable IRQ3.**
=1 Disable IRQ3.

### 8.29 WISA_CTRLREG3-ISA BRIDGE CONTROL REGISTER 3

Address Offset: 72h
Default Value: 00h
Attribute: Read/Write

**Bit 7-3** **Reserved.**
**Bit 2** **=0 Enable IRQ15.**
**=1 Disable IRQ15.**
**Bit 1** **=0 Enable IRQ14.**
**=1 Disable IRQ14.**
**Bit 0** **=0 Enable IRQ12.**
**=1 Disable IRQ12.**

## 8.30 WISA_CTRLREG4-ISA BRIDGE CONTROL REGISTER 4

Address Offset: 73h
Default Value: 00h
Attribute: Read/Write

**Bit7** **=0 Enable DRQ 7.**
**=1 Disable DRQ 7.**
**Bit 6** **=0 Enable DRQ6.**
**=1 Disable DRQ6.**
**Bit 5** **=0 Enable DRQ5.**
**=1 Disable DRQ5.**
**Bit 4** **Reserved.**
**Bit 3** **=0 Enable DRQ 3.**
**=1 Disable DRQ 3.**
**Bit 2** **=0 Enable DRQ 2.**
**=1 Disable DRQ 2.**
**Bit 1** **=0 Enable DRQ 1.**
**=1 Disable DRQ 1.**
**Bit 0** **=0 Enable DRQ 0.**
**=1 Disable DRQ 0.**

## 8.31 WISA_TSTREG-ISA BRIDGE TEST REGISTER

Address Offset: 80h
Default Value: 04h
Attribute: Read/Write

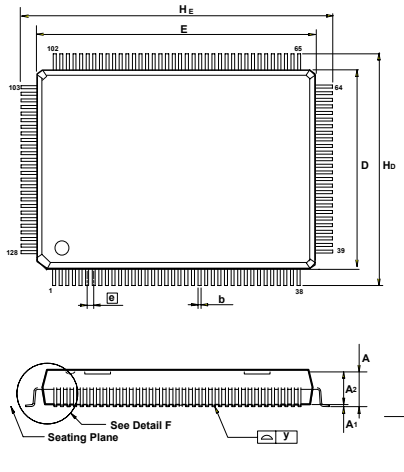
**Bit 7-5** **Reserved and should not write data to this register.**

***Bit 4*** ***=0 80h port decoding on subtrastive cycles of LPC I/F.***
***=1 80h port decoding on positive cycles of LPC I/F.***
***This Bit must be set 1when LPC I/F is only decoding on positive cycles,but when the bridge is used in PIIX4 for test set the bit to 0 .***

**Bit 3** **Reserved and should not write data to this register.**

***Bit 2-0*** ***000 - 0.8 nS. For Winbond Internal Reference only.***
***001 - 0.6 nS.***
***010 - 0.4 nS.***
***011 - 0.2 nS.***
***100 0 nS.***
***101 +0.2 nS.***
***110 +0.4 nS.***
***111 +0.6 nS.***

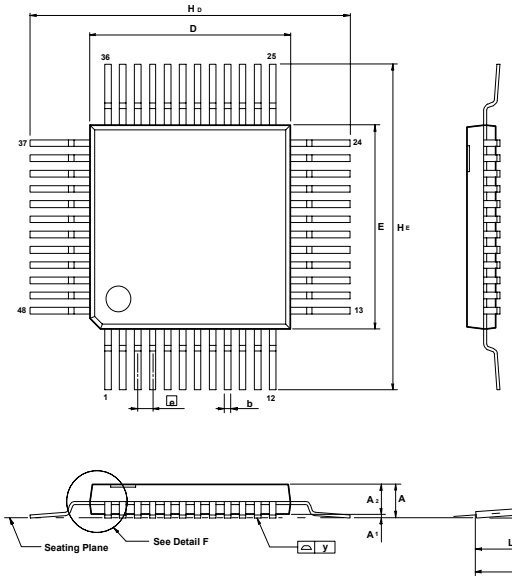
## 9. PACKAGE DIMENSIONS 1 FOR W83628F (128-PIN PQFP)




| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| $A_1$ | 0.25 | 0.35 | 0.45 | 0.010 | 0.014 | 0.018 |
| $A_2$ | 2.57 | 2.72 | 2.87 | 0.101 | 0.107 | 0.113 |
| b | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 13.90 | 14.00 | 14.10 | 0.547 | 0.551 | 0.555 |
| E | 19.90 | 20.00 | 20.10 | 0.783 | 0.787 | 0.791 |
| e | —— | 0.50 | —— | —— | 0.020 | —— |
| $H_D$ | 17.00 | 17.20 | 17.40 | 0.669 | 0.677 | 0.685 |
| $H_E$ | 23.00 | 23.20 | 23.40 | 0.905 | 0.913 | 0.921 |
| L | 0.65 | 0.80 | 0.95 | 0.025 | 0.031 | 0.037 |
| $L_1$ | —— | 1.60 | —— | —— | 0.063 | —— |
| y | —— | —— | 0.08 | —— | —— | 0.003 |
| θ | 0 | —— | 7 | 0 | —— | 7 |

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

## 10. PACKAGE DIMENSIONS 2 FOR W83629D (48-PIN LQFP)




| Symbol | Dimension in inch | | | Dimension in mm | | |
|---|---|---|---|---|---|---|
| | Min. | Nom. | Max. | Min. | Nom. | Max. |
| A | | | | --- | --- | 1.60 |
| $A_1$ | | | | 0.05 | --- | 0.15 |
| $A_2$ | | | | 1.35 | 1.40 | 1.45 |
| b | | | | 0.17 | 0.20 | 0.27 |
| c | | | | 0.09 | --- | 0.20 |
| D | | | | | 7.00 | |
| E | | | | | 7.00 | |
| e | | | | | 0.50 | |
| $H_D$ | | | | | 9.00 | |
| $H_E$ | | | | | 9.00 | |
| L | | | | 0.45 | 0.60 | 0.75 |
| $L_1$ | | | | | 1.00 | |
| y | | | | --- | 0.08 | --- |
| θ | | | | 0 | 3.5° | 7 |

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

## 11. REVISION HISTORY

| VERSION | DATE | PAGE | DESCRIPTION |
|---|---|---|---|
| | 1998.11.16 | | Add High-Address BIOS ROM decoder function(CS#/HS3). (Page 7 & Page 20) |
| | 1998.11.19 | | Change decode range to #FFF00000~#FFFFFFFF & #000E0000~#000FFFFF. |
| | 1999.01.17 | | Supports 3 fully ISA Compatible Slots without Buffering.<br>Rename HS3. it is renamed to ROMCS# in W83628F,and NC in W83629D. |
| 0.32 | 1999.04.21 | | Indicate the Bit 4 of offset address 80h is used to enable 80h port decoding when only positive decoding switched of LPC I/F. |
| A1 | May 18, 2005 | 25 | ADD Important Notice |
| | | | |

### Important Notice

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