HCPL-810J
PLC Powerline DAA IC

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-810J is a galvanically isolated Powerline Data Access Arrangement IC. It provides the key features of isolation, Tx line driver and Rx amplifier as required in a powerline modem application.

Used together with a simple LC coupling circuit, the HCPL-810J offers a highly integrated, cost effective Analogue Front End (AFE) solution. Optical coupling technology provides very high isolation mode rejection, facilitating excellent EMI and EMC performance. Application robustness is enhanced by the inherent properties of opto-isolation devices, to effectively block the transfer of damaging surge transients.

Excellent transmitter performance is achieved with the use of a high efficiency, low distortion line driver stage. Transmitter robustness is further enhanced with integrated load detection and over-temperature protection functions.

The HCPL-810J is designed to work with various transceiver ICs and significantly simplify the implementation of a powerline modem.

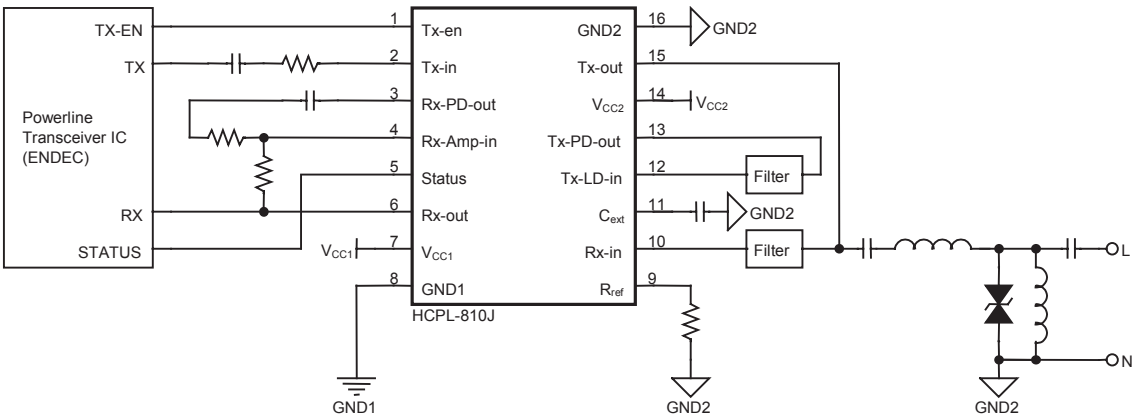
Features

- Highly Efficient Tx Line Driver
- Built-in Rx Amplifier
- Load Detection Function
- Under-Voltage Detection
- Over-Temperature Shutdown
- Temperature Range: -40°C to +85°C
- Regulatory Approvals (pending): UL, CSA, IEC/EN/DIN EN 60747-5-2

Applications

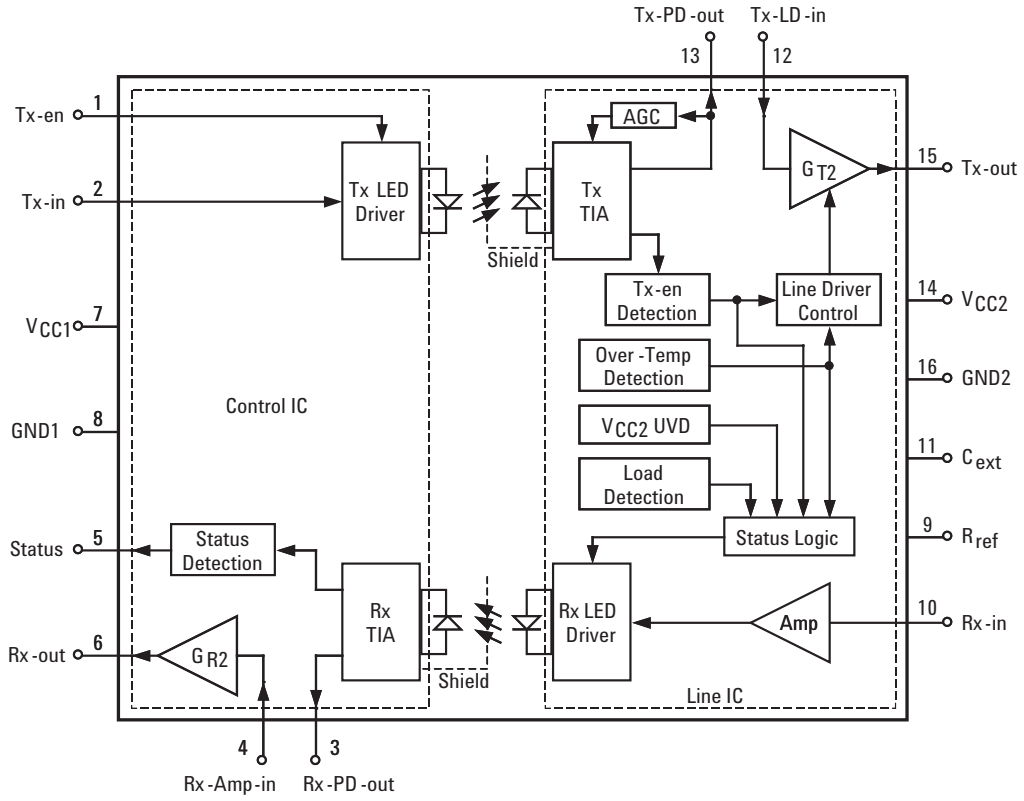
- Automatic Meter Reading (AMR)
- Powerline Modem
- Home Automation/Control
- Security and Surveillance
- General Purpose Isolated Transceiver
- Internet Appliances

Connection Diagram

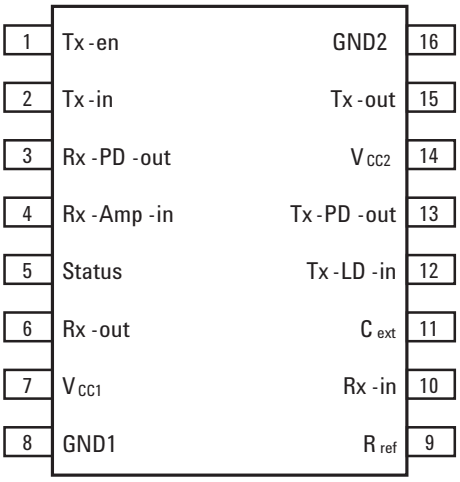


CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Block Diagram



Pin Descriptions



Package Pin Out

Pin No.	Symbol	Description
1	Tx-en	Transmit Enable Input
2	Tx-in	Transmit Input Signal
3	Rx-PD-out	Rx Photodetector Output
4	Rx-Amp-in	Receiver Output Amplifier Input
5	Status	Signal indicating Line Condition
6	Rx-out	Receiving Signal Output
7	V_{CC1}	5 V Power Supply
8	GND1	V_{CC1} Power Supply Ground
9	R_{ref}	Sets Line Driver biasing current, typically 24 kΩ
10	Rx-in	Receiving Signal Input from Powerline
11	C_{ext}	External Capacitor
12	Tx-LD-in	Tx Line Driver Input
13	Tx-PD-out	Tx Photodetector Output
14	V_{CC2}	5 V Power Supply
15	Tx-out	Transmit Signal Output to Powerline
16	GND2	V_{CC2} Power Supply Ground

Ordering Information

Part number	Option: RoHS Compliant	Option: Non RoHS Compliant	Packaging	Surface Mount	Tape & Reel	Quantity
HCPL-810J	-000E	No option	SO-16	X		45 per tube
	-500E	-500	SO-16	X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-810J-500E to order product of SO-16 package in Tape and Reel packaging and RoHS compliant.

Example 2:

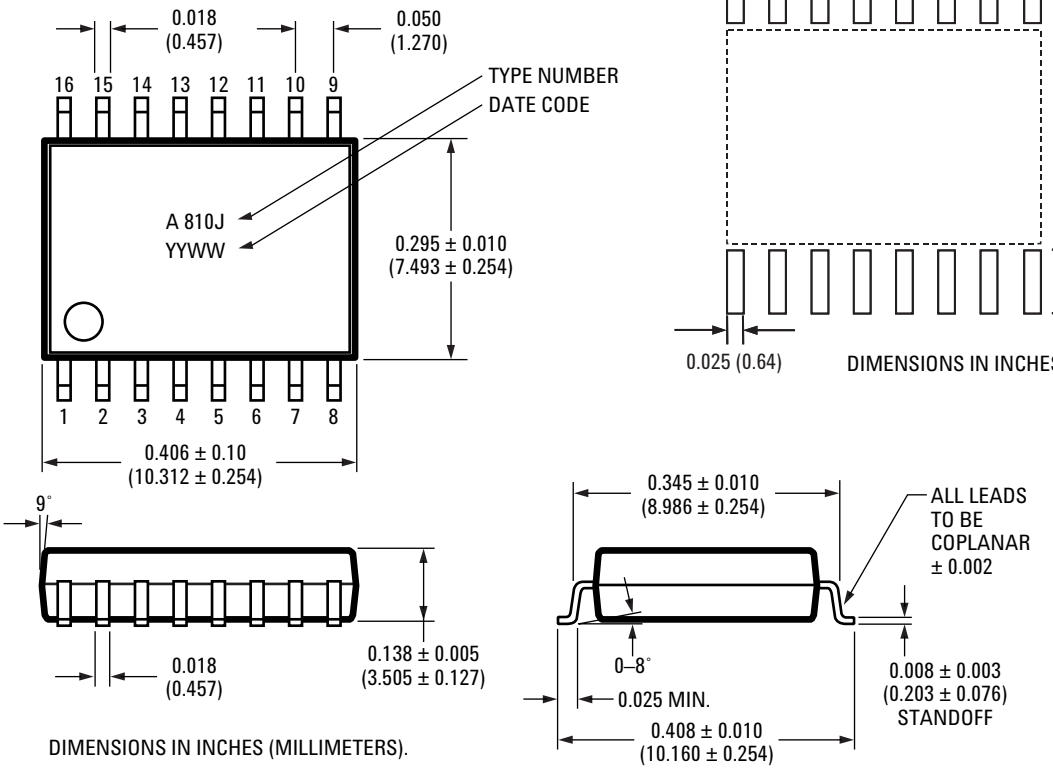
HCPL-810J-000E to order product of SO-16 package in Tube packaging and RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawings

16-Lead Surface Mount



Land Pattern Recommendation

NOTES:
1. INITIAL AND CONTINUED VARIATION IN THE COLOR OF THE HCPL-810J's WHITE MOLD COMPOUND IS NORMAL AND DOES NOT AFFECT DEVICE PERFORMANCE OR RELIABILITY.
2. FLOATING LEAD PROTRUSION IS 0.006 (0.15) MAX.

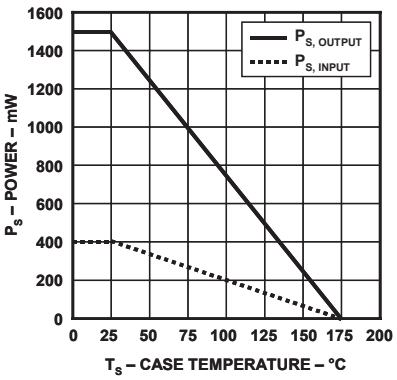
Package Characteristics

All specifications and figures are at the nominal (typical) operating conditions of V_{CC1} = 5 V, GND1 = 0 V, V_{CC2} = 5 V, GND2 = 0 V and T_A = +25°C.

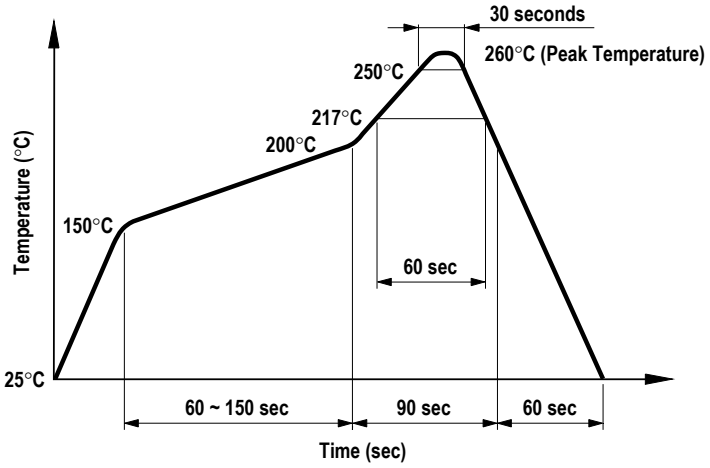
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Control IC - Line IC Momentary Withstand Voltage	V_{ISO}	3750			V_{rms}	RH< 50%, t = 1 min., T_A = 25°C	1, 2, 3
Resistance (Control IC - Line IC)	R_{I-O}		$>10^9$		Ω	V_{I-O} = 500 Vdc	3
Capacitance (Control IC – Line IC)	C_{I-O}		1.4		pF	f = 1 MHz	
Control IC to Ambient Thermal Resistance	θ_{IA}		83		°C/W	1 oz. trace, 2-layer PCB, Still air, T_A = 25°C	4
Line IC to Ambient Thermal Resistance	θ_{OA}		85				

Notes:

1. In accordance with UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 4500 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5\mu A$). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
2. The Control IC-Line IC Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as a Control IC-Line IC continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table.
3. Device is considered as a two terminal device: pins 1 - 8 shorted together and pins 9 - 16 shorted together.
4. Maximum power dissipation in Control side and Line side IC's needs to be limited to ensure that their respective junction temperature is less than 125°C. The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature. Details on the typical thermal impedances are given in the Package Characteristics. Further details on applying this to an actual application can be found in the Application Information section under Thermal Considerations.



Recommended Pb-free IR Profile



Note: Non-halide flux should be used.

Regulatory Information

The HCPL-810J is pending for approval by the following organizations:

IEC/EN/DIN EN 60747-5-2
Approved under:
IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
with VIORM = 891 Vpeak.

UL
Recognized under UL 1577,
component recognition program,
File E55361.

CSA
Approved under CSA
Acceptance Notice #5,
File CA 88324.

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (1)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
For rated mains voltage ≤ 150 Vrms	I – IV		
For rated mains voltage ≤ 300 Vrms	I – III		
For rated mains voltage ≤ 600 Vrms	I – II		
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{PEAK}
Input to Output Test Voltage, Method b (2) V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1670	V_{PEAK}
Input to Output Test Voltage, Method a (2) V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	1336	V_{PEAK}
Highest Allowable Over-voltage (2) (Transient Over-voltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-limiting values - maximum values allowed in the event of a failure			
Case Temperature	T_S	175	°C
Control Side Power (3)	$P_{S, INPUT}$	400	mW
Line Side Power (3)	$P_{S, OUTPUT}$	1500	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by protective circuits in application. Surface mount classification is class A in accordance with CECCOO802.
2. Refer to the optocoupler section of the Isolation and Control Component Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.
3. Refer to the following figure for dependence of $P_{S, INPUT}$ and $P_{S, OUTPUT}$ on case temperature.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Unit	Condition
Minimum External Air Gap (Clearance)	L(101)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance of conductor to conductor, usually the straight-line distance between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	°C	
Ambient Operating Temperature	T_A	-40	85	°C	
Junction Temperature	T_J		125	°C	
Supply Voltage 1	V_{CC1}	-0.5	5.5	V	
Supply Voltage 2	V_{CC2}	-0.5	5.5	V	
Transmit Output Voltage	$V_{Tx\text{-}out}$	-0.5	V_{CC2}	V	
Transmit Input Signal Voltage	$V_{Tx\text{-}in}$	-0.5	V_{CC1}	V	
Transmit Enable Voltage	$V_{Tx\text{-}en}$	-0.5	V_{CC1}	V	
Receiving Input Signal Voltage	$V_{Rx\text{-}in}$	-0.5	V_{CC2}	V	
Control-Side Power Dissipation	P_I		200	mW	1
Line-Side Power Dissipation	P_O		1000	mW	
Solder Reflow Temperature Profile	(See Solder Reflow Temperature Profile Section)				

Notes:
1. Maximum power dissipation in Control side and Line side IC's needs to be limited to ensure that their respective junction temperature is less than 125°C. The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature. Details on the typical thermal impedances are given in the Package Characteristics. Further details on applying this to an actual application can be found in the Application Information section under Thermal Considerations.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40		85	°C	
Input Supply Voltage	V_{CC1}	4.75	5	5.25	V	
Output Supply Voltage	V_{CC2}	4.75	5	5.25	V	
Tx-in Signal Current	$I_{Tx\text{-}in}$		250		μA_{PP}	1

Notes:
1. The transmitter input impedance is very low, this is meant for signal current input. Transmitter performance is optimized at 250 μA_{PP} input signal, an external series resistor with nominal value of 2 kΩ would be required if the input signal is 0.5 V_{PP}.

Electrical Specifications

Unless otherwise noted, for sinusoidal waveform input and reference resistor R_{ref} = 24 kΩ, all typical values are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

General

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Fig.	Note
V_{CC1} Supply Current	I_{CC1}		6	20	mA	$V_{Tx\text{-}en}$ = 0 V	1	
			20	35	mA	$V_{Tx\text{-}en}$ = 5 V	1	
V_{CC2} Supply Current	I_{CC2}		22	30	mA	$V_{Tx\text{-}en}$ = 0 V	2	
			40	70	mA	$V_{Tx\text{-}en}$ = 5 V	2, 3, 4	
Status Logic High Output	V_{OH}	V_{CC1} -1			V	I_{OH} = -4 mA		
Status Logic Low Output	V_{OL}			1	V	V_{CC2} = 3.5 V, I_{OL} = 4 mA		
V_{CC2} Under Voltage Detection	V_{UVD}	3.8	4	4.3	V			1
Junction Over-Temperature Threshold	T_{th}		130		°C			2
Load Detection Threshold			0.6		A_{PP}	$V_{Tx\text{-}en}$ = 5 V, f = 132 kHz	5, 13	
Isolation Mode Rejection Ratio	IMRR		80		dB	$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz	6, 14	3

Notes:
1. Threshold of falling V_{CC2} with hysteresis of 0.15 V (typ.).
2. Threshold of rising junction temperature with hysteresis of 15°C (typ.).
3. IMRR is defined as the ratio of the signal gain (measured at Rx-PD-out with signal applied to Rx-in) to the isolation mode gain (measured at Rx-PD-out with Rx-in connected to GND2 and the isolation mode voltage, V_{IM}, applied between GND1 and GND2), expressed in dB.

Electrical Specifications (Cont.)

Unless otherwise noted, for sinusoidal waveform input and reference resistor R_{ref} = 24 kΩ, all typical values are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Fig.	Note
Input Impedance	$Z_{I, Rx}$		4		kΩ	$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz		
Output Impedance (Rx-PD-out)	$Z_{O, RxPD}$		30		Ω	$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz		
Input Referred Noise	V_{nr}		70		$nV/\sqrt{Hz}$	$V_{Tx\text{-}en}$ = 0 V, $V_{Rx\text{-}in}$ = 0 VPP		
Bandwidth (Rx-PD-out)	BW_{RxPD}		500		kHz	$V_{Tx\text{-}en}$ = 0 V		
Gain	G_{R1}		20		dB	$V_{Tx\text{-}en}$ = 0 V, $V_{Rx\text{-}in}$ = 0.05 V_{PP}, f = 132 kHz	11	
Set-up Time (Rx-PD-out)	t_s, R_x		10		µs	$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz		
Receiver Output Amplifier (RxAMP)								
DC Biased Voltage	$V_{Bias, Rx}$		2.27		V			
Output Impedance	$Z_{O, RxA}$		20			$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz		
Gain Bandwidth Product	GBW_{RxA}		28		MHz	$V_{Tx\text{-}en}$ = 0 V, f = 132 kHz, $V_{Rx\text{-}in}$ = 0.1 V_{PP}, GR2 = -20, feedback resistor 20 kΩ	12	

Electrical Specifications (Cont.)

Unless otherwise noted, for sinusoidal waveform input and reference resistor R_{ref} = 24 kΩ, all typical values are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

Transmitter

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition	Fig.	Note
Transmit Enable Threshold Voltage	$V_{th, Tx-en}$	0.8		2.4	V			
Set-up Time (Tx-PD-out)	$t_{s, Tx}$		10		µs	V_{Tx-en} = 5 V, I_{Tx-in} = 250 $µA_{PP}$, f = 132 kHz, Tx-PD-out no load	15	1
AGC Settling Time	t_{AGC}		180		µs			2
Tx Photodetector Output Voltage (Tx-PD-out)		2.8	3.3	3.6	V_{PP}	V_{Tx-en} = 5 V, I_{Tx-in} = 250 $µA_{PP}$, f = 132 kHz, T_A = 25°C	7, 8, 9	
Bandwidth (Tx-PD-out)	BW_{TxPD}		1		MHz	V_{Tx-en} = 5 V, ITx-in = 250 $µA_{PP}$		
Tx Photodetector Output Impedance (Tx-PD-out)	$Z_{O, TxPD}$		1		Ω	V_{Tx-en} = 5 V, f = 132 kHz		
Line Driver (LD)								
Power Supply (V_{CC2}) Rejection Ratio	PSRR		55		dB	50 Hz ripple, V_{ripple} = 200 mV_{PP}		
Input Impedance	$Z_{I, LD}$		10		kΩ	V_{Tx-en} = 5 V, f = 132 kHz		
DC Biased Voltage	$V_{Bias, LD}$		2.27		V	V_{Tx-en} = 5 V		
Gain	G_{T2}	1.8	2	2.2	V/V	V_{Tx-en} = 5 V, f = 132 kHz, Tx-out no load, T_A = 25°C	10	
2nd Harmonic Distortion (Tx-out)	$HD2_{LD}$		-60		dB	V_{Tx-en}= 5 V, V_{Tx-out}= 3.6 VPP, f=132 kHz, Tx-out load 50Ω, T_A=25°C		
3rd Harmonic Distortion (Tx-out)	$HD3_{LD}$		-65		dB			
Output Impedance (Tx-out)	$Z_{O, LD}$		0.5		Ω	V_{Tx-en} = 5 V, f = 132 kHz		
			7.5		kΩ	V_{Tx-en} = 0 V, f = 132 kHz		
Short-Circuit Output Current	I_{OS}		2		A_{PP}	V_{Tx-en} = 5 V, $V_{Tx-LD-in}$ = 1.8 V_{PP}, f = 132 kHz, $t_P \leq$ 50 µs		3, 4

Notes:
1. Time from transmit is enabled (V_{Tx-en} is set to logic high) until output (Tx-PD-out) is available. See Figure 18 in the Application Information section.
2. Time from output (Tx-PD-out) is available until Tx-PD-out signal reaches 66% of its steady state level. See Figure 18 in the Application Information section.
3. To keep the junction temperature as close to the ambient temperature as possible, pulse testing method is used. The device is transmit-enabled within the pulse duration time, t_P. Thermal effects must be considered separately.
4. Maximum power dissipation in Control side and Line side IC's needs to be limited to ensure that their respective junction temperature is less than 125°C. The maximum permissible power dissipation is dependent on the thermal impedance and the ambient temperature. Details on the typical thermal impedances are given in the Package Characteristics. Further details on applying this to an actual application can be found in the Application Information section under Thermal Considerations.

Typical Performance Plots

Unless otherwise noted, all typical plots are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V, sinusoidal waveform input, signal frequency f = 132 kHz, $I_{Tx\text{-}in}$ = 250 μA_{PP}, and R_{ref} = 24 kΩ.

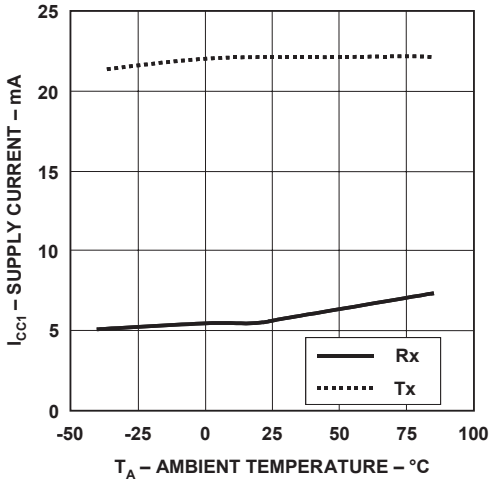


Figure 1. V_{CC1} supply current vs. temperature.

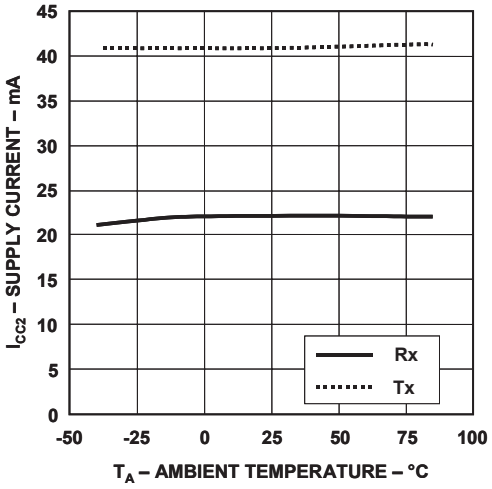


Figure 2. V_{CC2} supply current vs. temperature.

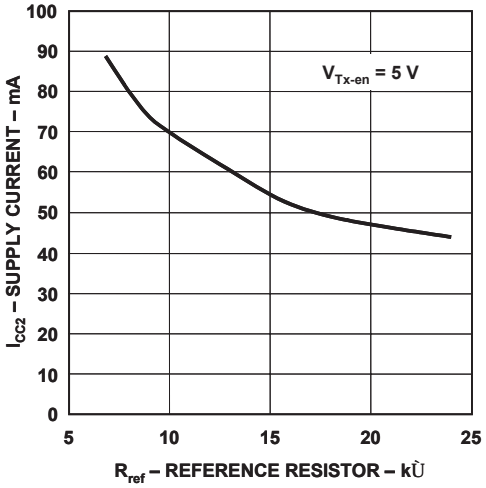


Figure 3. V_{CC2} supply current vs. reference resistor.

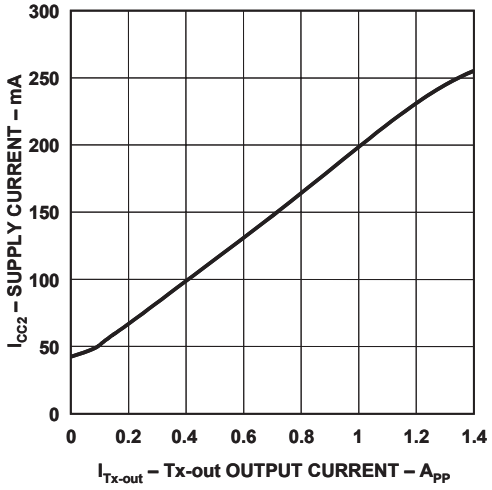


Figure 4. V_{CC2} supply current vs. Tx output current.

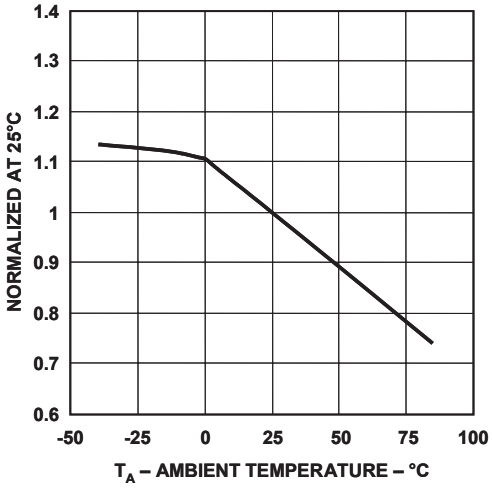


Figure 5. Normalized load detection threshold vs. temperature.

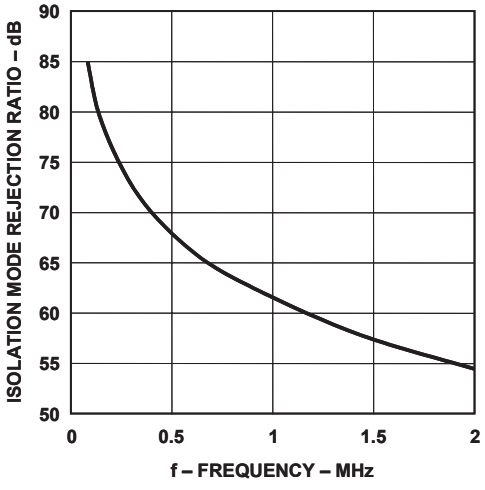


Figure 6. Isolation mode rejection ratio vs. frequency.

Typical Performance Plots (Cont.)

Unless otherwise noted, all typical plots are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V, sinusoidal waveform input, signal frequency f = 132 kHz, $I_{Tx\text{-}in}$ = 250 μA_{PP}, and Rref = 24 kΩ.

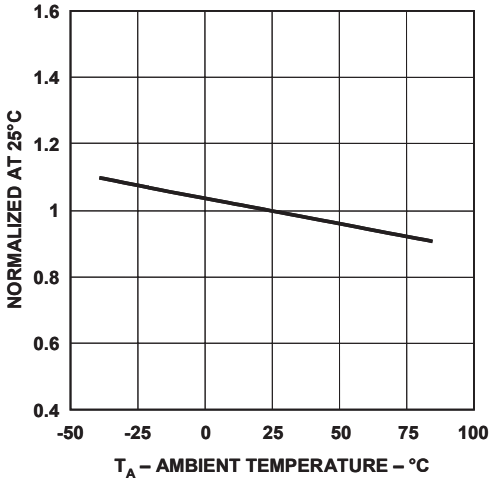


Figure 7. Normalized Tx-PD-out output voltage vs. temperature.

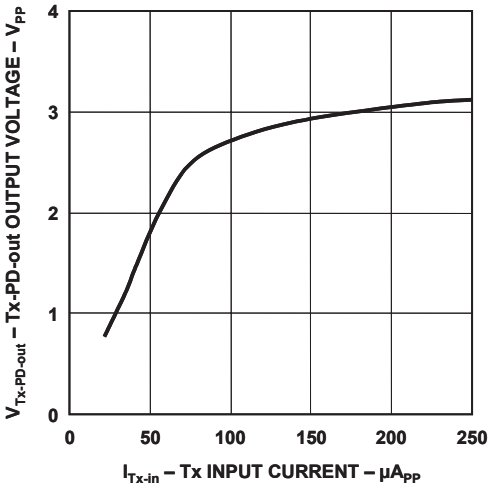


Figure 8. Tx-PD-out output voltage vs. Tx-in input current.

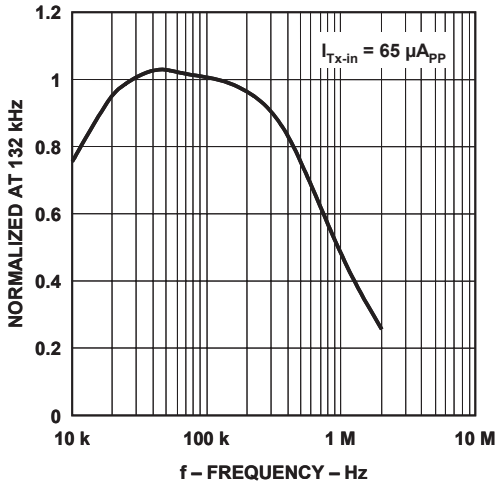


Figure 9. Normalized Tx-PD-out output voltage vs. frequency.

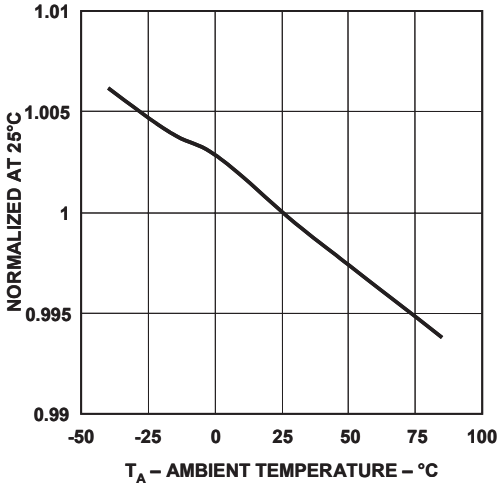


Figure 10. Normalized line driver gain vs. temperature.

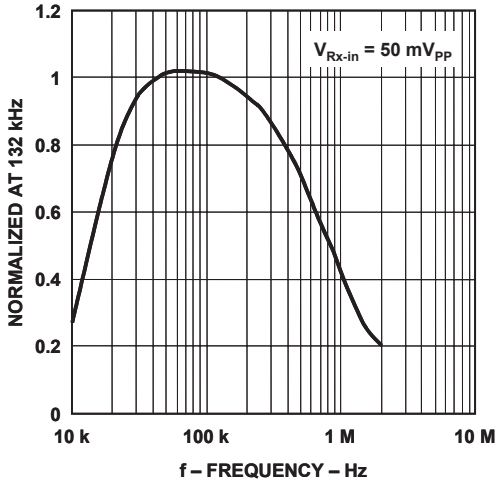


Figure 11. Normalized Rx-PD-out output voltage vs. frequency.

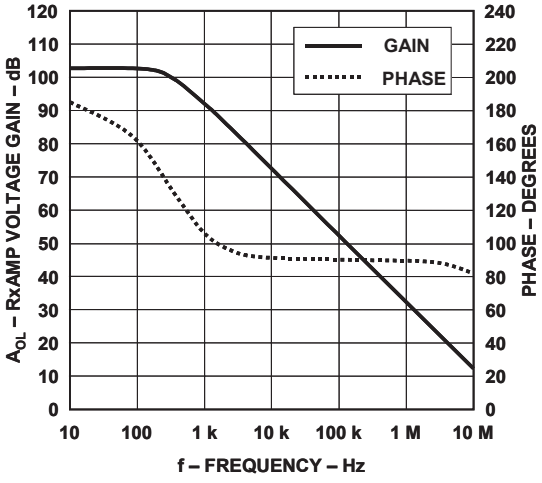


Figure 12. RxAMP gain and phase vs. frequency.

Test Circuit Diagrams

Unless otherwise noted, all test circuits are at T_A = 25°C, V_{CC1} = 5 V, V_{CC2} = 5 V, sinusoidal waveform input, and signal frequency f = 132 kHz.

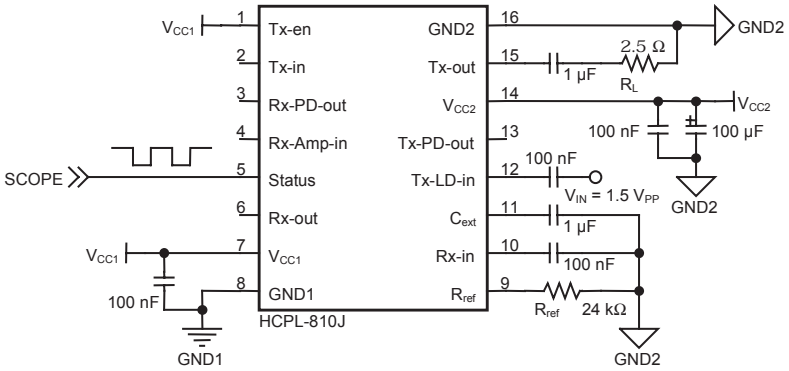


Figure 13. Load detection test circuit.

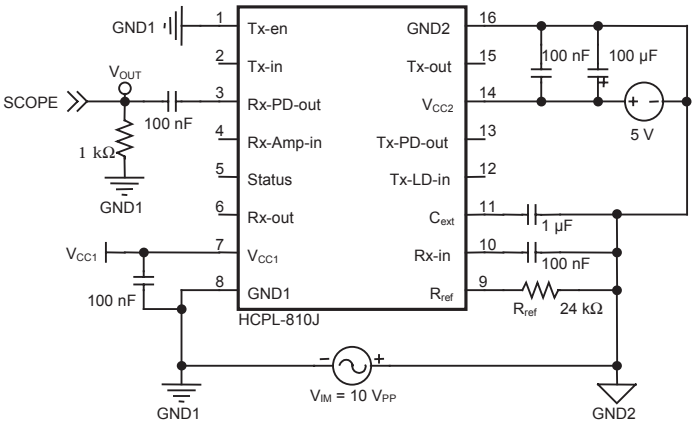


Figure 14. Isolation mode rejection ratio test circuit.

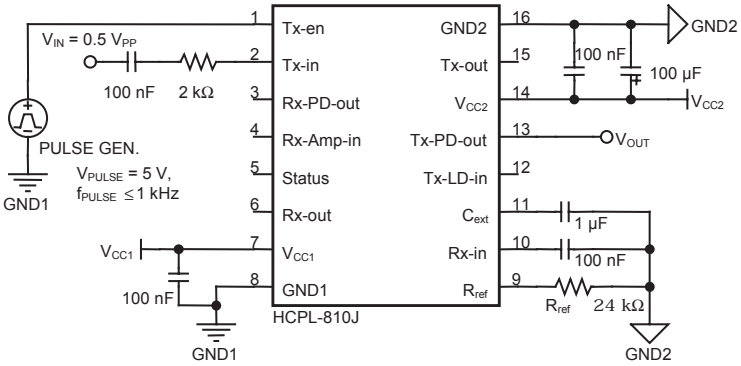


Figure 15. Tx-PD-out enable/disable time test circuit.

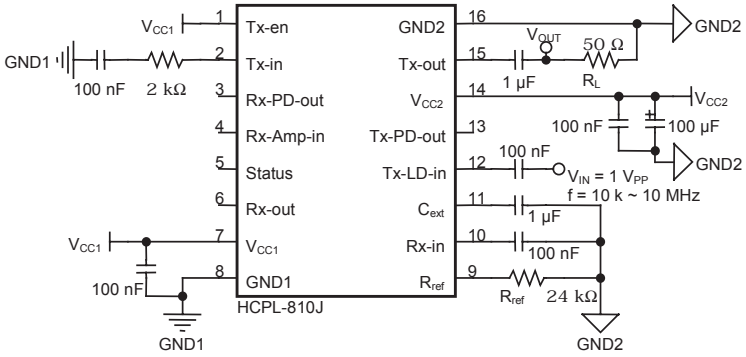


Figure 16. Line driver bandwidth test circuit.

Applications Information

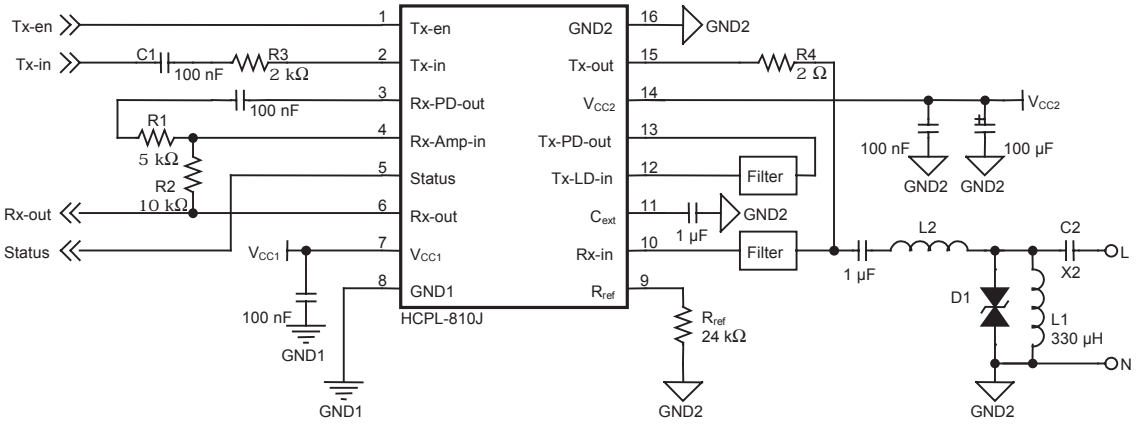


Figure 17. Schematic of HCPL-810J application for FSK modulation scheme.

Typical application for FSK modulation scheme

The HCPL-810J is designed to work with various transceivers and can be used with a variety of modulation methods including ASK, FSK and BPSK. Figure 17 shows a typical application in a powerline modem using Frequency Shift Keying (FSK) modulation scheme.

Transmitter

The analogue Tx input pin is connected to the modulator via an external coupling capacitor C1 and a series resistor R3 (see Figure 17). Optimal performance is obtained with an input signal of 250 μA_{PP}. E.g., for a modulator with an output signal of 0.5 VPP using a coupling capacitor of 100 nF, the optimal series resistor R3 would be 2 kΩ.

Tx AGC

To ensure a stable and constant output voltage at Tx-PD-out, the HCPL-810J includes an Automatic Gain Control (AGC) circuit in the isolated transmit signal path.

This AGC circuit compensates for variations in the input signal level presented at Tx-in and variations in the optical channel over temperature and time. The Tx-PD-out output signal is effectively stabilized for input Tx-in signals of between 150 μA_{PP} and 250 μA_{PP} (see Figure 8). The AGC circuit starts to function 10 µs after the Tx-en signal is set to logic high. After a period of 180 µs the Tx-PD-out signal typically reaches 66% of its steady state level (see Figure 18). To ensure correct operation of the internal circuitry, an external 1 µF capacitor needs to be connected from pin 11 to GND2.

The optical signal coupling technology used in the HCPL-810J transmit path achieves very good harmonic distortion, which is usually significantly better than the distortion performance of the modulated input signal. However to meet the requirements of some international EMC regulations it is often necessary to filter the modulated input signal. The optimal position for such a filter is between pins 13 and 12 as shown in Figure 17. A possible band-pass filter topology is shown in Figure 19, some typical values of the components in this filter are listed in Table 1.

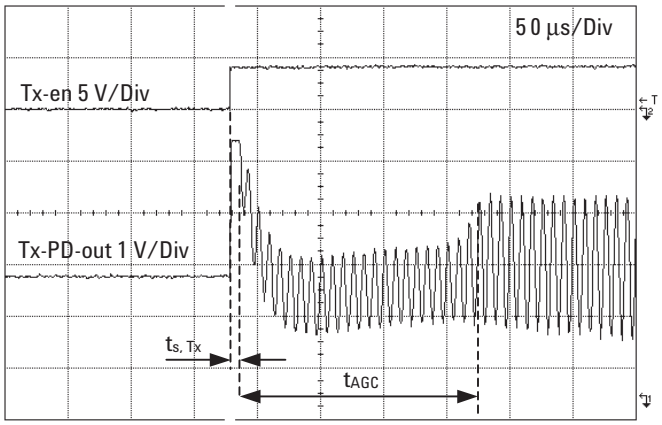


Figure 18. Tx-PD-out AGC response time.

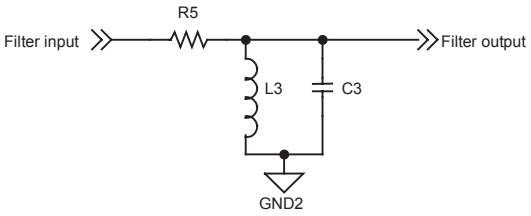


Figure 19. An example of a band-pass filter for transmit.

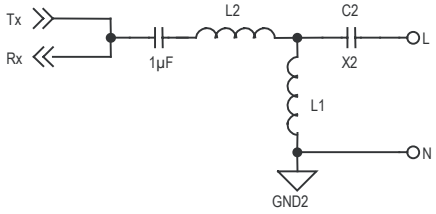


Figure 20. LC coupling network.

To compensate for the attenuation in the filter, the line driver stage has 6 dB gain. To prevent the line driver output from saturating, it is therefore important to achieve 6 dB of attenuation between Tx?PD?out (pin 13) and Tx?LD?in (pin 12) either by the inherent filter attenuation or by other means.

Transmitter Line Driver

The line driver is capable of driving powerline load impedances with output signals up to 4 VPP. The internal biasing of the line driver is controlled externally via a resistor Rref connected from pin 9 to GND2. The optimum biasing point value for modulation frequencies up to 150 kHz is 24 kΩ. For higher frequency operation with certain modulation schemes, it may be necessary to reduce the resistor value to enable compliance with international regulations.

The output of the line driver is coupled onto the powerline using a simple LC coupling circuit as shown in Figure 20. Refer to Table 1 for some typical component values. Capacitor C2 and inductor L1 attenuate the 50/60 Hz powerline transmission frequency. A suitable value for L1 can range in value from 200 µH to 1 mH. To reduce the series coupling impedance at the modulation frequency, L2 is included to compensate the reactive impedance of C2. This inductor should be a low resistive type capable of meeting the peak current requirements. To meet many regulatory requirements, capacitor C2 needs to be an X2 type. Since these types of capacitors typically have a very wide tolerance range of 20%, it is recommended to use as low Q factor as possible for the L2/C2 combination. Using a high Q coupling circuit will result in a wide tolerance on the overall coupling impedance, causing potential communication difficulties with low powerline impedances. Occasionally with other circuit configurations, a high Q coupling arrangement is recommended, e.g., C2 less than 100 nF. In this case it is normally used as a compromise to filter out of band harmonics originating from the line driver. This is not required with the HCPL-810J.

Although the series coupling impedance is minimized to reduce insertion loss, it has to be sufficiently large to limit the peak current to the desired level in the worst expected powerline load condition. The peak output current is effectively limited by the total series coupling resistance, which is made up of the series resistance of L2, the series resistance of the fuse and any other resistive element connected in the coupling network.

To reduce power dissipation when not operating in transmit mode the line driver stage is shut down to a low power high impedance state by pulling the Tx-en input (pin 1) to logic low state. The high impedance condition helps minimize attenuation on received signals.

Receiver

The received signal from the powerline is often heavily attenuated and also includes high level out of band noise. Receiver performance can be improved by positioning a suitable filter prior to the Rx-in input (pin 10). To counter the inevitable attenuation on the powerline, the HCPL-810J receiver circuit includes a fixed 20 dB front-end gain stage. If desired, this fixed gain can be reduced to unity gain by inserting an impedance of 33 kΩ in the receiver signal path. It is however recommended to maintain the fixed gain of 20 dB at this position and reduce the overall signal gain elsewhere if required. This configuration will result in the best SNR and IMRR.

The optical isolated Rx signal appears at Rx-PD-out (pin 3). This signal is subsequently AC coupled to the final gain stage via a capacitor.

The final gain stage consists of an op-amp configured in an inverting configuration and DC biased at 2.27 V. The actual gain of this gain stage is user programmable with external resistors R1 and R2 as shown in Figure 17. The signal output at Rx-out (pin 6) is buffered and may be directly connected to the demodulator or ADC, using AC coupling if required.

Table 1. Typical component values for band-pass filter and LC coupling network.

Carrier Frequency (kHz)	Band-Pass Filter		LC Coupling	
	L3 (µH)	C3 (nF)	L2 (µH)	C2 (nF)
110	680	3.3	15	150
120	680	2.7	10	220
132	680	2.2	6.8	220
150	680	1.8	6.8	220

Internal Protection and Sensing

The HCPL-810J includes several sensing and protection functions to ensure robust operation under wide ranging environmental conditions.

The first feature is the VCC2 Under Voltage Detection (UVD). In the event of VCC2 dropping to a voltage less than 4 V, the output status pin is switched to a logic low state.

The next feature is the over-temperature shutdown. This particular feature protects the line driver stage from over-temperature stress. Should the IC junction temperature reach a level above 130°C, the line driver circuit is shut down, simultaneously the output of Status (pin 5) is pulled to the logic low state.

The final feature is load detection function. The powerline impedance is quite unpredictable and varies not just at different connection points but is also time variant. The HCPL-810J includes a current sense feature, which may be utilized to feedback information on the instantaneous powerline load condition. Should the peak current reach a level greater than 0.6 APP, the output of Status pin is pulled to a logic low state for the entire period the peak current exceeds -0.3 A, as shown in Figure 21. Using the period of the pulse together with the known coupling impedance, the actual powerline load can be calculated. Table 2 shows the logic output of the Status pin.

External Transient Voltage Protection

To protect the HCPL-810J from high voltage transients caused by power surges and disconnecting/connecting the modem, it is necessary to add an external 6.8 V bi-directional transient voltage protector (as component D1 shown in Figure 17).

Additional protection from powerline voltage surges can be achieved by adding an appropriate Metal Oxide Varistor (MOV) across the powerline terminals after the fuse.

VCC2 Power Supply Requirements

The recommended voltage regulator to supply VCC2 is a low cost 78L05 or equivalent. To minimize harmonic distortion, it is recommended to connect a tantalum decoupling capacitor of at least 10 °F together with a 100 nF ceramic capacitor in parallel. The capacitors should be positioned as close as possible to the supply input pin. The supply voltage for the regulator can be supplied from the system level power supply transformer (powerline side winding). Alternatively, the supply can be derived directly from the powerline via a simple low cost circuit as shown in Figure 22.

Table 2. Status pin logic output.

Mode	Normal	V_{CC2} < 4V	Over-Temperature	$I_{Tx\text{-}out}$ < -0.3 A
Receiver	High	Low	-	-
Transmitter	High	Low	Low	Low (pulsed)

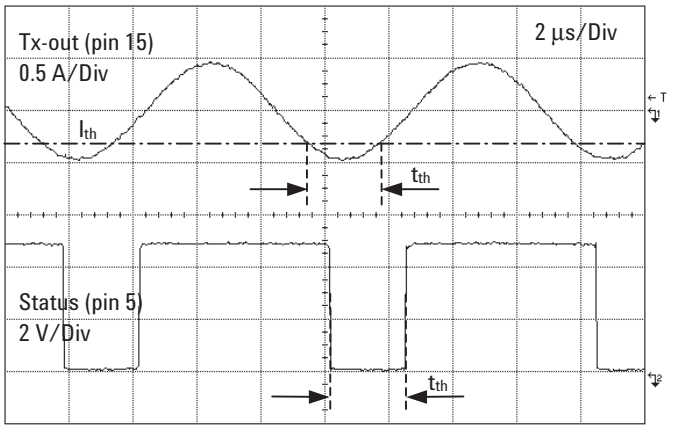


Figure 21. Transmit output load detection.

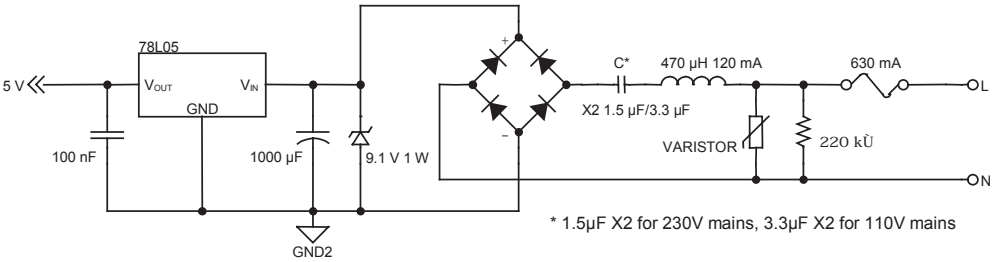


Figure 22. A simple low cost non-isolated power supply.

Thermal Considerations

The high efficiency line driver used in the HCPL-810J ensures minimum internal power dissipation, even for high peak output currents. Despite this, operating the line driver continuously with high output currents at elevated ambient temperatures can cause the peak junction temperature to exceed 125°C and/or resulting in the triggering of the thermal protection.

To prevent this from happening, when operating the line driver continuously with high output currents, an ambient temperature derating factor needs to be applied. A typical derating curve is shown in Figure 23.

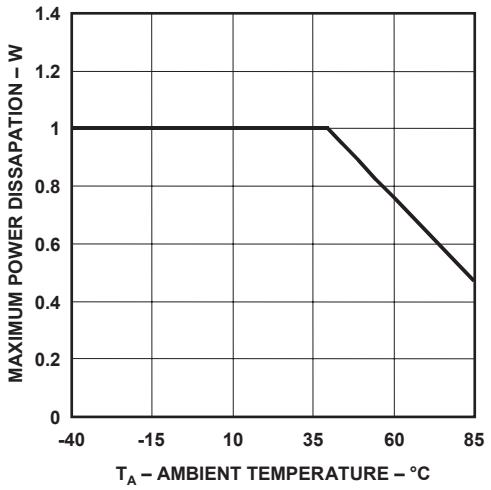


Figure 23. Power derating vs. temperature.

In this case the assumption is that the transmitter is operating continuously in still air with a typical 2-layer Printed-Circuit Board (PCB). However, it should be noted that operating the transmitter discontinuously for short periods of time will allow lower derating or even no derating at all. Conversely operating the line driver continuously with a poor PCB layout and/or with restricted air convection could result in the requirement for a larger derating factor.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0415EN - May 11, 2007