HEWLETT® PACKARD

High Speed CMOS Optocouplers

Technical Data

HCPL-7100
HCPL-7101

Features

- **1 µm CMOS IC Technology**
- **Compatibility with All +5 V CMOS and TTL Logic Families**
- **No External Components Required for Logic Interface**
- **High Speed: 15 MBd (HCPL-7100) and 50 MBd (HCPL-7101) Guaranteed**
- **Low Power Consumption**
- **Safety Approvals**
  UL 1577 (3750 Vac/1 Min)
  VDE 0884 (V_{IORM} = 848 V_{peak})
  CSA
- **3-State Output**
- **3750 Vac/1 Minute Dielectric Withstand**
- **High Common Mode Transient Immunity**

Applications

- **Multiplexed Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Instrument Input/Output Isolation**
- **Motor Control**
- **Power Inverter**

Description

The HCPL-7100/7101 optocoupler combines the latest CMOS IC technology, a new high-speed high-efficiency AlGaAs LED, and an optimized light coupling system to achieve outstanding performance with very low power consumption. It requires only two bypass capacitors for complete CMOS/TTL compatibility.

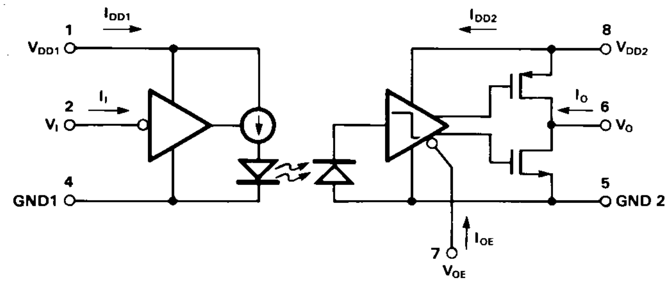
Basic building blocks of the HCPL-7100/7101 are a CMOS LED driver IC, an AlGaAs LED, and a CMOS detector IC. A CMOS or TTL logic input signal controls the LED driver IC which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high-speed trans-impedance amplifier and a voltage comparator with hysteresis. The 3-state output is CMOS and TTL compatible and is controlled by the output enable pin, V_{OE}.

The HCPL-7100/7101 consumes very little power, due to the CMOS IC technology and the light coupling system. The entire optocoupler typically uses only 10 mA of supply current, including the LED current.

World-wide safety approval and 3750 Vac/1 minute dielectric withstand is achieved with our patented "light-pipe" optocoupler packaging technology.

The HCPL-7100/7101 provides he user with an easy-to-use CMOS or TTL compatible optocoupler ideally suited for a variety of applications where high speed and low power consumption are desired.

Schematic



TRUTH TABLE
(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
H	H	Z
L	H	Z
H	L	H
L	L	L

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

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Ordering Information

HCPL-710x

- 0 = 15 MBd Minimum Data Rate
- 1 = 50 MBd Minimum Data Rate

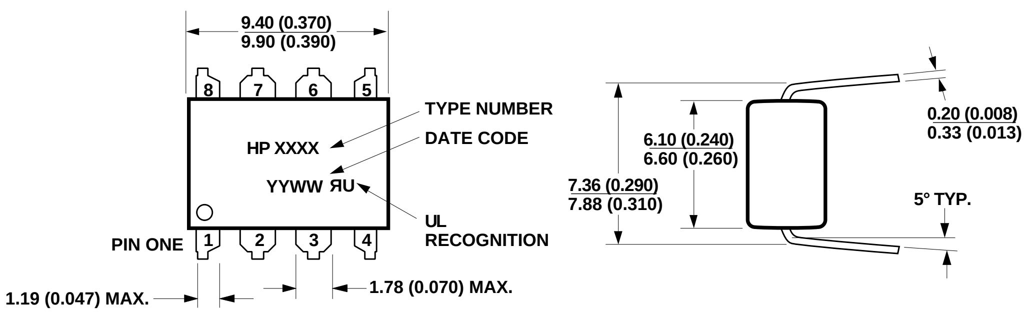
Option yyy

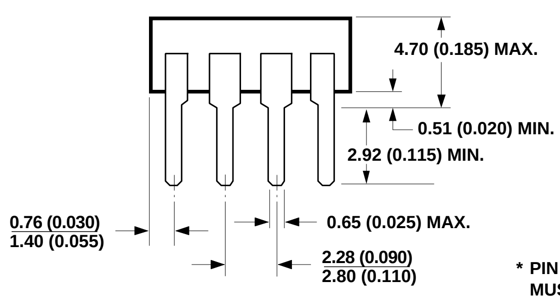
- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

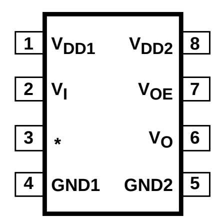
Option data sheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

Standard DIP Package







* PIN 3 IS THE ANODE OF THE INTERNAL LED AND MUST BE LEFT UNCONNECTED FOR GUARANTEED DATA SHEET PERFORMANCE.

DIMENSIONS IN MILLIMETERS AND (INCHES).

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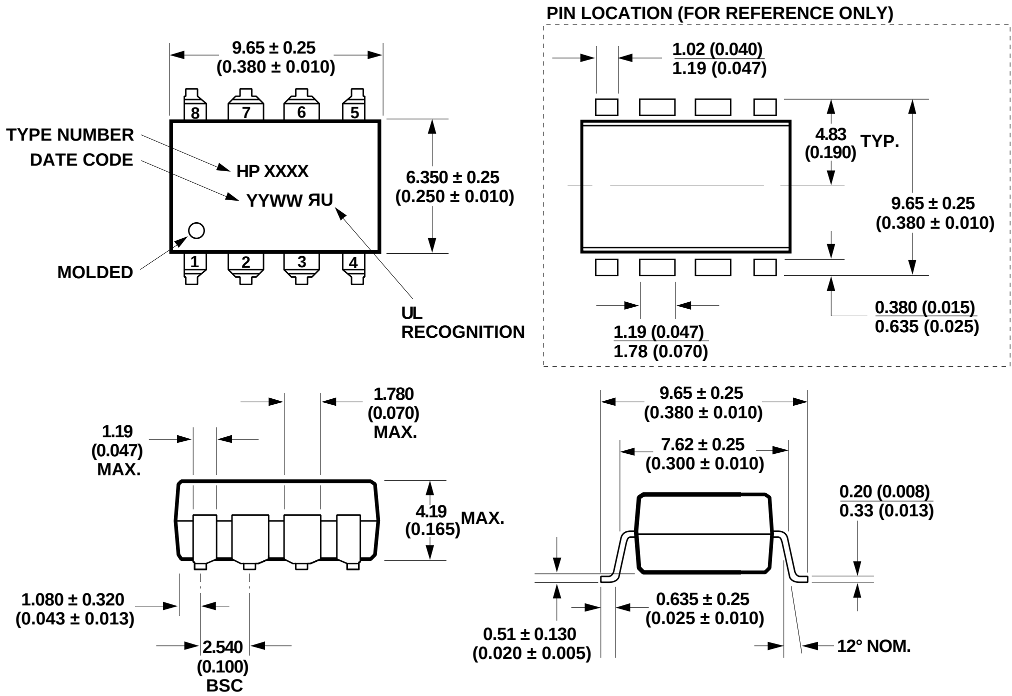
Gull Wing Surface Mount Option 300*

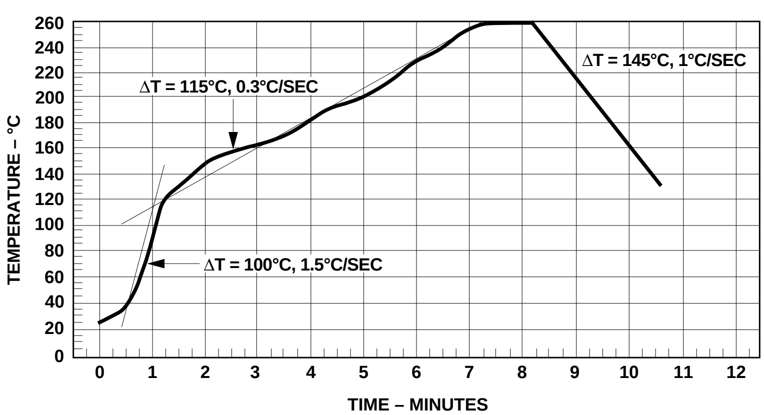


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

*Refer to Option 300 data sheet for more information.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

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Regulatory Information

The HCPL-7100/1 has been approved by the following organizations:

UL
Recognized under UL 1577, Component Recognition Program, File E55361.

CSA
Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE
Approved according to VDE 0884/06.92

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 PART 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/85/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** $V_{PR} = 1.875 \times V_{IORM}$, Production test with $t_p = 1$ sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** $V_{PR} = 1.5 \times V_{IORM}$, Type and sample test, $t_p = 60$ sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage, $t_{TR} = 10$ sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 15) Case Temperature Input Power Output Power	 T_S $P_{S,INPUT}$ $P_{S,OUTPUT}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, $V_{IO} = 500$ V	R_S	$\geq 1 \times 10^{12}$	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section in the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

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Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-55	125	°C
Ambient Operating Temperature	T_A	-40	85	°C
Supply Voltages	$V_{DD1,2}$	0.0	5.5	V
Input Voltage	V_I	-0.5	V_{DD1} + 0.5	V
Output Voltage	V_O	-0.5	V_{DD2} + 0.5	V
Output Enable Voltage	V_{OE}	-0.5	V_{DD2} + 0.5	V
Average Output Current	I_O		25	mA
Package Power Dissipation	P_{PD}		220	mW
Lead Solder Temperature (1.6 mm Below Seating Plane, 10 sec.)	T_{LS}		260	°C
Reflow Temperature Profile	See **Package Outline Drawings** Section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Operating Temperature	T_A	-40	85	°C	
Supply Voltages	$V_{DD1,2}$	4.5	5.5	V	
Logic High Input Voltage	V_{IH}	2.0	V_{DD1}	V	
Logic Low Input Voltage	V_{IL}	0.0	0.8	V	
Logic High Output Enable Voltage	V_{OEH}	2.0	V_{DD2}	V	Output in high impedance state
Logic Low Output Enable Voltage	V_{OEL}	0.0	0.8	V	Output enabled
Input Signal Rise and Fall Times	t_r, t_f		1	ms	
TTL Fanout	N		6		Standard Loads

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Electrical Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic Low Input Supply Current	I_{DD1L}		5.2	10.0	mA	V_{DD1} = 5.5 V V_I = V_{IL}		1
Logic High Input Supply Current	I_{DD1H}		0.3	0.6	mA	V_I = 4.5 V; V_{DD1} = 5.5 V		1
			0.9	1.6		V_I = 2.0 V		
Logic Low Output Supply Current	I_{DD2L}		5.0	9.0	mA	V_{DD2} = 5.5 V V_{OE} = V_{OEL} V_I = V_{IL}		
Logic High Output Supply Current	I_{DD2H}		5.2	9.0	mA	V_{DD2} = 5.5 V V_{OE} = V_{OEL} I_O = 0 mA V_I = V_{IH}		
Tri-State Output Supply Current	I_{DD2Z}		5.1	9.0	mA	V_{OE} = 4.5 V; V_{DD2} = 5.5 V		
			5.6	10.0		V_{OE} = 2.0 V		
Input Current	I_I	-1		1	µA	V_I = V_{DD1} or GND V_{DD1} = 5.5 V		
Output Enable Current	I_{OE}	-1		1	µA	V_{OE} = V_{DD2} or GND V_{DD2} = 5.5 V		
Logic High Output Voltage	V_{OH}	4.4	5.0		V	I_O = -20 µA; V_{DD2} = 4.5 V, V_I = V_{IH}, V_{OE} = V_{OEL}	6	
		4.0	4.8			I_O = -4.0 mA		
		3.7	4.7			I_O = -6.0 mA		
Logic High Output Current	I_{OH}	-7.5	-25		mA	V_{DD2} = 4.5 V V_O = 3.6 V V_I = V_{IH} V_{OE} = V_{OEL}	6	
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA; V_{DD2} = 4.5 V, V_I = V_{IL}, V_{OE} = V_{OEL}	5	
			0.1	0.3		I_O = 4.0 mA		
			0.15	0.4		I_O = 6.0 mA		
Logic Low Output Current	I_{OL}	10.5	23		mA	V_{DD2} = 4.5 V V_O = 0.6 V V_I = V_{IL} V_{OE} = V_{OEL}	5	
High Impedance State Output Current	I_{OZ}	-5		5	µA	V_{DD2} = 5.5 V V_{OE} = V_{OEH} V_O = V_{DD2} or GND		
Input Capacitance	C_I		4.3		pF	f = 1 MHz		4

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Switching Specifications

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output	t_{PHL}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		28	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Propagation Delay Time to Logic High Output	t_{PLH}	HCPL-7100			70	ns	C_L = 50 pF CMOS Signal Levels	7, 8	5, 6
		HCPL-7101		27	40				
		HCPL-7100			70	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			40				
Pulse Width Distortion $\|t_{PHL}-t_{PLH}\|$	PWD	HCPL-7100			20	ns	C_L = 50 pF CMOS Signal Levels	7, 9	6, 7
		HCPL-7101		2	6				
		HCPL-7100			20	ns	C_L = 15 pF TTL Signal Levels		
		HCPL-7101			6				
Data Rate		HCPL-7100	15			MBd	% PWD < 30%		8
		HCPL-7101	50	65					
Propagation Delay Skew	t_{PSK}	HCPL-7101			10	ns		10	9
Output Rise Time (10-90%)	t_R	HCPL-7100		12		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		10					
Output Fall Time (90-10%)	t_F	HCPL-7100		8		ns	C_L = 50 pF CMOS Signal Levels	7	
		HCPL-7101		7					
Random Jitter	RJ	HCPL-7101		50		ps rms	V_1 = 0-5 V square wave, f = 25 MHz, input rise/fall time = 5 ns. R_L = 10 kΩ, C_L = 5 pF. TTL Threshold Levels.		
Propagation Delay Time From Output Enabled to Logic High Output	t_{PZH}			13		ns	C_L = 50 pF CMOS Signal Levels	12	6
				12		ns	C_L = 15 pF TTL Signal Levels		
Propagation Delay Time From Output Enabled to Logic Low Output	t_{PZL}			11		ns	C_L = 50 pF CMOS Signal Levels	12	6
				10		ns	C_L = 15 pF TTL Signal Levels		

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Switching Specifications (cont.)

Guaranteed across recommended operating conditions. Test conditions represent worst case values for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at 25°C and 5 V supplies unless otherwise noted.

Parameter	Symbol	Device	Min.	Typ.	Max.	Unit	Test Conditions		Fig.	Note
Propagation Delay Time from Logic High to Output Disabled	t_{PHZ}			12		ns	C_L = 50 pF CMOS Signal Levels		12	6
				12		ns	C_L = 15 pF TTL Signal Levels			
Propagation Delay Time from Logic Low to Output Disabled	t_{PLZ}			9		ns	C_L = 50 pF CMOS Signal Levels		12	6
				11		ns	C_L = 15 pF TTL Signal Levels			
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$	HCPL-7100	1000			V/µs	V_{CM} = 50 V	$V_I = V_{IH}$ V_D > 3.2 V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V			
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$	HCPL-7100	1000			V/µs	V_{CM} = 50 V	$V_I = V_{IL}$ V_D < 0.8 V	13, 14	10
		HCPL-7101	2000				V_{CM} = 200 V			
Input Dynamic Power Dissipation Capacitance	C_{PD1}			68		pF				11
Output Dynamic Power Dissipation Capacitance	C_{PD2}			10		pF				11

Package Characteristics

Guaranteed across recommended operating conditions. Test conditions represent worst case value for the parameter under test. Test conditions that are not specified can be anywhere within their operating range. All typicals are at T_A = 25°C and 5 V supplies unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH < 50%, T_A = 25°C			2, 3
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C	V_{I-O} = 500 Vdc		2
		10^{11}				T_A = 100°C			
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz			2

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

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Notes:

1. The LED is OFF when the V_I is high and ON when V_I is low.
2. Device considered a two terminal device; pins 1-4 shorted together and pins 5-8 shorted together.
3. In accordance with UL 1577, for devices with minimum V_{ISO} specified at 3750 V rms, each optocoupler is proof-tested by applying an insulation test voltage greater than 4500 V rms for one second (leakage current detection limit $I_{I-O} < 5\ \mu A$). This test is performed before the method b, 100% production test for partial discharge shown in the VDE 0884 Insulation Characteristics Table.
4. C_I is the capacitance measured at pin 2 (V_I).
5. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the logic switching level of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the logic switching level of the V_O signal.
6. The logic switching levels are 1.5 V for TTL signals (0-3 V) and 2.5 V for CMOS signals (0-5 V).
7. PWD is defined as $|t_{PHL} - t_{PLH}|$. %PWD (percent pulse width distortion) is equal to PWD in ns divided by symbol duration (bit length) in ns.
8. Minimum data rate is calculated as follows: %PWD/PWD where %PWD is typically chosen by the design engineer (30% is common).
9. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at the same temperature, supply voltage, and output load within the recommended operating condition range.
10. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 3.2$ V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
11. Unloaded dynamic power dissipation is calculated as follows: $C_{PD} \bullet V_{DD}^2 \bullet f + I_{DD} \bullet V_{DD}$ where f is switching frequency in MHz.

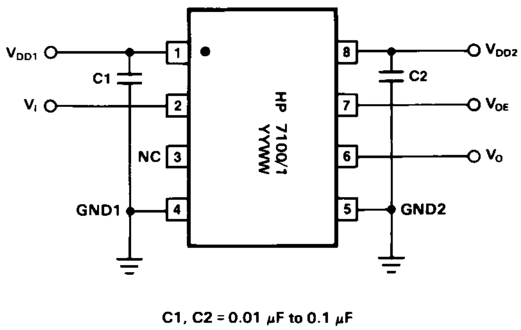

Figure 1. Recommended Application Circuit.

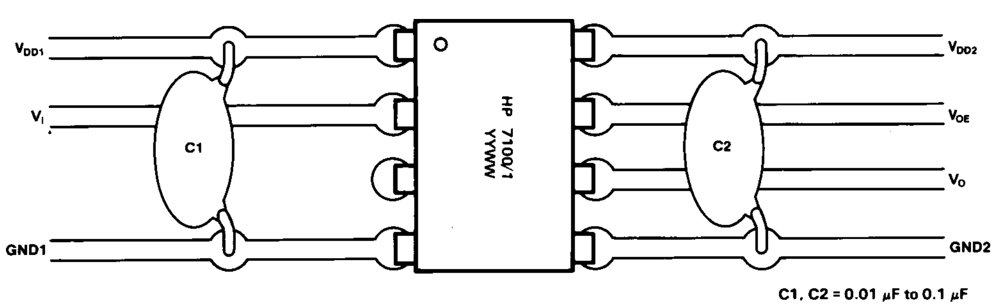

Figure 2. Recommended Printed Circuit Board Layout.

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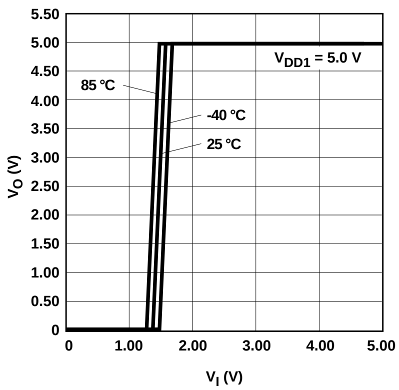

Figure 3. Typical Output Voltage vs. Input Voltage.

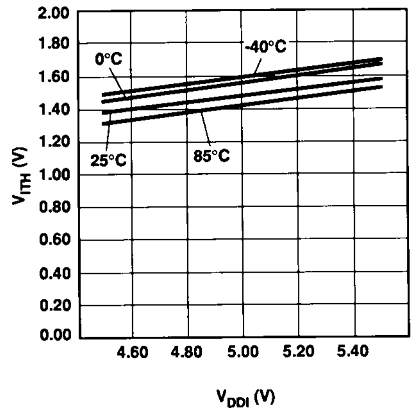

Figure 4. Typical Input Voltage Switching Threshold vs. Input Supply Voltage.

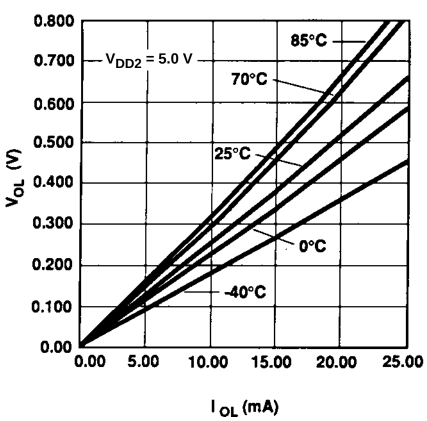

Figure 5. Typical Logic Low Output Voltage vs. Logic Low Output Current.

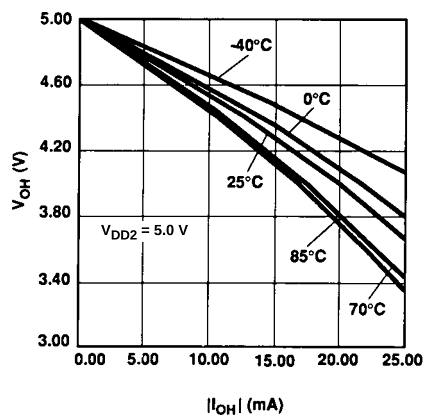

Figure 6. Typical Logic High Output Voltage vs. Logic High Output Current.

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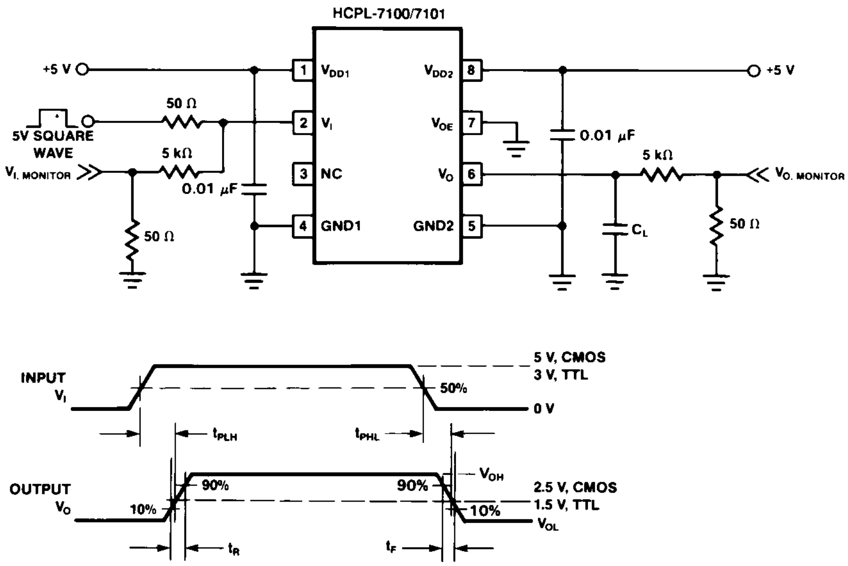

Figure 7. Test Circuit for Propagation Delay, Rise Time and Fall Time.

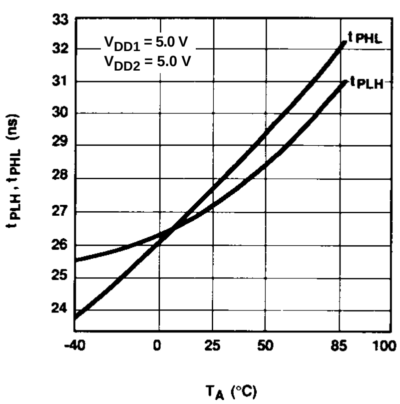

Figure 8. HCPL-7101 Typical Propagation Delay vs. Temperature.

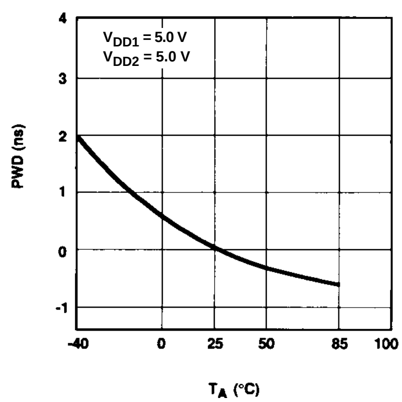

Figure 9. HCPL-7101 Typical Pulse Width Distortion vs. Temperature.

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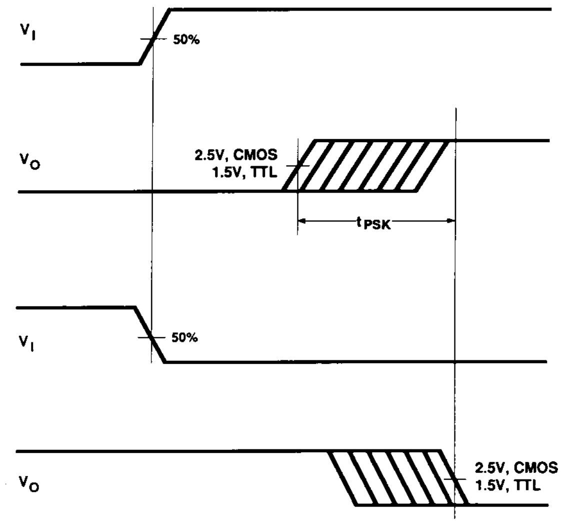

Figure 10. Propagation Delay Skew Waveform.

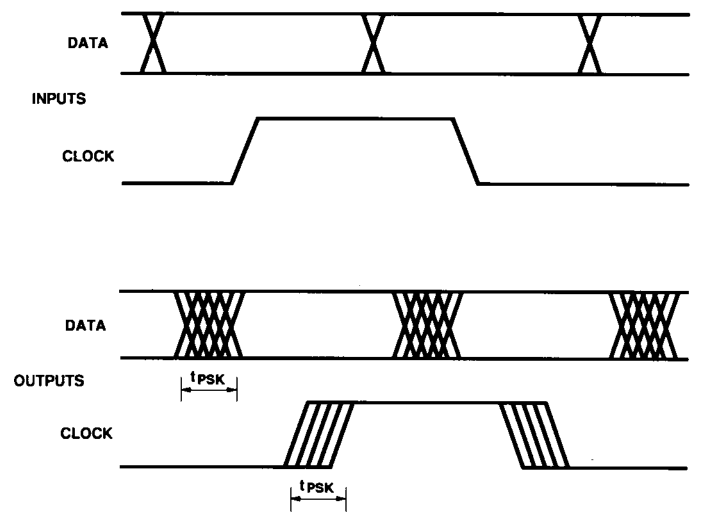

Figure 11. Parallel Data Transmission Example.

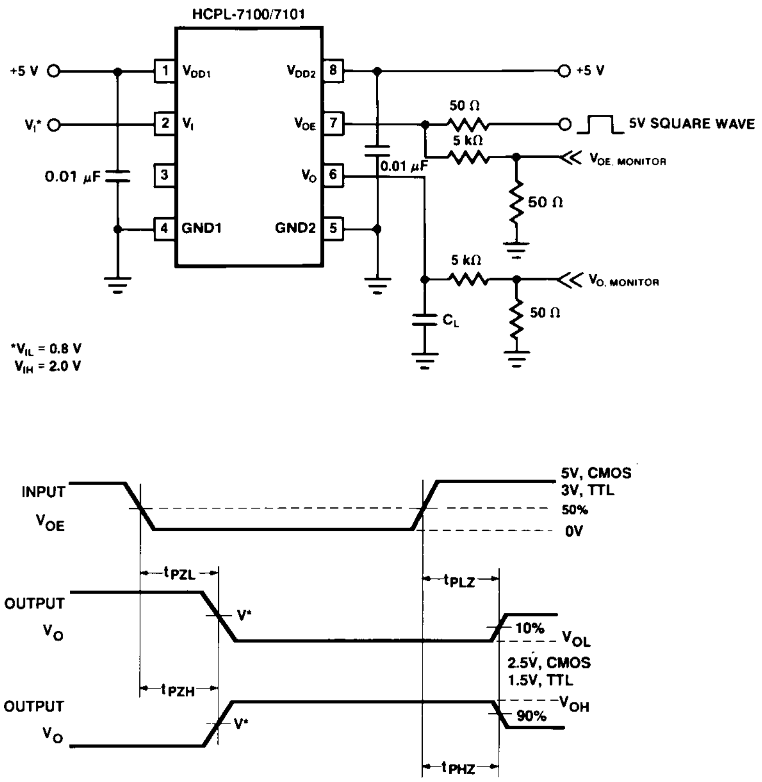

Figure 12. Test Circuit for 3-State Output Enable and Disable Propagation Delays.

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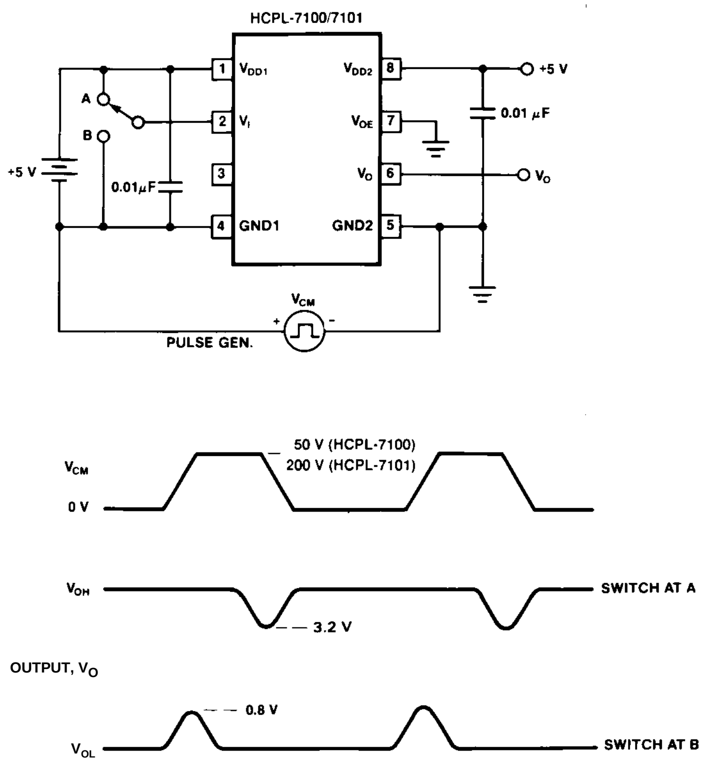

Figure 13. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

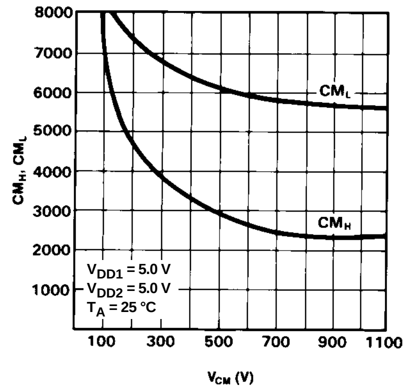

Figure 14. Typical Common Mode Transient Immunity vs. Common Mode Transient Voltage.

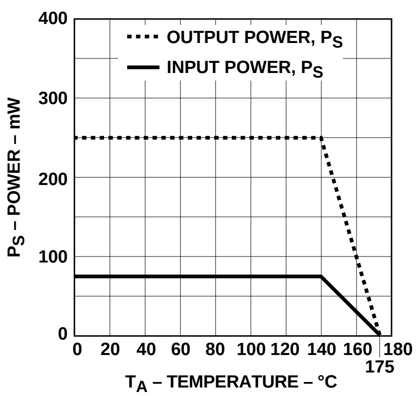

Figure 15. Dependence of Safety-Limiting Data on Ambient Temperature.

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HCPL-7100/7101 Application Information

The HCPL-7100/7101 is extremely easy to use. Because the optocoupler uses high-speed CMOS IC technology, the inputs and output are fully compatible with all +5 V TTL and CMOS logic. TTL or CMOS logic can be connected directly to the inputs and output; no external interface circuitry is required.

As shown in Figure 1, the only external components required for proper operation are two ceramic bypass capacitors. Capacitor values should be between 0.01 µF and 0.1 µF. For each capacitor, the total lead length between both ends of the capacitor and the power-supply pins should not exceed 20 mm. Figure 2 illustrates the recommended printed circuit board layout for the HCPL-7100/7101.

Propagation Delay, Pulse-Width Distortion, and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (see Figure 7).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-1, etc.).

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same supply voltage, output load, and operating temperature). As illustrated in Figure 10, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL}, and the longest propagation delay, either t_{PLH} or t_{PHL}.

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 11 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data; if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 11 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The HCPL-7101 optocoupler offers the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, and power supply ranges.

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