MK1573-03
GenClock™ HSYNC to Video Clock

Description

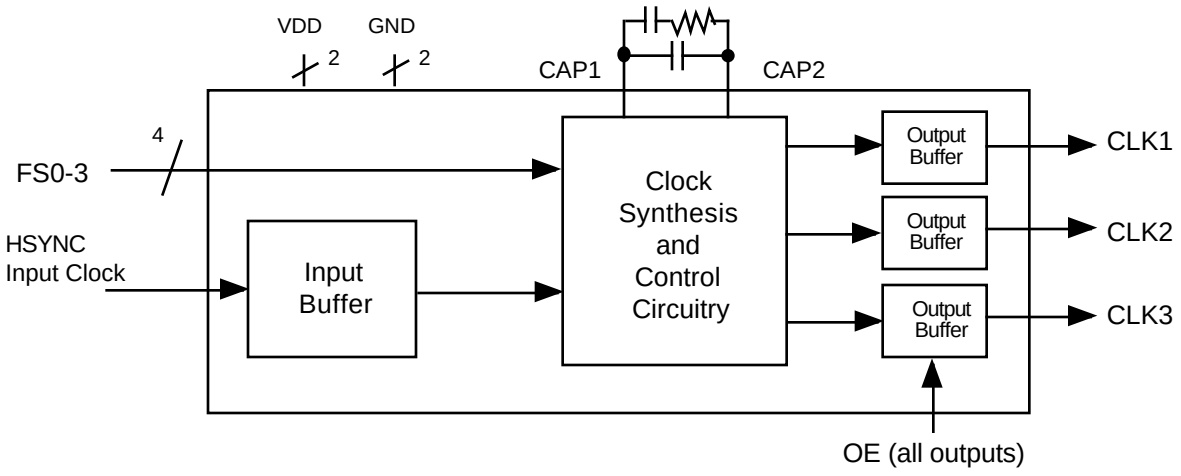
The MK1573 GenClock™ provides genlock timing for video overlay systems. The device accepts the horizontal sync (HSYNC) signal as the input reference clock, and generates a frequency-locked high speed output. Stored in the device are the multipliers for 16 combinations of popular frequencies for analog and digital TV and set-top box systems. Frequency-locked outputs include 1X, 4X, and 8X the subcarrier frequencies of NTSC and PAL systems, and 27MHz plus 13.5MHz for digital video systems. In most selections, the chip recovers the HSYNC clock by outputting a low jitter 50% duty cycle version of HSYNC. Also available is an inverted recovered HSYNC clock, and a double speed recovered HSYNC clock.

ICS can customize this device for any other different frequencies.

Features

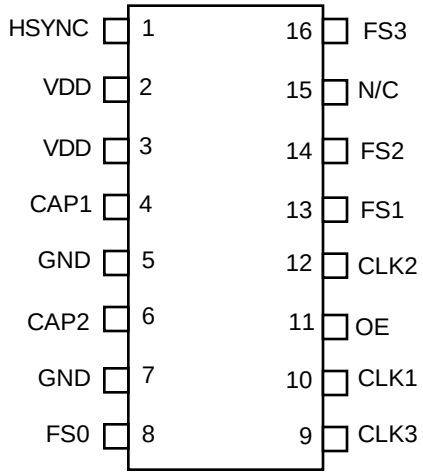
- Packaged in 16 pin narrow (150 mil) SOIC
- Exact ratios stored in the device eliminate the need for external dividers
- Accepts HSYNC of 15.625kHz or 15.73426kHz
- Highly accurate frequency generation within 1 ppm
- Generates NTSC/PAL subcarrier frequencies, and 4X and 8X of those frequencies
- Generates 27MHz and 13.5MHz
- 2X HSYNC clock available
- Recovered HSYNC clock available
- Inverted HSYNC clock available
- 3.3V operation

Block Diagram



Integrated Circuit Systems, Inc.• 525 Race Street • San Jose • CA • 95126 • (408)295-9800 • www.icst.com

Pin Assignment



16 pin (150 mil) SOIC

Output Clocks Decoding Table MK1573-03 (MHz)

Decode FS3:0	Address (Hex)	HSYNC pin 1	Multiplier On-chip	CLK 1 pin 10	CLK 2 pin 12	CLK 3 pin 9
0000	0	15.625k	2270	35.46875M	15.62k	31.25k
0001	1	15.734264k	1820	28.63636M	15.734264k	31.4685k
0010	2	15.625k	1728	27M	13.5M	15.625k
0011	3	15.734264k	1716	27M	13.5M	15.734264k
0100	4	15.625k	960	15M	7.5M	15.625k
0101	5	15.734264k	953 1/3	15M	7.5M	15.734264k
0110	6	15.625k	3840	60M	30M	15.625k
0111	7	15.734264k	3840	60.41957M	30.20979M	15.734264k
1000	8	15.625k	2270	35.46875M	17.734375M	4.433594M
1001	9	15.734264k	1820	28.63636M	14.31818M	3.579545M
1010	A	15.625k	2270	35.46875M	15.625k	15.625k
1011	B	15.734264k	1820	28.63636M	15.734264k	15.734264k
1100	C	15.625k	2048	32M	16M	15.625k
1101	D	15.734264k	808	12.71329M	15.734264k	31.4685k
1110	E	15.734264k	1218	19.164M	Off	Off
1111	F	15.625k	1260	19.6875M	Off	Off

- 0 = connect directly to ground, 1 = connect directly to VDD.
- CLK2 is a recovered HSYNC (with 50% duty cycle) on selections in italic.
- HSYNC reference outputs on CLK3 (in italic) are inverted, recovered HSYNC.

Pin Descriptions

Number	Name	Type	Description
1	HSYNC	I	HSYNC clock input. The output clocks are synchronized to the HSYNC falling edge.
2	VDD	P	Connect to +3.3V.
3	VDD	P	Connect to +3.3V.
4	CAP1	I	Connect a 0.047µF ceramic NP0 capacitor and a 22kΩ resistor in series and also a parallel .0022µF low leakage capacitor between this pin and CAP2.
5	GND	P	Connect to ground.
6	CAP2	I	Connect a 0.047µF ceramic NP0 capacitor and a 22kΩ resistor in series and also a parallel .0022µF low leakage capacitor between this pin and CAP1.
7	GND	P	Connect to ground.
8	FS0	I	Frequency Select 0. Determines CLK outputs (with given input) per table above.
9	CLK3	O	Clock 3 determined by status of FS3:0 per table above.
10	CLK1	O	Clock 1 determined by status of FS3:0 per table above.
11	OE	I	Output Enable. Tri-states the three output clocks when low.
12	CLK2	O	Clock 2 determined by status of FS3:0 per table above.
13	FS1	I	Frequency Select 1. Determines CLK outputs (with given input) per table above.
14	FS2	I	Frequency Select 2. Determines CLK outputs (with given input) per table above.
15	N/C	-	No connect. Nothing is connected to this pin.
16	FS3	I	Frequency Select 3. Determines CLK outputs (with given input) per table above.

Type: I = Input, O = output, P = power supply connection

External Components/Crystal Selection

The MK1573 requires a minimum number of external components for proper operation. A 0.047µF capacitor should be connected in series with a 22kΩ resistor between CAP1 and CAP2 pin (resistor on CAP2 side), with a parallel low leakage 0.0022µF capacitor between CAP1 and CAP2 pins. A decoupling capacitor of 0.1µF must be connected between VDD and GND pins (pins 2 and 3, 5 and 7) close to the chip, and 33Ω terminating resistors can be used on clock outputs with traces longer than 1 inch.

Electrical Specifications

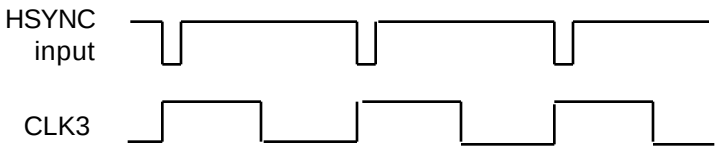
Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (Note 1)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs		-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	℃
Soldering Temperature	Max of 10 seconds			250	℃
Storage Temperature		-65		150	℃
DC CHARACTERISTICS (VDD = 3.3V unless noted)					
Operating Voltage, VDD		3.15		3.45	V
Input High Voltage, VIH		2			V
Input Low Voltage, VIL				0.8	V
Output High Voltage	IOH=-4mA	VDD-0.4			V
Output High Voltage	IOH=-25mA	2.4			V
Output Low Voltage	IOL=25mA			0.4	V
Operating Supply Current, IDD	No Load, VDD=5.0V		10		mA
Short Circuit Current	Each output		±100		mA
Input Capacitance			5		pF
Actual mean frequency error versus target, note 2	Any clock selection		0	1	ppm
AC CHARACTERISTICS (VDD = 3.3V unless noted)					
Input Frequency, NTSC			15.734264		kHz
Input Frequency, PAL			15.625		kHz
Output Clock Rise Time	0.8 to 2.0V		0.7	1.5	ns
Output Clock Fall Time	2.0 to 0.8V		0.7	1.5	ns
Output Clock Duty Cycle, High Time	At VDD/2	40	49 to 51	60	%
Absolute Clock Period Jitter, MHz outputs			±200		ps
Absolute Clock Period Jitter, kHz outputs			±1.5		ns
Output Enable Time, OE high to outputs on				50	ns
Output Disable Time, OE low to tri-state				3	µs

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.
2. Most selections have zero ppm error. Some selections have a maximum of 1 ppm synthesis error.

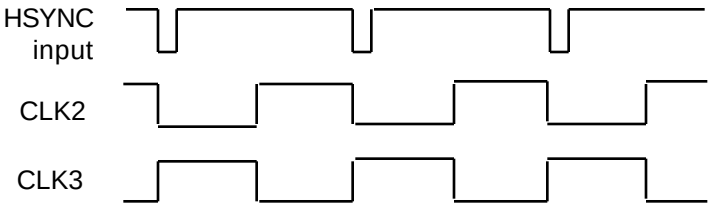
Clock Waveforms

In addition to generating the video clock on CLK1 (pin 10), the MK1573 also outputs the recovered HSYNC clocks. On certain selections, a double speed recovered HSYNC clock is also available. These recovered clocks will have lower jitter than the HSYNC input due to the filtering action of the PLL. The jitter spectrum of the recovered clocks will be reduced at frequencies higher than the loop bandwidth. The waveforms of the recovered clocks fall into one of three different groups depending on the address selection:

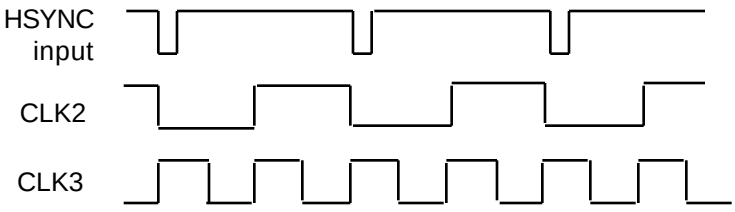
Addresses 2 to 7 and C



Addresses A and B

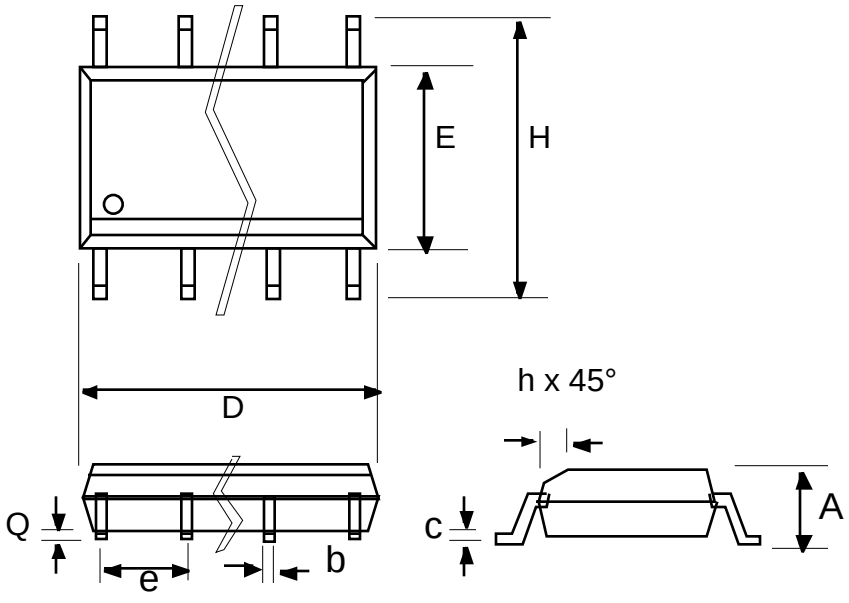


Addresses D, E, and F



The recovered clocks are triggered by the falling edge of HSYNC and are delayed by about 100ns.

Package Outline and Package Dimensions



16 pin SOIC narrow

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.070	1.397	1.778
b	0.013	0.019	0.330	0.483
c	0.007	0.010	0.191	0.254
D	0.385	0.400	9.779	10.160
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.016		0.406
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
MK1573-03S	MK1573-03S	16 pin narrow SOIC	0-70°C
MK1573-03STR	MK1573-03S	Add Tape & Reel	0-70°C