

# DATA SHEET

## **SAA1310**

Control interface for VHS video recorders

Product specification  
File under Integrated Circuits, IC02

April 1995

## Control interface for VHS video recorders

# SAA1310

### FEATURES

- Full support of VISS and VASS mode (VHS Index/Address Search System)
- Read, write and overwrite of Tape Control/head signal (CTL)
- Power-ON and power-failure indicator
- 4 general purpose comparators for interface between sensors and microprocessor
- 2 comparators have a 100 mA output driver
- PAL and NTSC compatible

### GENERAL DESCRIPTION

The SAA1310 provides an interface between the tape control head in the VHS deck-electronics.

The circuit also includes an interface between sensors in the deck mechanics and the microprocessor.

### ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA1310	18	DIL	plastic	SOT102 <sup>(1)</sup>
SAA1310T	20	SO	plastic	SOT163A <sup>(2)</sup>

### Note

1. SOT102-1; 1996 December 02.
2. SOT163-1; 1996 December 02.

Control interface for VHS video recorders

SAA1310

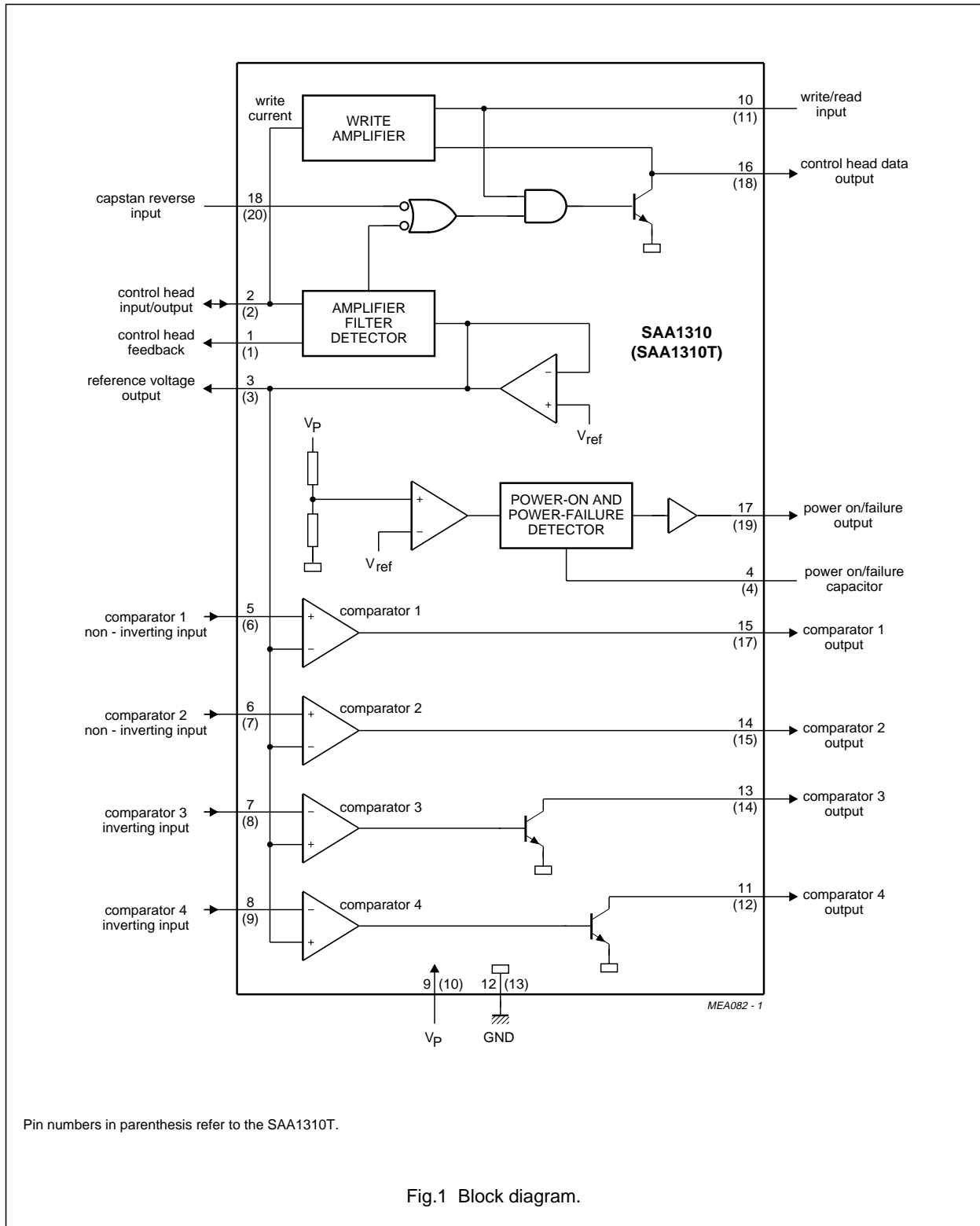
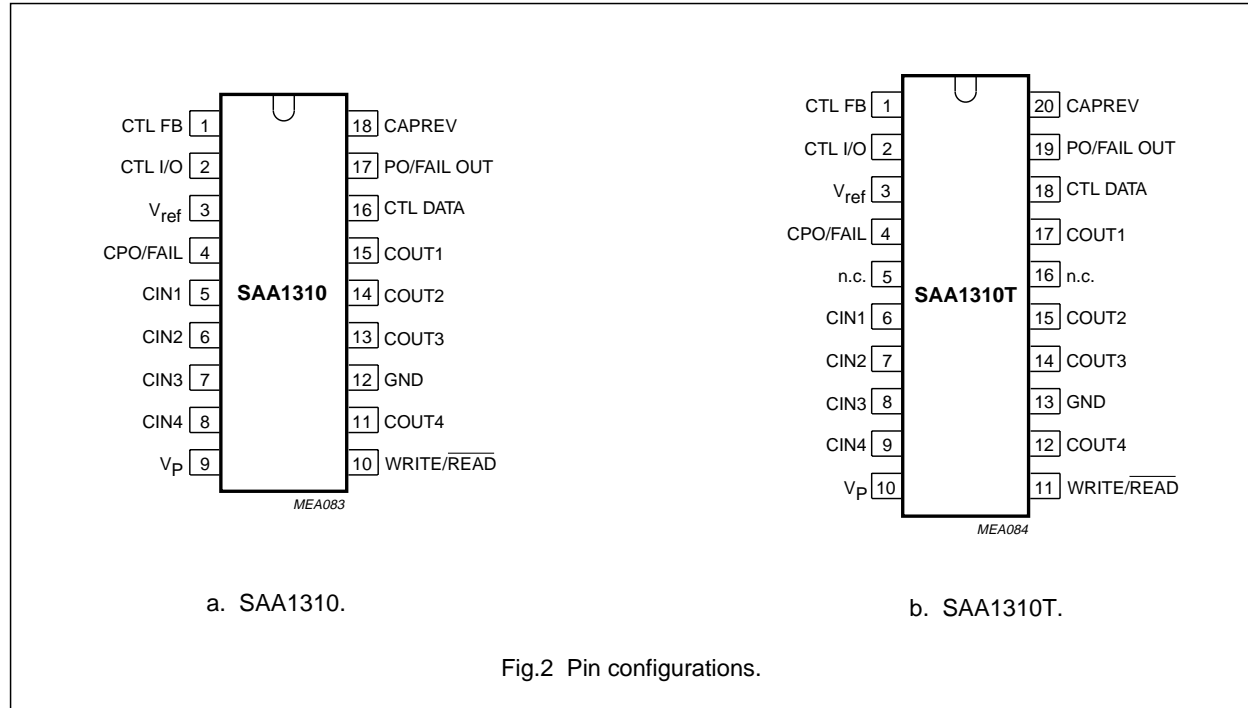


Fig.1 Block diagram.

## Control interface for VHS video recorders

## SAA1310

## PIN CONFIGURATION



## PINNING (pins in parenthesis refer to SAA1310T)

SYMBOL	PIN	DESCRIPTION
CTL FB	1 (1)	control head feedback
CTL I/O	2 (2)	control head input/output
V <sub>ref</sub>	3 (3)	reference voltage output
CPO/FAIL	4 (4)	power on/failure capacitor
CIN1	5 (6)	comparator 1 input
CIN2	6 (7)	comparator 2 input
CIN3	7 (8)	comparator 3 input
CIN4	8 (9)	comparator 4 input
V <sub>p</sub>	9 (10)	supply voltage
WRITE/ $\overline{\text{READ}}$	10 (11)	write/read input
COU4	11 (12)	comparator 4 output
GND	12 (13)	ground
COU3	13 (14)	comparator 3 output
COU2	14 (15)	comparator 2 output
COU1	15 (17)	comparator 1 input
CTL DATA	16 (18)	control head data output
PO/FAIL OUT	17 (19)	power on/failure output
CAPREV	18 (20)	capstan reverse input

## Control interface for VHS video recorders

SAA1310

**LIMITING VALUES (PIN NUMBERS IN PARENTHESIS REFER TO SAA1310T)**

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_P$	supply voltage range		0	6.0	V
$V_I/V_O$	voltage on all pins	except pins 11 (12) and 13 (14)	0	$V_P$	V
$V_O$	output voltage on pins 11 (12) and 13 (14)		0	18	V
$T_{stg}$	storage temperature range		-65	+150	°C
$T_{amb}$	ambient temperature range		0	+70	°C

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th}$	thermal resistance (SAA1310)	75	–	K/W
$R_{th}$	thermal resistance (SAA1310T)	90	–	K/W

## Control interface for VHS video recorders

## SAA1310

**CHARACTERISTICS (PIN NUMBERS IN PARENTHESIS REFER TO SAA1310T)**

$V_P = 5\text{ V}$ ;  $T_{\text{amb}} = 25\text{ °C}$ ; all voltage referenced to pin 12 (13); according to the test set-up (see Fig.4); unless otherwise specified

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$P_d$	power dissipation	note 1	–	85	–	mW
<b>Supply pin 9 (10)</b>						
$V_P$	supply voltage		4.5	5.0	5.5	V
$I_P$	supply current	read mode	10	15	20	mA
		write mode; duty factor = 50%	13	18	24	mA
<b>CTL I/O pin 2 (2)</b>						
READ MODE PIN 10 (11) < 0.5 V						
$V_i$	input voltage (peak-to-peak value)	f = 500 Hz	0.35	–	–	mV
		f = 30 kHz; non-linear operation	–	–	200	mV
B	bandwidth low-pass filter		–	3	–	kHz
$I_b$	input bias current	read mode	–	0.1	–	$\mu\text{A}$
WRITE MODE PIN 10 (11) > 3.5 V						
$V_O$	output voltage LOW	$I_{\text{CTL I/O}} = 3\text{ mA}$ ; pin CTL DATA = HIGH	–	–	0.4	V
$V_O$	output voltage HIGH	$I_{\text{CTL I/O}} = -3\text{ mA}$ ; pin CTL DATA = LOW	4.6	–	–	V
<b>WRITE/READ pin 10 (11)</b>						
$V_i$	input voltage	read mode	–	–	0.5	V
		write mode; analog	1.6	–	3.3	V
$I_i$	input current	read mode	–	–1.5	–	$\mu\text{A}$
		write mode	–	0.1	–	$\mu\text{A}$
<b><math>V_{\text{ref}}</math> pin 3 (3); note 2</b>						
$V_O$	output voltage		2.4	2.5	2.6	V
$I_{\text{tot}}$	total current	including write current	–4	–	+4	mA
$R_O$	output resistance		–	0.4	0.6	$\Omega$
<b>CAPREV pin 18 (20)</b>						
$V_{\text{IH}}$	input voltage HIGH		2.0	–	–	V
$V_{\text{IL}}$	input voltage LOW		–	–	0.8	V
$I_{\text{IH}}$	input current HIGH	$V_{\text{CAPREV}} = 5\text{ V}$	–	–	10	$\mu\text{A}$
$I_{\text{IH}}$	input current LOW	$V_{\text{CAPREV}} = 0\text{ V}$	–10	–	–	$\mu\text{A}$

## Control interface for VHS video recorders

## SAA1310

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
<b>CTL DATA pin 16 (18)</b>						
WRITE MODE						
$V_{IH}$	input voltage HIGH		2.0	–	–	V
$V_{IL}$	input voltage LOW		–	–	0.8	V
$I_{IH}$	input current HIGH	$V_{CTL\ DATA} = 5\ V$	–	–	10	$\mu A$
$I_{IL}$	input current LOW	$V_{CTL\ DATA} = 0\ V$	–10	–	–	$\mu A$
READ MODE						
$V_{OL}$	output voltage LOW	$I_{OL} = 0.5\ mA$	–	–	0.4	V
$V_{OH}$	output voltage HIGH	$I_{OH} = -50\ \mu A$	2.4	–	–	V
<b>CPO/FAIL and PO/FAIL OUT pin 4 (4) and 17 (19); see Fig.3</b>						
$V_O$	operating voltage range	at decreasing $V_P$	1.5	–	5.5	V
$V_{OL}$	output voltage LOW	$I_{OL} = 1\ mA$	–	–	0.4	V
$V_{OH}$	output voltage HIGH	$I_{OH} = 1\ mA$	$V_P - 0.9$	–	–	V
$t_d$	delay time	$C_{CAPREV} = 68\ nF$	–	50	–	ms
$V_{TL1}$	threshold level 1		4.5	–	4.8	V
$V_{TL2}$	threshold level 2		–	3.5	–	V
$I_O$	source current pin 4		–	–3	–	$\mu A$
$I_O$	sink current pin 4		–	300	–	$\mu A$
$V_{O(min.)}$	minimum output voltage		–	20	–	mV
$V_{O(max.)}$	maximum output voltage		–	2.1	–	V
<b>High output current type comparators</b>						
CIN3 and CIN4 pins 7 (8) and 8 (9)						
$V_{hys}$	input hysteresis		–	10	–	mV
$V_{IL}$	input voltage LOW		–	–	$V_{ref} - 10\ mV$	V
$V_{IH}$	input voltage HIGH		$V_{ref} + 10\ mV$	–	–	V
$I_{IL}$	input current LOW	$CIN3 = CIN4 = 0\ V$	–1	–	–	$\mu A$
$I_{IH}$	input current HIGH	$CIN3 = CIN4 = V_P$	–	–	+ 1	$\mu A$
COUT3 and COUT4 pins 13 (14) and 11 (12)						
$V_{OL}$	output voltage LOW	$I_{OL} = 100\ mA$	–	–	1.0	V
		$I_{OL} = 2\ mA$	–	–	0.4	V
$\pm I_{OL}$	leakage current	output voltage HIGH; $COUT3 = COUT4 = 17\ V$	–	–	1	$\mu A$
$t_{tr}$	transient time	note 3	–	0.5	–	$\mu s$
$T_j$	thermal protection		–	130	–	$^{\circ}C$

## Control interface for VHS video recorders

SAA1310

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
<b>Low output current type comparators</b>						
CIN1 AND CIN2 pins 5 (6) and 6 (7)						
$V_{hys}$	input hysteresis		–	10	–	mV
$V_{IL}$	input voltage LOW		–	–	$V_{ref} - 10 \text{ mV}$	V
$V_{IH}$	input voltage HIGH		$V_{ref} + 10 \text{ mV}$	–	–	V
$I_I$	input current	CIN1 = CIN2 = 0 V	–1	–	–	$\mu\text{A}$
		CIN1 = CIN2 = $V_P$	–	–	+1	$\mu\text{A}$
COUT1 AND COUT2 pins 15 (17) and 14 (15)						
$V_{OL}$	output voltage HIGH	$I_{OH} = -100 \mu\text{A}$	4.5	–	–	V
$V_{OH}$	output voltage LOW	$I_{OL} = 2 \text{ mA}$	–	–	1	V
$t_{tr}$	transient time	note 4	–	0.5	–	$\mu\text{s}$

**Notes to the characteristics**

1. Without the sink current of the comparators; in write mode.
2. Minimum value of capacitor connected to this pin is 4.7  $\mu\text{F}$ .
3.  $V_i = 100 \text{ mV p-p}$ . Inputs connected to  $V_{ref}$  via a 10 k $\Omega$  resistor; outputs connected to  $V_P$  via a 250  $\Omega$  resistor.
4.  $V_i = 100 \text{ mV p-p}$ . Inputs connected to  $V_{ref}$  via a 10 k $\Omega$  resistor; outputs connected to  $V_P$  via a 2.5 k $\Omega$  resistor.



Control interface for VHS video recorders

SAA1310

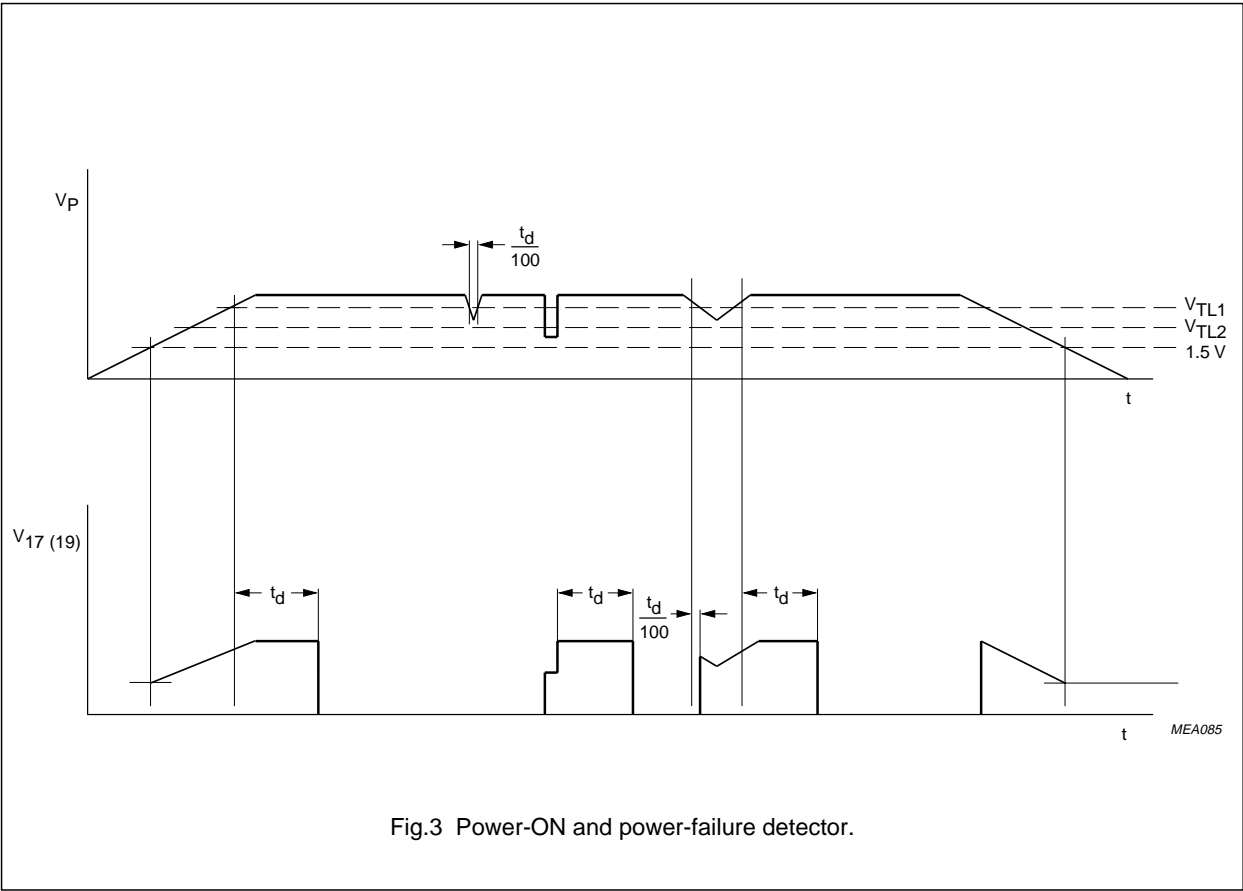


Fig.3 Power-ON and power-failure detector.

Control interface for VHS video recorders

SAA1310

APPLICATION INFORMATION

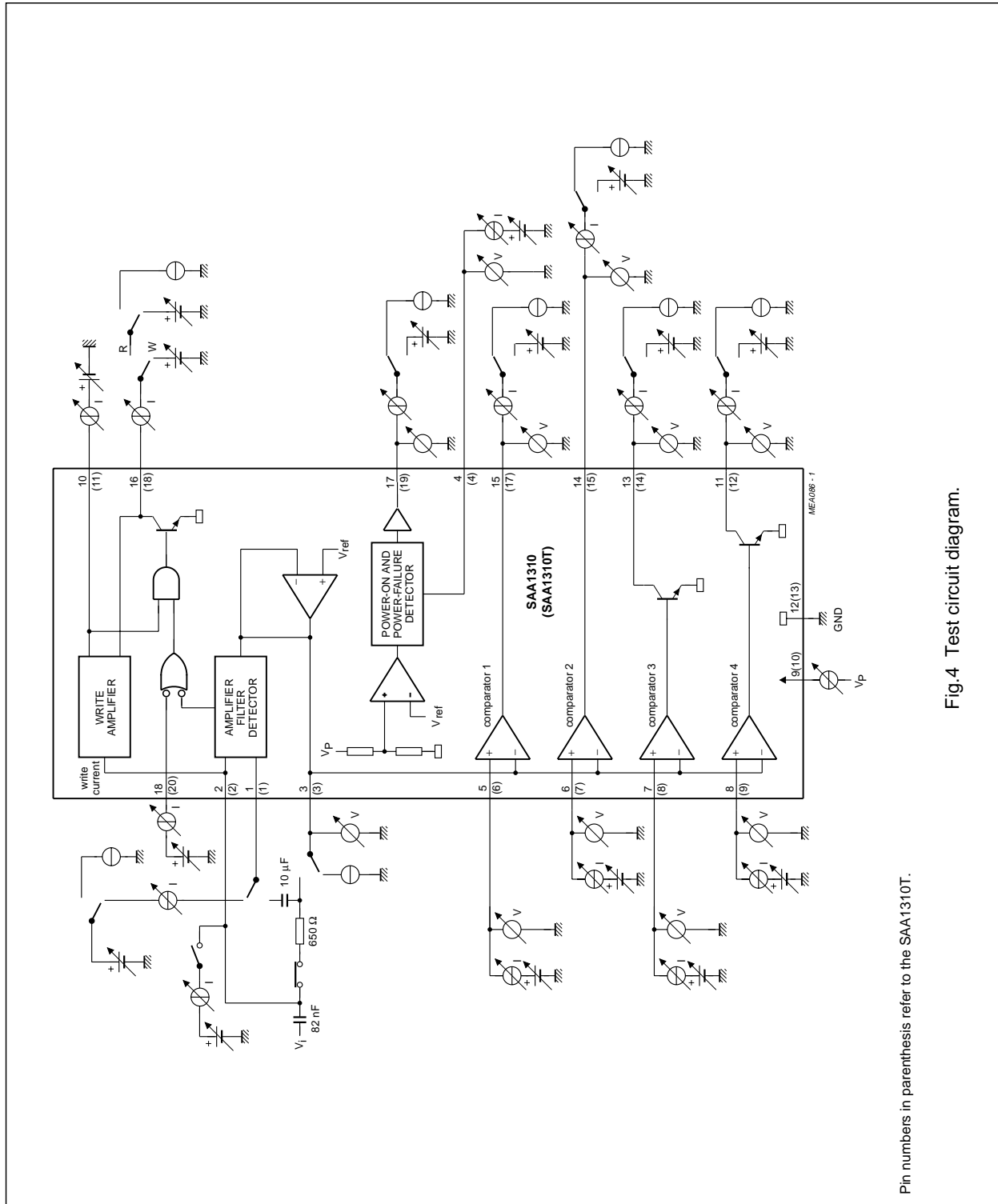


Fig.4 Test circuit diagram.

Control interface for VHS video recorders

SAA1310

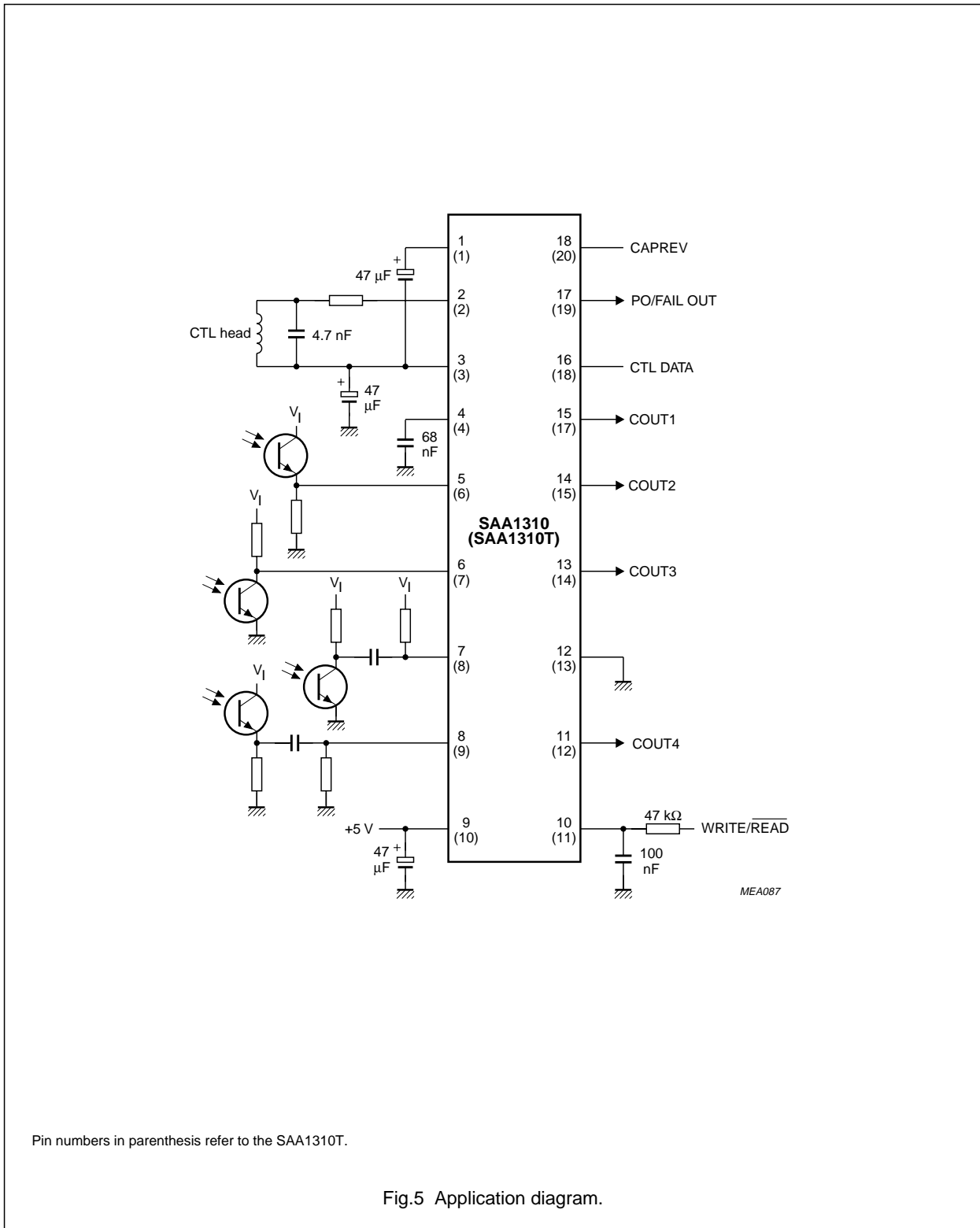


Fig.5 Application diagram.

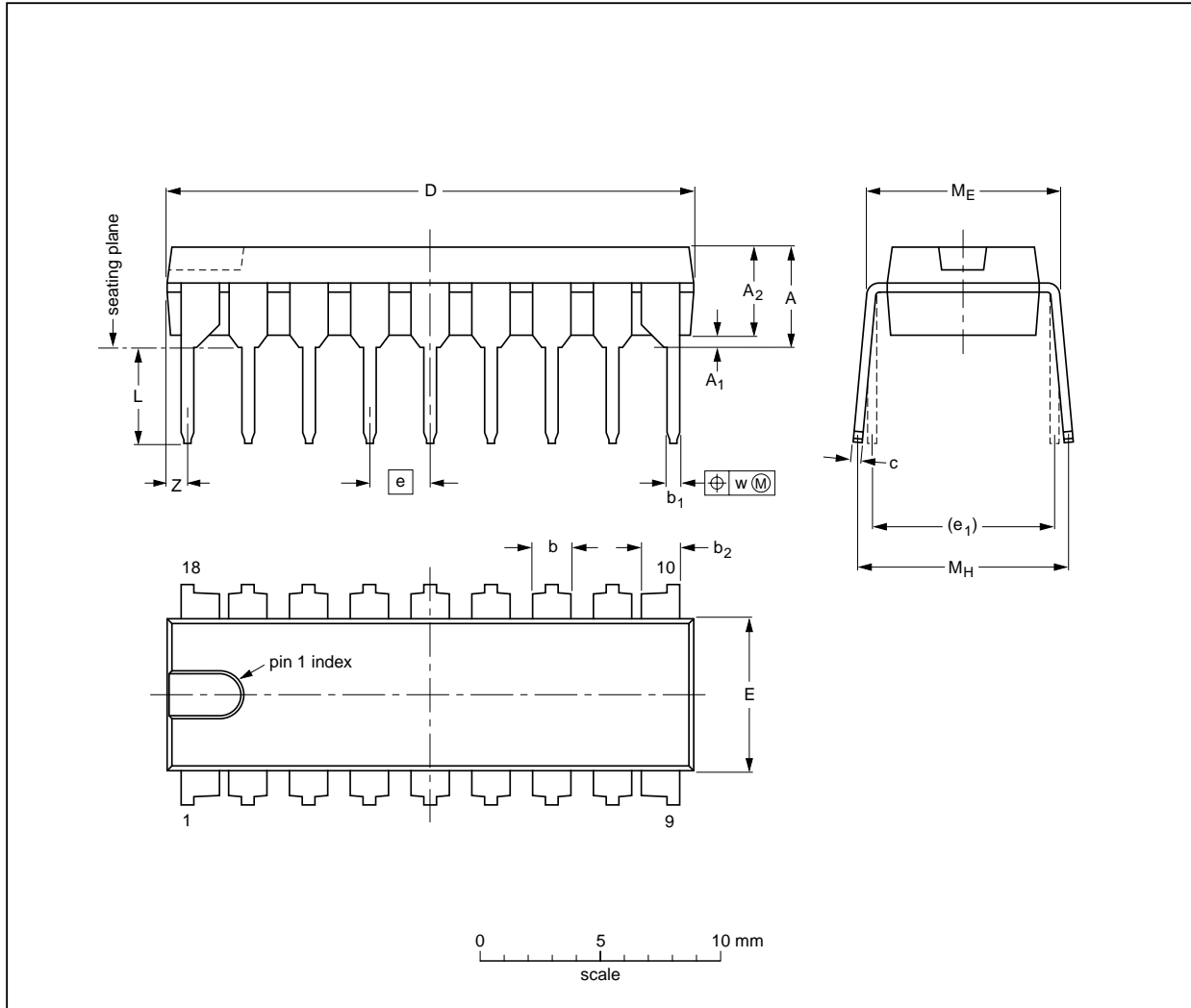
Control interface for VHS video recorders

SAA1310

PACKAGE OUTLINES

DIP18: plastic dual in-line package; 18 leads (300 mil)

SOT102-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

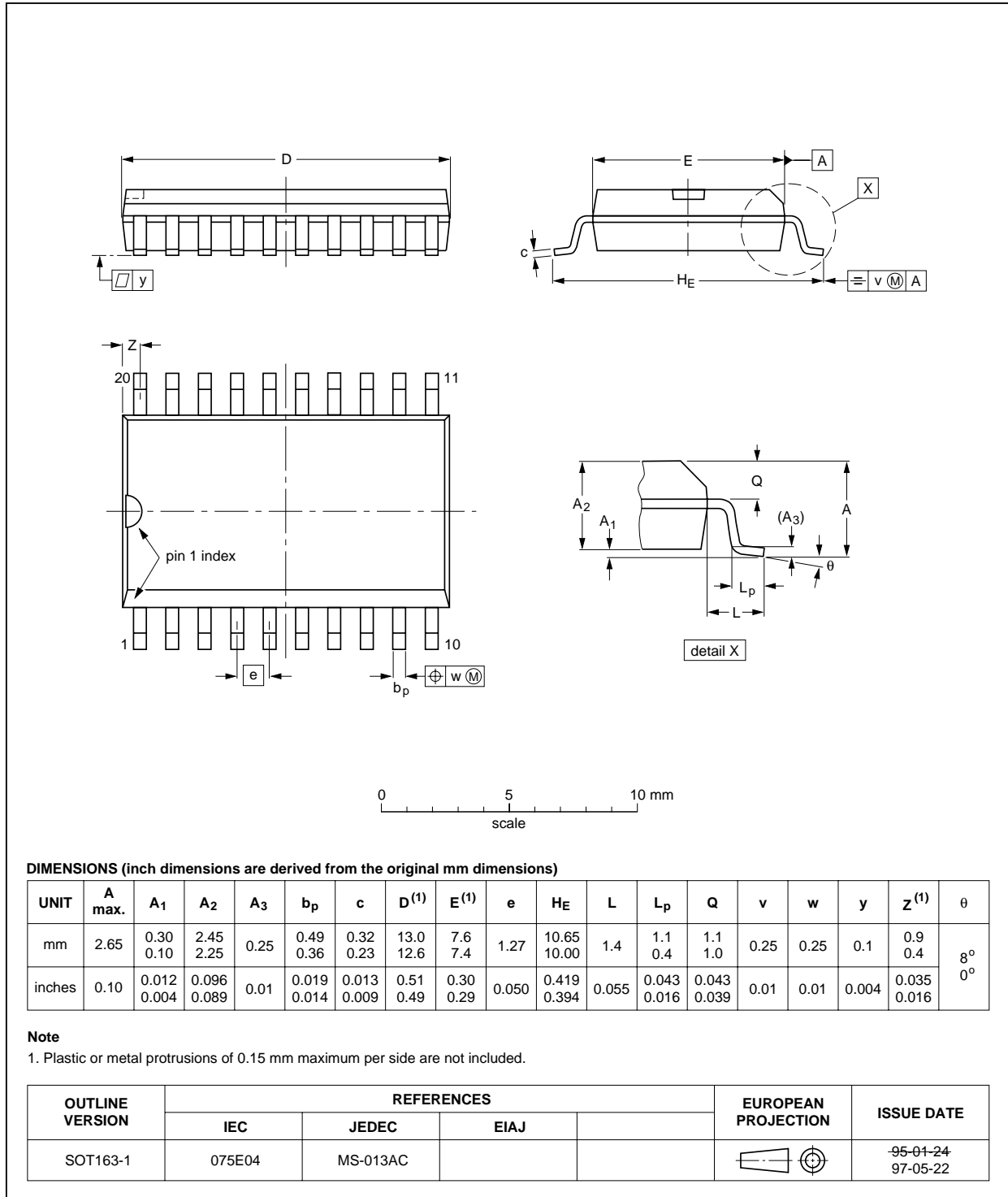
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						93-10-14 95-01-23

Control interface for VHS video recorders

SAA1310

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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## Control interface for VHS video recorders

## SAA1310

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Control interface for VHS video recorders

SAA1310

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

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