Signetics

SAA1061
Output Port Expander

Product Specification

Linear Products

DESCRIPTION

The SAA1061 is an NMOS output port expander circuit, which converts serial input data into parallel output information. The IC is used in combination with a microcomputer.

The SAA1061 is an addressable output port expander for use in microcomputer-controlled systems. It converts serial input data into parallel output information. The circuit comprises a CBUS receiver, logic to check input format, a 16-bit serial/parallel converter, latches and drivers for the parallel outputs.

The data is transmitted via the 3-line CBUS from the microcomputer. If the data transmission is valid, the data is transferred by a load pulse via the latch to the driver output. Each data transmission is checked for word length (18-bit) by the on-chip word format control circuitry. This allows different bus information to be supplied on the same bus lines for other circuits.

The address inputs A_0 and A_1 determine four address possibilities. A data transmission only takes place if the programmed addresses correspond with the address bits S0 and S1.

FEATURES

- **Bus control for the selection of 18-bit words**
- **16-bit latch and low-ohmic driver outputs**
- **Pin compatible with the SAA1060, except the SAA1061 has no duplex mode**
- **Address selection inputs; up to four SAA1061 circuits can be operated from a common CBUS**

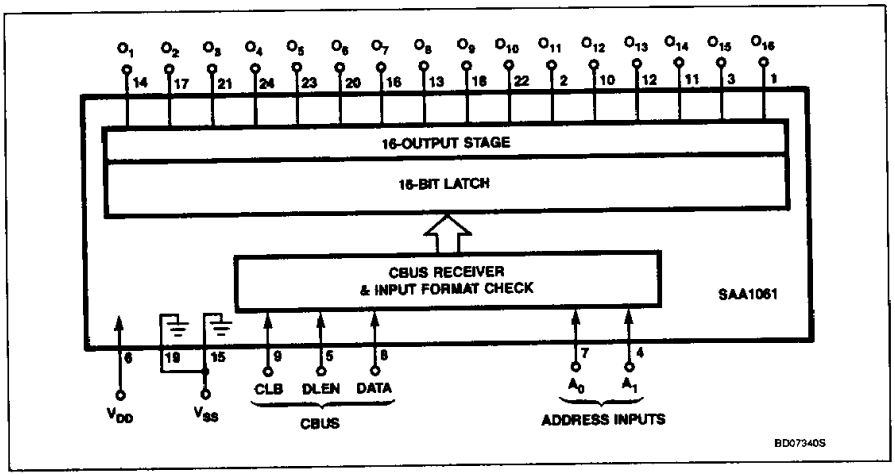
APPLICATIONS

- **LED driver**
- **μP output port expander**

ORDERING INFORMATION

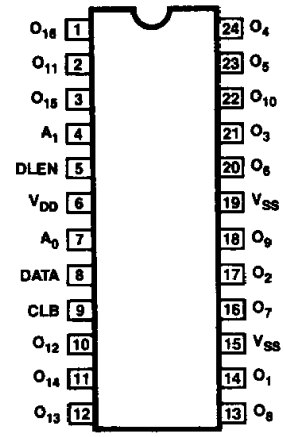
DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
24-Pin Plastic DIP (SOT-101A)	−20°C to +80°C	SAA1061N

BLOCK DIAGRAM



PIN CONFIGURATION

N Package



TOP VIEW

CD10780S

PIN NO.	SYMBOL	DESCRIPTION	
6	V_{DD}	Positive supply (+5V)	
15, 19	V_{SS}	Ground (0V)	
Inputs			
4	A_1	Address bit S1	C BUS
5	DLEN	Data line enable	C BUS
7	A_0	Address bit S0	C BUS
8	DATA	Data word	C BUS
9	CLB	Clock burst	C BUS
Outputs			
1	O_{16}		
2	O_{11}		
3	O_{15}		
10	O_{12}		
11	O_{14}		
12	O_{13}		
13	O_8		
14	O_1		
16	O_7		
17	O_2		
18	O_9		
20	O_6		
21	O_3		
22	O_{10}		
23	O_5		
24	O_4		

Driver outputs O_1 to O_{16} corresponding with the data bits 1 to 16 of the data word.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Supply voltage range	−0.3 to +7.5	V
V_{IN}	Input voltage range	−0.3 to +15	V
$\pm I_{IN}$	Input current	10	mA
V_{OUT}	Output voltage range	−0.3 to +16.5	V
$\pm I_{OUT}$	Output current per output	20	mA
P_O	Power dissipation per output	7.5	mW
P_{TOT}	Total power dissipation per package	300	mW
T_A	Operating ambient temperature range	−20 to +80	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{SS} = 0V; V_{DD} = 5V; T_A = −20 to +80°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5	5.5	V
I_{DD}	Supply current				20	mA
Inputs CLB, DLEN, DATA, A_0, A_1						
V_{IL}	Input voltage LOW	T_A = 25°C	−0.3		0.8	V
V_{IH}	Input voltage HIGH		2.0		15	V
I_{IR}	Input leakage current	V_I = −0.3 to +15V			1	μA
Outputs O_1 to O_{16} (open-drain)						
V_{OL}	Output voltage LOW	I_{OL} = 15mA			0.65	V
I_{OH}	Output leakage current HIGH	V_{OH} = 16.5V			20	μA
t_R, t_F	Rise and fall times	V_{OL} = 1.5V; V_{OH} = 13.5V			10	μs
C BUS timing						
t_R, t_F	Rise and fall times	see Figure 1			2	μs
t_{SUDA}	Data setup time: DATA → CLB		400			ns
t_{HDDA}	Data hold time: DATA → CLB		250			ns
t_{SUEN}	Enable setup time: DLEN → CLB		400			ns
t_{SUDI}	Disable setup time: CLB → DLEN		600			ns
t_{SULD}	Setup time: DLEN → CLB (load pulse)		400			ns
t_{WH}, t_{WL}	CLB pulse width HIGH/LOW		450			ns

Output Port Expander | SAA1061

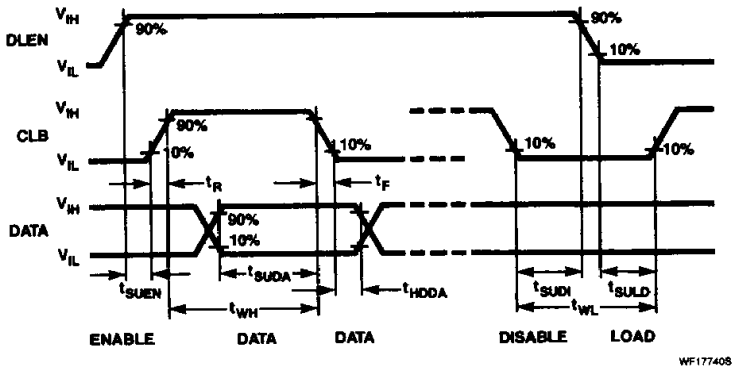


Figure 1. C BUS Timing

OPERATION DESCRIPTION

1. CBUS Transmission

The data words are entered via a serial CBUS interface. A clock burst of 18 clock periods is used to transmit the 16-bit data word, plus 2 identifier bits.

Serial data words, which are synchronized with the clock burst (CLB), are accepted if the enable input DLEN is HIGH at the same time. Each transmission is checked for word length (number of clock pulses during DLEN is HIGH) and the address bits S0 and S1.

The valid data flag is only set if:
1. Word length is correct; 2 address bits and 16 data bits.
2. Address bits S0 and S1 correspond with A_0 and A_1.

Loading the information into the selected latch register is done by the load pulse (first clock pulse after the HIGH-to-LOW transition of DLEN) if the address bits correspond with A_0 and A_1. The load pulse or a new LOW-to-HIGH transition of DLEN resets the valid data flag. Only after the valid data flag is reset, will new data be accepted.

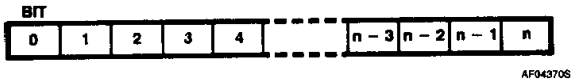


Figure 2. Data Word Organization

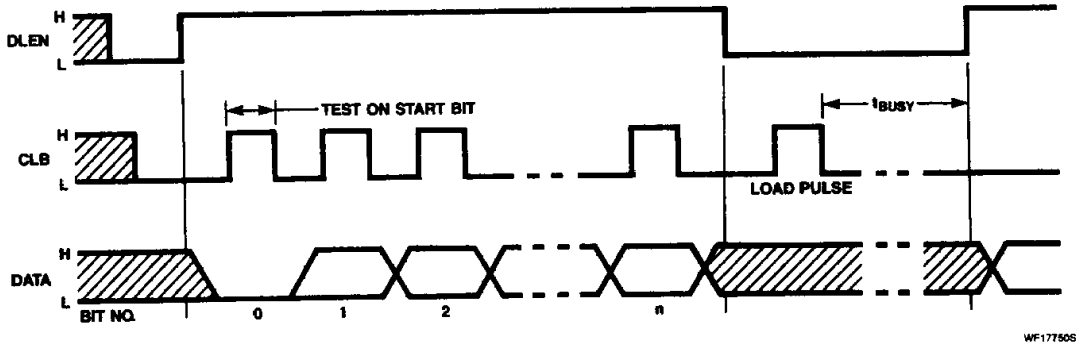


Figure 3. CBUS Data Transmission

Definitions to Figures 2 and 3:

- Word length: number of clock pulses during DLEN is active (HIGH); n + 1 bits = 18 bits.
- Bit number 0 is for the SAA1061 S0.
- Data bits: bit numbers 1 to n-1 (16-bits); bit no. n is S1.
- Load pulse: first clock pulse after DLEN returns to inactive (LOW).

2. Address Inputs A_0 and A_1

The 1st bit (bit S0) and the 18th bit (bit S1) of the data word are the address bits. Data is accepted only if the addresses correspond to the programmed addresses at inputs A_0 and A_1, that is for:

A_0 = S0 and A_1 = S1.

3. Data Outputs O_1 to O_{16}

The outputs O_1 to O_{16} correspond with the data bits 1 to n-1 (16-bits). The open-drain driver outputs (O_1 to O_{16}) are switched to ground (O_n = LOW), if the corresponding data bit is LOW.

4. Power-On Reset

The circuit generates internally a reset-cycle after switching on the supply and the outputs become high-ohmic (HIGH).