DATA SHEET

GTL2001
22-bit GTL processor voltage clamp

Product specification

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Philips
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22-bit GTL processor voltage clamp GTL2001

FEATURES

- Direct interface with TTL level
- 6.5Ω ON-state connection between port S_n and D_n

DESCRIPTION

The GTL2001 provides twenty-two bits of high-speed voltage clamps. The low ON-state resistance of the clamp allows connections to be made with minimal propagation delay.

The device is organized as one 22-bit voltage clamp. When S or D is low the clamp is in the ON–state and a low resistance connection exists between the S and D ports. When S port and D port are high, the clamp is in the OFF-state and a very high impedance exists between the S and D ports. When the D port is high, the voltage on the S port is clamped to the applied reference voltage on the G_{REF} port.

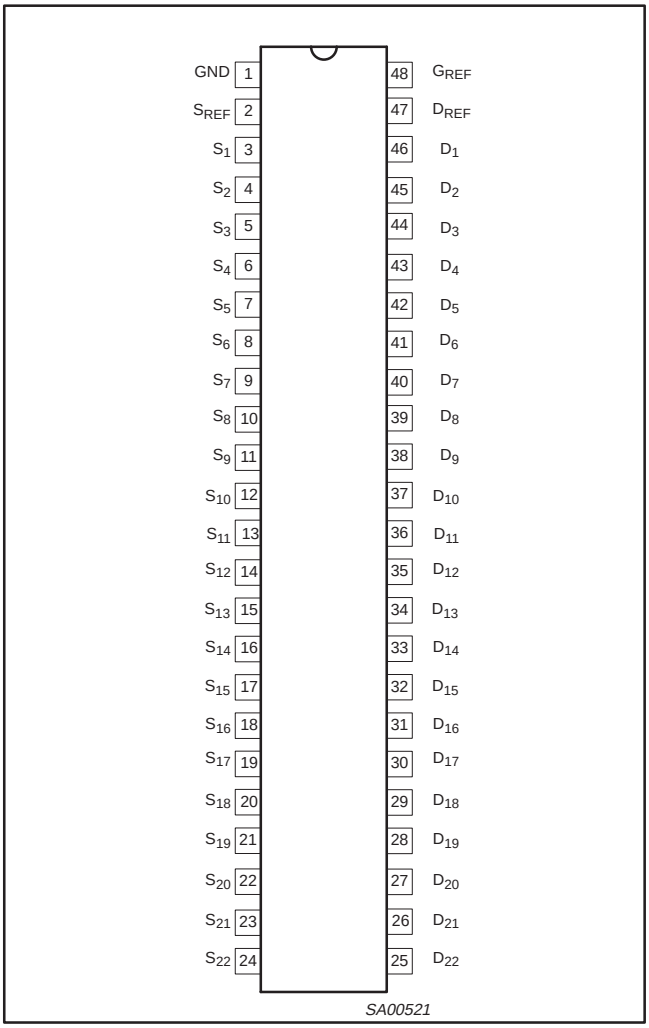
FUNCTION TABLE

G_{REF}	D_{REF}	S_{REF}[4]	Switch	Driven Input	Output of Driven Input
H	H	0 V	off	X	X
H	H	V_{TT}	on	H	V_{TT}[1]
H	H	V_{TT}	nearly off	V_{TT}	H[2]
L	L	V_{TT}	on	L	L[3]
L	L	0 – V_{TT}	off	X	X

H = High voltage level
L = Low voltage level
X = Don't Care

NOTES:
1. The output is not pulled up or pulled down.
2. The output is pulled up to V_{CC} through an external resistor.
3. The driven output can be S_n or D_n; the output of drivn input follows the input low.
4. G_{REF} must be at least 1.5 V higher than S_{REF} for proper switch operation.

PIN CONFIGURATION



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH}	Propagation delay Sn to Dn	V_{DD1} = 3.3 V; V_{DD2} = 2.5 V; V_{REF} = 1.5 V; unloaded	1.5	ns
C_{OFF}	Channel capacitance (OFF-state)	V_S = 1.5 V	7.5	pF

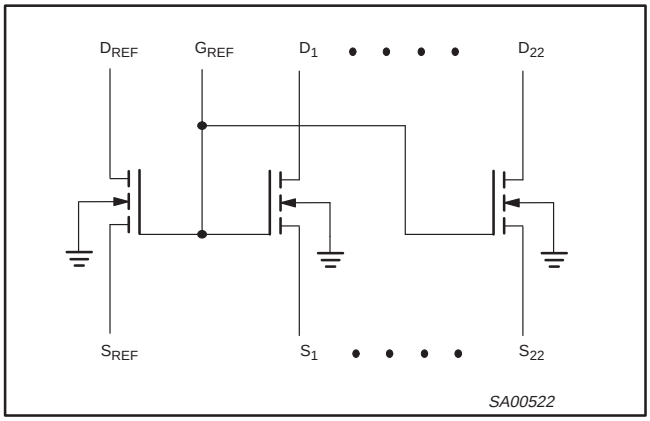
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic SSOP Type II	0°C to +85°C	GTL2001 DL	SOT370–1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	GND	Ground (0V)
2	S_{REF}	Source of reference transistor
3 – 24	S_n	Port S_1 to Port S_{22}
25 – 46	D_n	Port D_1 to Port D_{22}
47	D_{REF}	Drain of reference transistor
48	G_{REF}	Gate of reference transistor

CLAMP SCHEMATIC



ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{S_REF}	DC source reference voltage		–0.5 to +7.0	V
V_{D_REF}	DC drain reference voltage		–0.5 to +7.0	V
V_{G_REF}	DC gate reference voltage		–0.5 to +7.0	V
V_{Sn}	DC voltage Port S_n		–0.5 to +7.0	V
V_{Dn}	DC voltage Port D_n		–0.5 to +7.0	V
I_{REFK}	DC reference diode current	$V_I < 0$	–50	mA
I_{SK}	DC diode current Port S_n	$V_I < 0$	–50	mA
I_{DK}	DC diode current Port D_n	$V_I < 0$	–50	mA
I_{MAX}	DC clamp current per channel	Channel in ON-state	±35	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{S_REF}	DC source reference voltage		1.0	4.4	V
V_{D_REF}	DC drain reference voltage		V_{S_REF} + 0.6	5	V
V_{G_REF}	DC gate reference voltage		V_{S_REF} + 0.6	5	V
V_{Sn}	DC voltage Port S_n (OFF-state)		V_{S_REF}	5	V
V_{Sn}	DC voltage Port S_n (ON-state)		0	0.2	V
V_{Dn}	DC voltage Port D_n (OFF-state)		V_{S_REF}	5	V
V_{Dn}	DC voltage Port D_n (ON-state)		0	0.4	V
I_S	Switch input leakage current (OFF-state) for S_n and D_n I/O	V_S , V_D = 5 V		15	µA
I_I	G_{REF} input leakage current	V_G = 5 V		2.5	µA
T_{amb}	Operating ambient temperature range	In free air	0	+85	°C

DC CHARACTERISTICS for V_{DD1} = 3.0 to 3.6 V; V_{DD2} = 2.36 to 2.64 V; V_{REF} = 1.365 to 1.635 V range

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V). Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = 0°C to +85°C			
			MIN	TYP[1]	MAX	
V_{OL}	LOW level output voltage	V_S = 0.175 V; I_{CLAMP} = 15.2 mA		260	350	mV

NOTE:

1. All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C

AC CHARACTERISTICS for V_{DD1} = 3.0 to 3.6 V; V_{DD2} = 2.36 to 2.64 V; V_{REF} = 1.365 to 1.635 V range

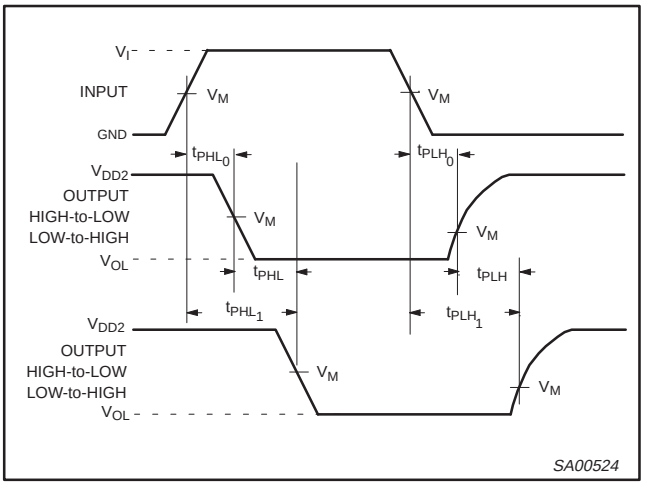
GND = 0V; $t_r = t_f \leq 3.0$ ns. Refer to the Test Circuit diagram.

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = 0°C to +85°C			
			MIN	TYP[1]	MAX	
t_{PLH}[2]	Propagation delay Sn to Dn; Dn to Sn		0.5	1.5	5.5	ns

NOTES:

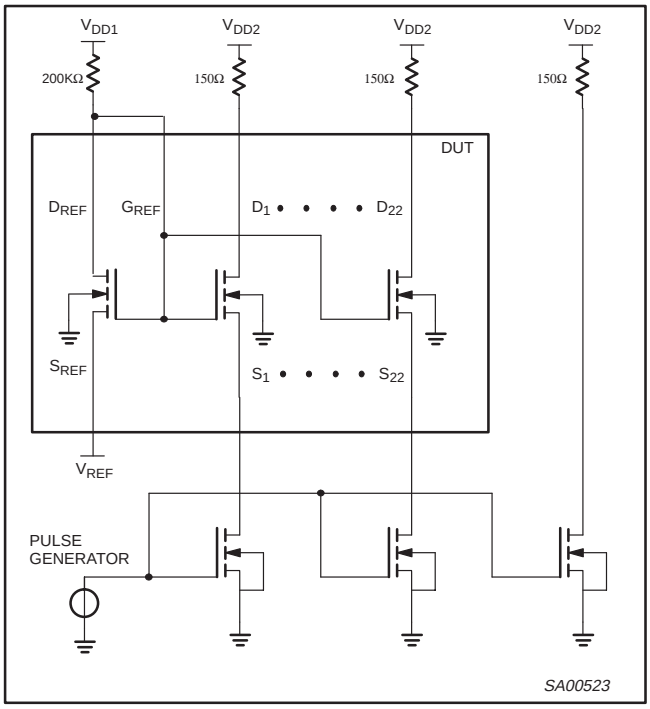
1. All typical values are measured at V_{DD1} = 3.3 V, V_{DD2} = 2.5 V, V_{REF} = 1.5 V and T_{amb} = 25°C.
2. Propagation delay guaranteed by characterization.
3. $C_{ON,MAX}$ of 30 pF and a $C_{OFF,MAX}$ of 15 pF is guaranteed by design.

AC WAVEFORMS



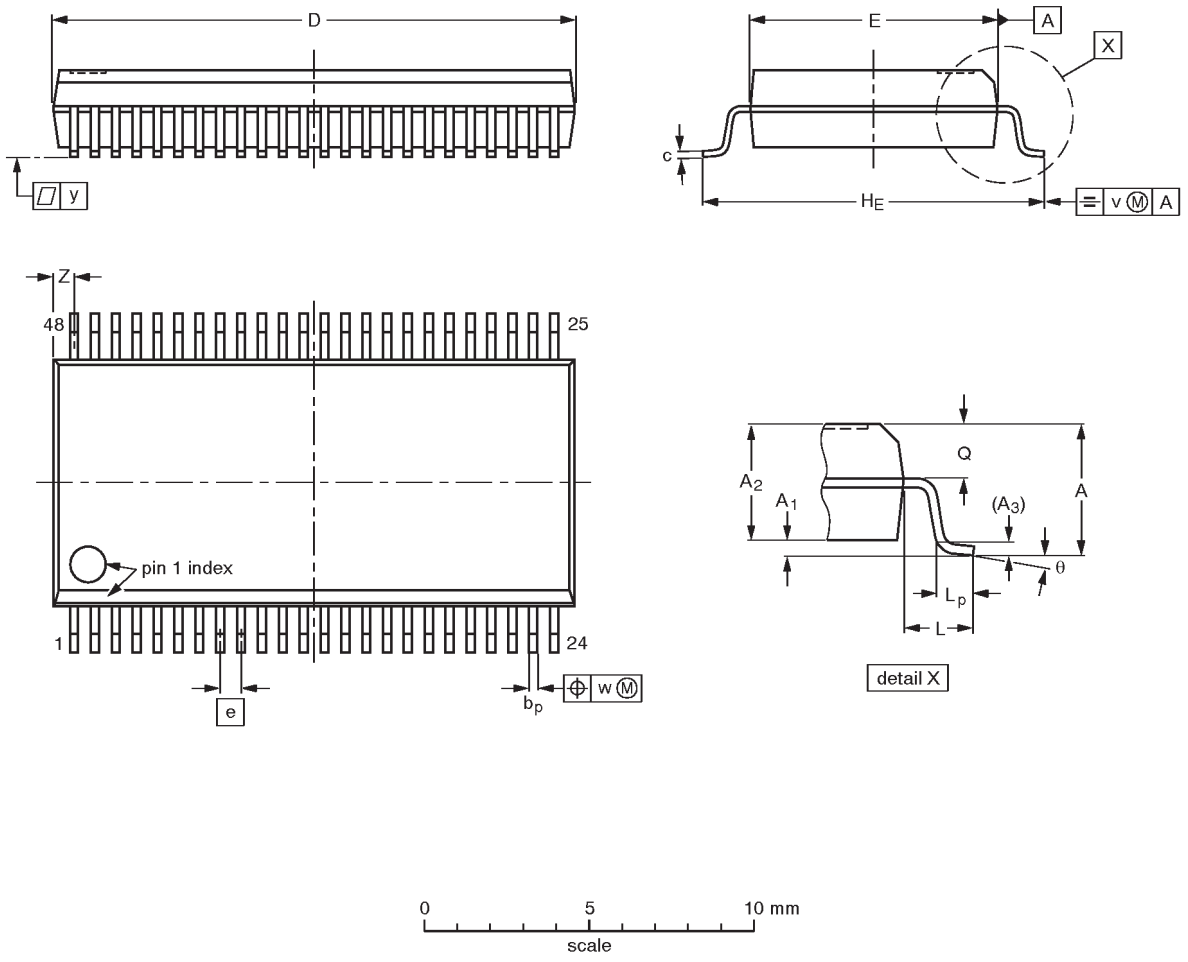
Waveform 1. The Input (S_n) to Output (D_n) Propagation Delays

TEST CIRCUIT



Waveform 2. Load circuit

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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